p.252

INTERNATIONAL

ElectronicDesign®

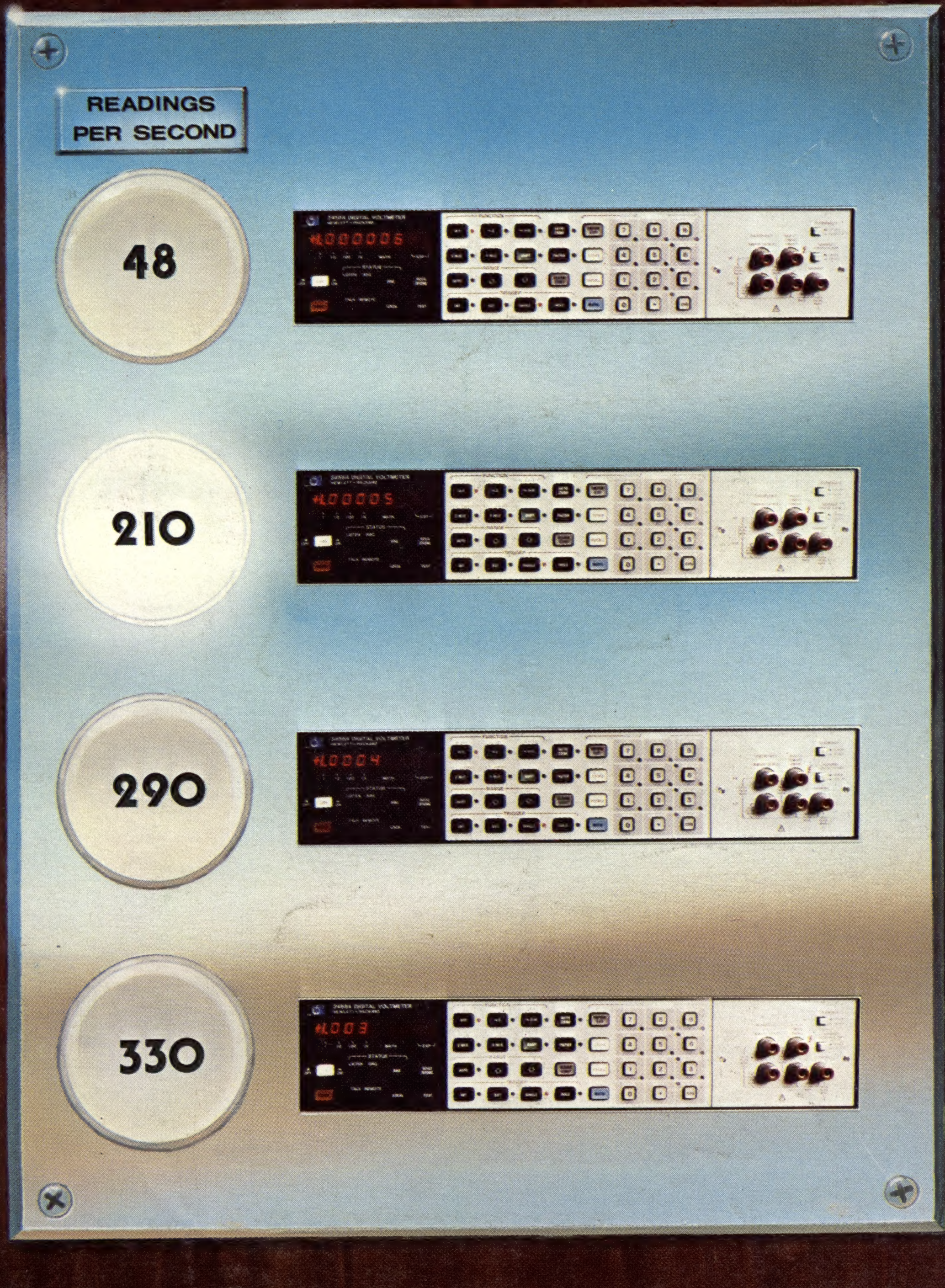
FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

JUNE 7, 1980

Semiconductor Technology Issue

- Linear LSI
- Digital LSI
- Discretes
- Communication ICs
- IC Fabrication

Smart DMM lets you choose performance level



Panasonic: in plastic transistors, we're the source to see first

for industry-standard TIP and high-technology TOP

Some plastic transistors are so commonly used, they're industry standards. Some are more advanced, to meet high-technology standards. Whichever type does the job for your next power amplifier, high-speed switching application or design, Panasonic is the source to see first.

Low cost: just one reason for specifying industry-standard TIP.

Our rugged TIP TO-220 package is the all-silicon transistor that gives you a lot more than price. Its reliability is proven in life tests. And with seven series of NPN and PNP devices, it gives you the right voltage, current and power specs: I_c 1-10 Amps, V_{ce} 40-400 volts, P_c-30 W.

High technology: TOP sets the pace.

Panasonic (TOP-3) high power plastic audio transistors meet your needs with innovative design. Their FE (Floating Emitter) structure allows a wider safe-operating range—significantly more than conventional metal types.

And reliability is built-in with the Panasonic combination of "fine comb" construction, a die-bond technique that provides positive contact to the chip, and single-point mounting that reduces thermal-mechanical stress.

Ranging from 60-100 watts, each high power device has leads that can be easily formed to meet JEDEC TO-3 mounting dimensions. Add the cost-effectiveness of plastic vs. metal construction, and you've got one powerful design aid.

For facts and figures demonstrating the see-us-first benefits of Panasonic TIP/TOP transistors, write to: Panasonic Electronic Components, One Panasonic Way, Secaucus, N.J. 07094; or call (201) 348-7269.

Panasonic®

just slightly ahead of our time

CIRCLE NO. 131

Unless money is no object, Wavetek's new Model 859 Programmable Pulse Generator is obviously the way to go. First of all, the under-$8,000 price is for single channel operation. Our dual-channel version is priced about the same as other single-channel instruments!

Either way, the Model 859 is a high-performance, GPIB-compatible instrument for bench or ATE applications. You can program frequencies from 0.5 Hz to 50 MHz, pulse widths from 10 nanoseconds to 1 second, delays to 1 second, transition times from 5 nanoseconds to 25 milliseconds, and output levels up to 20 volts. For repetitive testing, you can store and recall up to 25 setups (which eliminates the need for a controller).

Besides economy, the key features of the 859 are accuracy and quality. Timing accuracy, for example, is 2%. And the microprocessor-assisted programming gives you pulse fidelity like you've never seen before.

Getting back to price: the money you save with the 859 will probably cover most of your software costs. But don't take our word for it. Call us and arrange a complete demonstration of the Model 859, and find out what pulse quality and value are really about.

Wavetek, 9045 Balboa Avenue,
P.O. Box 651, San Diego, CA 92112.
Tel. (714) 279-2200. TWX 910-335-2007.

WAVETEK®

FOR DEMONSTRATION CIRCLE NO. 2

FOR LITERATURE CIRCLE NO. 220

Some $11,000 programmable pulse generators perform as well as this one.
Unfortunately for them, this one sells for under $8,000.

ElectronicDesign
June 7, 1980 • Vol. 28 No. 12

Departments

5 Publisher's Memo
9 Editorial
13 Letters
15 Meetings
289 Your Profession
308 Index of Advertisers
310 Reader Service Card

News

25 Late News
31 Advanced peripheral chips coming to support MC68000.
32 Compatibility—the key to future board computers.
34 Software package handles "personal" high-level math.
38 Power transistors in solid copper take high currents.
38 μP-based devices simplify data-comm networks.
42 ROM-based keyboard sets up ideographic characters.
47 Washington Report
52A International Section

63

Semiconductor Special

63 Introduction: No limits in sight.

65 E-beams, new processes write a powerful legacy.

Geometries are moving to 1 μm, propelled by advanced fabrication techniques. Lithography, step-and-repeat optical projection, ion beam implantation and dry plasma etching—all play a role.

75 Memory and μP ICs pack more, consume less.

Processing and innovative structures have boosted densities in the latest memory and μP ICs, while bringing memorable performance improvements.

95 Converters show off linear LSI processing.

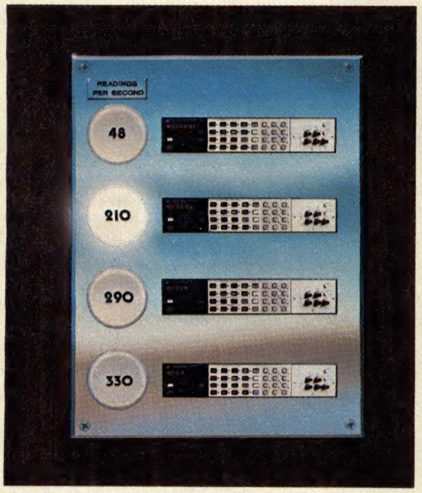
Although higher-resolution ADCs and DACs are imminent, 8 and 10-bit converters keep on improving with easier interfacing to μPs, simpler power-supply requirements and faster conversions.

109 ICs ride the tidal wave of data comm, telecomm.

For telecomm chips, the route to better performance, reliability, size, power and cost lies in processing, material and circuitry; for data-comm chips, the key is basically architecture.

131 MOS power vs bipolar—the designer wins.

With power-handling capability and breakdown voltages on the rise in both bipolar and MOS transistors, competition between the two is heating up. Designers can choose from the best of both.



149

Design

149 DVM gets speedy, accurate results (cover).

Instead of settling for the usual compromise between reading speed and accuracy or other parameters, a new digital voltmeter makes the best combination available for the choosing.

159 Macrocell approach customizes fast VLSI.

The Macrocell Array concept relies on sets of SSI and MSI functions, computer-aided design and high-density bipolar technology to create high-speed VLSI quickly and reliably.

171 16-bit architecture brings VLSI computing.

The general, floating-point and special-purpose registers, addressing modes and instructions of the 16000 processor show an aptitude for high-level languages and computations.

181 Match the converter with the application.

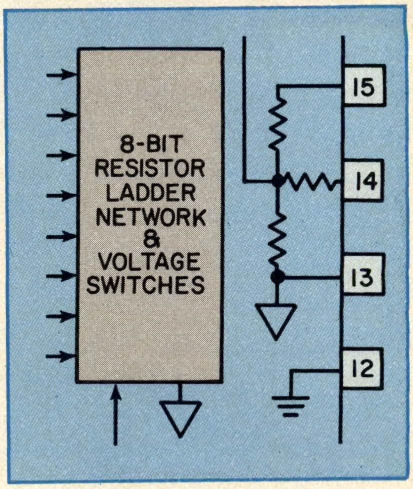
Analog-to-digital and digital-to-analog IC converter components come in a choice of technologies: bipolar, CMOS or hybrid. Each offers special advantages. But which will do the most good?

191 Controller plugs SDLC into 16-bit μP systems.

Bring the advantage of synchronous data-link control to 16-bit μP systems with a synchronous controller that simplifies all the interfacing.

199 Ideas for Design:

Broadband phase-sensitive detector needs just five components.
NOR gate unlatches pseudorandom noise generator.
Differential amplifier design avoids op amps.



181

Products

207 **Analog Circuits:** 2 hybrids make hi-rel, 12-bit data system.
208 ADC modules boost accuracy while cutting costs.
210 6-bit DAC has voltage output.
212 **Instruments:** Process monitor balances complexity, cost.
215 Stand-alone instrument emulates the Z8000.
216 Handheld multimeter ranges automatically.
218 Logic analyzer premieres with 32-channel timing.
224 Control unit changes data acquisition.
226 **Microsystems:** STD-Z80 board takes many memory combos.
234 **Packaging & Production:** Wafer trimmer speeds things up.
249 **Digital Circuits:** Nonvolatile RAM needs just two supplies.
256 **Components:** Mini-DIP ICs drive ac plasma displays.
258 LCD provides big display with low power.
268 **Peripherals:** Tape drives stress reliability.
270 Printer/plotter works in four colors.
274 **Computers:** Apples do word processing or info analysis.
252 **Materials**
276 **Communications**
282 **Subassemblies**
284 **New Literature**
288 **Evaluation Samples**

Coming in the June 21 issue:

Special Report on Packaging ... Focus Report on rf and microwave instrumentation ... First details on a major ATE system ... The inside story on a fast, monolithic, successive-approximation a/d converter ... Selecting high-speed ribbon cable ... Elastomeric connectors—pros and cons ... Interconnect high-speed ECL systems.

Cover: Instrument photos courtesy of Hewlett-Packard.

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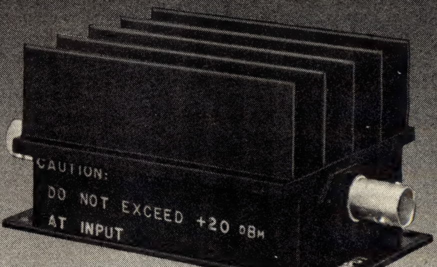
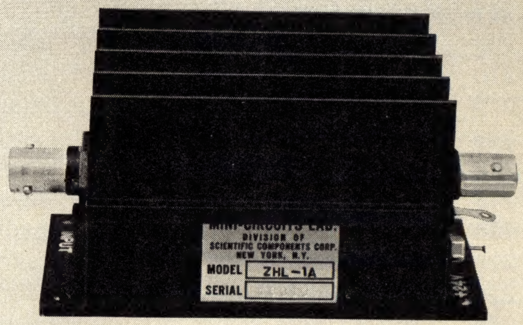


ZHL-2-8

If your application requires up to 1 watt for intermodulation testing of components ... broadband isolation ... flat gain over a wide bandwidth ... or much higher output from your frequency synthesizer or signal/sweep generator ... MiniCircuits' ZHL power amplifiers will meet your needs, at surprisingly low prices. Five models are available, offering a selection of bandwidth and gain.

Using an ultra-linear Class A design, the ZHL is unconditionally stable and can be connected to any load impedance without amplifier damage or oscillation. The ZHL is housed in a rugged ⅛ inch thick aluminum case, with a self-contained hefty heat sink. BNC connectors are supplied; however, SMA, TNC and Type N connectors are also available. Of course, our one-year guarantee applies to each amplifier.

So from the table below, select the ZHL model for your particular application now ... we'll ship within one week!



ZHL-1A

MODEL NO.	FREQ. MHz	GAIN dB	GAIN FLATNESS dB	MAX. POWER OUTPUT dBm 1-dB COMPRESSION	NOISE FIGURE dB	INTERCEPT POINT 3rd ORDER dBm	DC POWER		PRICE	
							VOLTAGE	CURRENT	$ EA.	QTY.
ZHL-32A	0.05-130	25 Min.	±1.0 Max.	+29 Min.	10 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	± 1.0Max.	+29 Min.	18 Typ.	+38 Typ.	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 Min.	10 Typ.	+38 Typ.	+24V	0.65A	449.00	(1-9)

Total safe input power +20 dBm, operating temperature 0° C to +60° C, storage temperature −55° C to +100° C, 50 ohm impedance, input and output VSWR 2.1 max.
For detailed specs and curves, refer to 1979/80 MicroWaves Product Data Directory, p. 364-365 or EEM p. 2970-2971.

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46 REV C

CIRCLE NO. 3

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Publisher'sMemo

No electronics technology is more pervasive than semiconductors—it influences the components of today, shapes the systems of tomorrow and brings the convenience and power of electronics to diversified applications all over the world.

To assess the advances in this ever-changing field, ELECTRONIC DESIGN has assembled five major staff-written reports. The first report examines the processing technologies that promise denser chips with better performance at lower costs. "Sophisticated processing techniques are moving digital chips up to VLSI," notes Morris Grossman, Packaging Editor, "with a push coming from electron beams for producing complex masks and writing circuits directly on wafers."

Systems on a chip are evolving into super systems that incorporate circuitry specialized for each application.

According to Dave Bursky, Semiconductors Editor, speech synthesizer chips show off the strength of digital VLSI: "Expect voice I/O for computer systems, talking home appliances and talking automobile dashboards." In addition, he notes, watch for more smart advanced support chips to offload micro chips for a more efficient design.

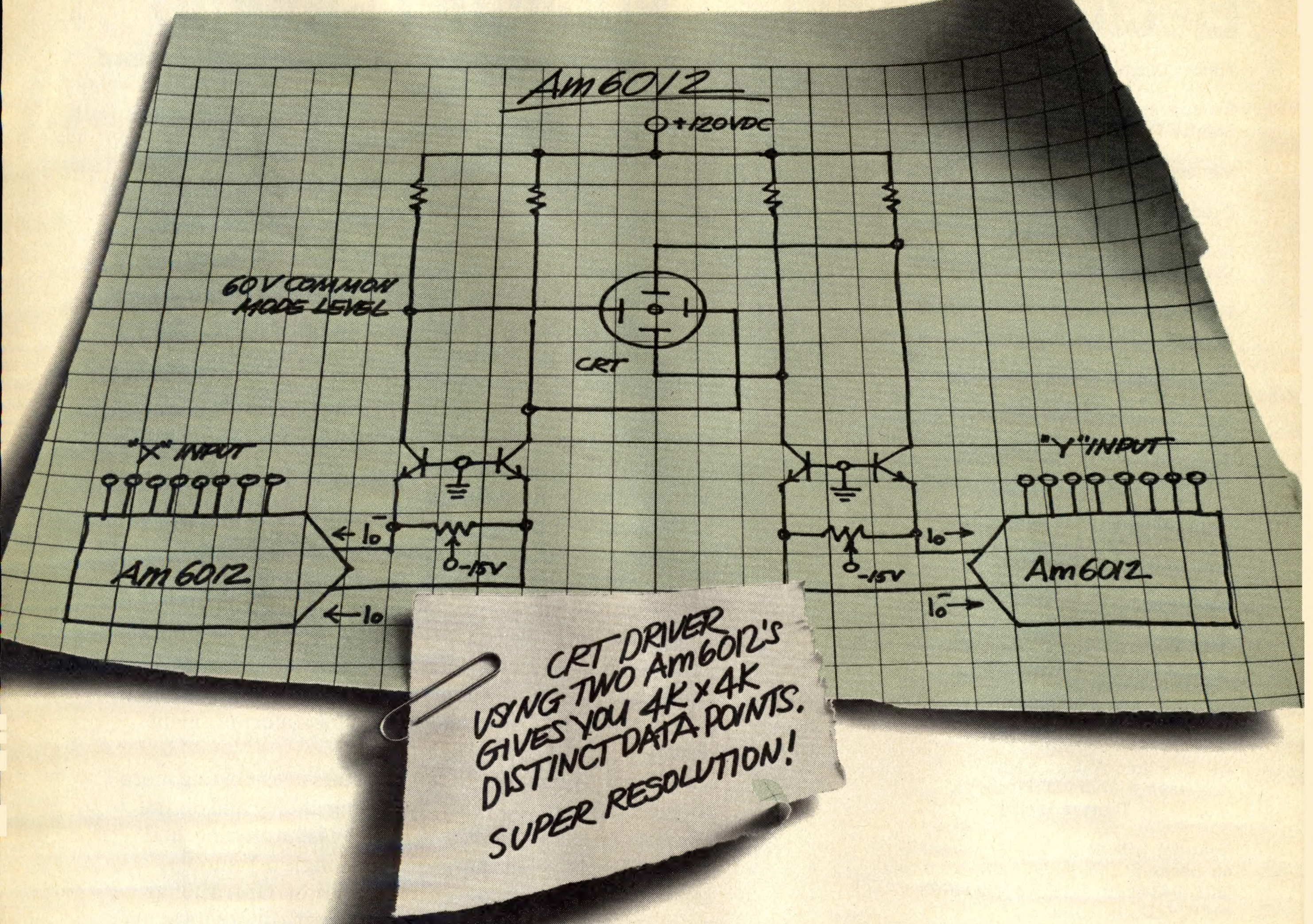
In linear technology, data converters are bringing more user conveniences on board by mixing analog and digital circuitry on the same chip. "Precision is improving, and some converters can operate from a single 5-V supply," reports Steve Ohr, Analog Circuits Editor. Operational amplifiers also mark breakthroughs, with dc errors at an all-time low.

Communications Editor, Sid Adlerstein directs attention to the "powerhouse chips" that control protocols for data communications and to coder/decoder systems that have compatible filtering for telecommunications. "The interface circuits for telephone subscriber lines are especially impressive. They could be the first practical integrated circuits to simulate a transformer with semiconductor technology."

The advances in power technology mean bipolar transistors will switch higher voltages and currents in less time than ever before. Gene Heftman, NY Field Editor, foresees that present trends in planar and V-groove processing will end in power MOSFETs that can handle power at a level and at a cost rivalling those of bipolars.

Our five-part semiconductor special thoroughly analyzes these and other trends in semiconductor technology. The special coverage starts on page 63.

Larry Altman



CRT DRIVER USING TWO Am6012's GIVES YOU 4K×4K DISTINCT DATA POINTS.

SUPER RESOLUTION!

We trimmed the price, not the DAC.

Announcing the Am6012. The lowest priced 12-bit DAC you can buy.

Advanced Micro Devices' new Am6012 12-bit monolithic DAC is only $9.95 in 100-up quantities.

But if you think it's just a stripped down DAC, think again. The only thing we trimmed on the Am6012 was the price. And we mean that literally.

The Am6012 is the world's first monolithic DAC produced with diffused, rather than thin-film, resistors. It requires no active trimming of individual devices.

It's the only 12-bit monolithic DAC to spec ±½ LSB (13-bit) differential nonlinearity over the entire temperature range. The only one to spec NL and DNL at both +5V and +15V supplies. It even offers high-output impedance plus high-voltage compliance: −5V to +10V.

Thanks to the Am6012's innovative design, it is inherently monotonic and fast. It has a 250ns typical settling time.

Thanks to Advanced Micro Devices, you get MIL-STD-883 for free.

If you're looking for the best 12-bit DAC at the best price in town, call or write Advanced Micro Devices. And ask for the Am6012.

The only thing we trimmed was the price.

Advanced Micro Devices

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Mail Operations, P.O. Box 4
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United Kingdom

6/7/80 ED

Send me the facts on your 12-bit DAC'S.

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SURPRISE!

Interface between power and logic with HP's Threshold-Sensing Optocoupler.

With microprocessor control replacing manual, pneumatic or electromechanical systems, isolation between power interface and computer logic is necessary—if not vital.

This new AC/DC threshold-sensing optocoupler from HP features adjustable external threshold levels and logic compatible output providing a smoother interface between power and logic. Ideal for industrial control and process applications—or anywhere a predetermined input threshold level is desired. The HP HCPL-3700 saves design time, board space and offers considerably improved performance over existing couplers.

This is possible because it contains a complex integrated circuit on the input side which processes the electrical input signal before it is passed onto the light emitting diode.

In quantities of 1000, the HCPL-3700 is priced at $3.65* each.

For delivery or for more information, call any franchised HP components distributor. In the U.S., contact Hall-Mark, Hamilton/Avnet, Pioneer Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar).

In Canada, call Hamilton/Avnet or Zentronics, Ltd.

01004

*U.S. Domestic Price Only.

HEWLETT
PACKARD

CIRCLE NO. 5

Editorial

Is our enemy without?

A Senator addressing laid-off automobile workers recently referred to Japan as a "predatory trading partner." We wonder if the Senator's quest for votes has somewhat clouded his understanding of "predatory."

Is it, we wonder, predatory for an industry or enterprise to spot a market vacuum and move in fast with products positioned to fill an overwhelming demand?

Is it predatory to boost the productivity of line workers by giving them the job security they need so as not to feel threatened by new technology or processes?

Is it predatory to motivate assembly-line workers to take pride in craftsmanship, rather than goad them to produce more products faster—at the cost of quality?

Is it predatory for a government to recognize, nurture, encourage and stimulate those industries recognized as sunrise industries—as with electronics or automobiles in Japan?

Is it predatory for a government to deny sustenance to declining, sunset industries, when such support clearly discourages productivity and encourages inflation, as with steel and automobiles in the United States?

Is it predatory for a country to invest a large percentage of its gross national product—Japan invests 20%, the U.S. only 10%—while holding down consumption?

Is is predatory for a government to stimulate R & D spending—to prevent a decline as in the United States? This country spent 3% on R & D in 1970—it spends 2% today.

In a recent survey, American automobile engineers selected Japanese cars as the most reliable in the world. The advantages, claim the engineers, had more to do with motivated assembly-line workers than with the generic designs of the cars.

Our nation needs a new commitment to productivity; and we need it now. We could learn a great deal from Japan and other nations which compete successfully in world markets. We could certainly do better by emulating than by calling names.

Engineering education needs a boost

If the health of engineering education is fundamental to the health of our economy, the U.S. had better brace itself for a decade of malaise.

Enrollment statistics released by the American Association of Engineering Societies in New York point to a situation in our graduate schools that has grown alarming: While Bachelor's degrees increased from 40,000 in 1969 to 53,000 in 1979, Master's degrees grew by a mere 1000 and doctorates dropped from 3400 to less than 2800. Not only that, but about 34% of today's full-time graduate students are foreign citizens—and at the PhD level alone, the figure rises to 40%.

Because most of the foreign students are here on temporary study permits—suggesting they won't stay after graduation—and because the lure of high-paying jobs is keeping undergraduates from going on to advanced degrees, it is clear that our nation will soon suffer from a shortage not only of engineering faculty but also of individuals able to turn out advanced, innovative products.

While it is difficult to forecast future engineering manpower requirements, the AAES recommends some policy changes to help make sure future manpower resources don't dry up:

- The 1967 federal decision to redirect the government's financial support from the institution to the student should be reexamined.
- The National Science Foundation must be reorganized to support fundamental engineering development, or a National Engineering Foundation should be considered.
- At least 2000 two-year fellowships, worth about $8000 a year, should be established to prime the faculty pipeline.
- About $40-million a year must be spent to modernize educational facilities.

A serious situation is in the making. It's up to industry, higher education and government to get together and prevent it.

Through The Looking Glass with the DAC-03

© PMI 1978

In *Through the Looking Glass,* Lewis Carroll introduced Alice to a mirror-image world where things were never what they seemed. In fact, they were just the reverse of what they should be. Punishment came before the crime; answers came before the questions.

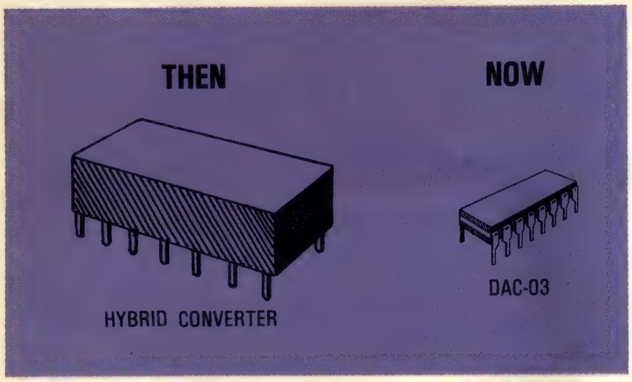
Linear Wonderland is like that sometimes, too. Salesmen spend their commissions before the purchase orders are signed. Marketing departments announce products before engineering develops them.

And at PMI, we try to develop products before anyone else realizes they're needed. We know that in Linear Wonderland, the best products create their own need.

That was how we developed the first truly monolithic D/A converter, the 6-bit DAC-01. At the time, no one thought they needed it because they were "making do" with modules or in-house designs with separate op amps and voltage references. When the DAC-01 (and the 10-bit DAC-02) came along and offered high performance specs with monolithic reliability, a lot of people suddenly found this was *just* what they needed.

PMI has another product we think a lot of engineers need: The DAC-03, a *low cost* 10-bit converter. Like the 10-bit DAC-02, it includes all the elements of a complete DAC on a single chip: precision voltage reference, current steering logic, current sources, diffused resistor ladder network, and high speed internally compensated output op amp. The DAC-03's 25°C tested and guaranteed performance and its low, low price are just what the systems engineer ordered.

The people who haven't needed the DAC-03 (until now) are all those designers who looked at our DAC-02 and decided that their system didn't justify the higher cost of wide temperature range testing.



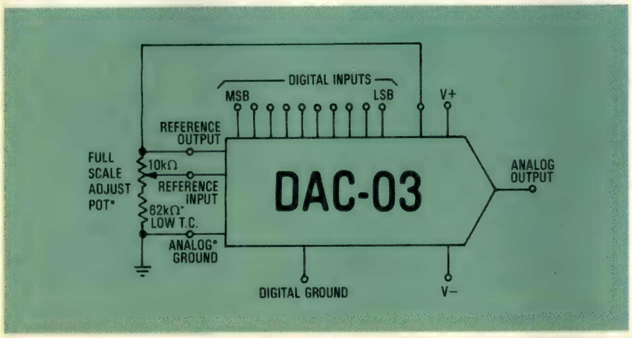
So they turned instead to in-house designs they could build with low-cost components, or to modules and hybrids which gave them the 25°C performance they wanted, but cost dearly in terms of space and power.

Was PMI going to let them go on forever making those trade-offs?

And will those same engineers go on using oversized $50 modules with a 1-watt power requirement and a speed of 5 μsec when they can get a DAC-03 in a DIP package which requires only 350mW, settles within 1.5 μsec to ½ LSB for a 10V step and costs as little as $7.95?

Even in the sometimes-backward world of Linear Wonderland that's not very likely. As Tweedledee said to Tweedledum:

"Contrariwise! If it was so, it might be; and if it were so, it would be; but as it isn't, it ain't. That's logic!"



Logic could also convince you to be one of the first to stop not needing the DAC-03. You'll quickly develop a need for the DAC-03's guaranteed monotonic performance in four non-linearity grades. We believe you'll need not only the DAC-03's speed and miserly power consumption, but also its ability to use a wide range of power sources, from ±12V to ±18V. And knowing that it's available in either + 5V or + 10V output range versions allows you to develop a need for either. Or both.

One need you'll *never* develop with the DAC-03 is additional devices for interfacing in TTL and DTL applications. Its inputs are fully TTL/DTL compatible, and only a 4¢ diode is required for full CMOS compatibility. You also won't need a big design budget since the DAC-03 is priced like a monolithic DAC, not like a module.

Sound too good to be true?

"One can't believe impossible things," Alice told the Queen.

"I daresay," replied the Queen, "that's because you haven't had much practice."

Why not practice with the impossible? Just fill in our "WHO NEEDS THE DAC-03?" coupon below and return it to us. PMI will send you a free sample so you can find out for yourself that in Linear Wonderland the best products are the ones nobody needs.

Until PMI develops them.

If someone beat you to the coupon, write to us for your sample. Or circle #200 for literature.

Part No.	100 and UP (US OEM)	Monotonicity
DAC-03DDX1 (or X2)	$ 7.95	7 bits
DAC-03CDX1 (or X2)	$ 9.95	8 bits
DAC-03BDX1 (or X2)	$14.00	9 bits
DAC-03ADX1 (or X2)	$18.00	10 bits

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Santa Clara, California 95050
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In Europe contact:
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c/o Bourns Ag
ZUGERSTRASSE 74, 6340 Baar, Switzerland
Phone: 042/33 33 33 Telex: 78722

I want to practice with the impossible and I need the DAC-03 to do it. Please send me a DAC-03 sample and data kit.

Mail to:
Precision Monolithics, Inc., 1500 Space Park Drive
Santa Clara, CA 95050

Check which type and voltage:
☐ DAC-03DDX2 (5V) or ☐ X1 (10V) ☐ DAC-03CDX2 (5V) or ☐ X1(10V)
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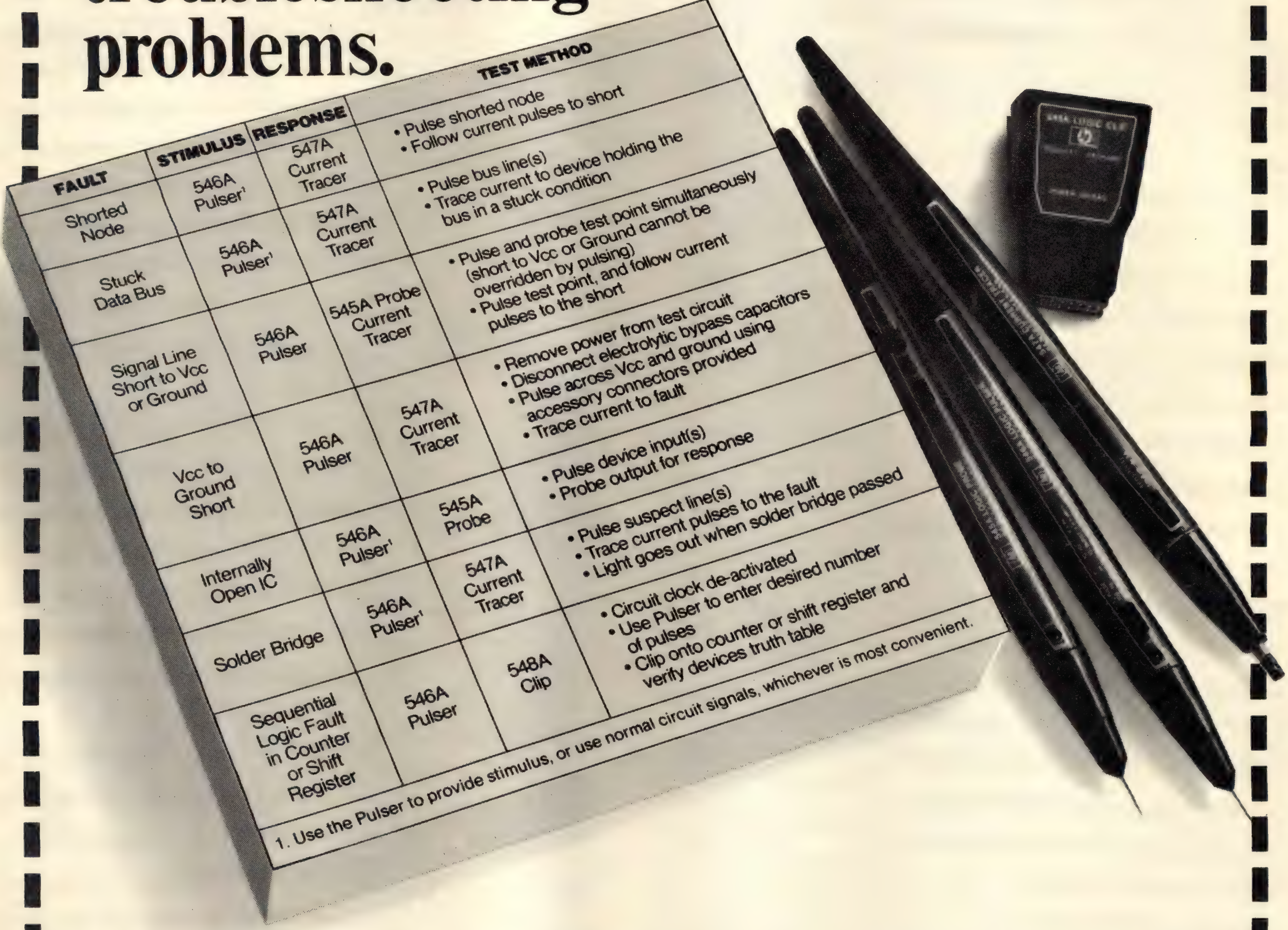

FAULT	STIMULUS	RESPONSE	TEST METHOD
Shorted Node	546A Pulser[1]	547A Current Tracer	• Pulse shorted node • Follow current pulses to short
Stuck Data Bus	546A Pulser[1]	547A Current Tracer	• Pulse bus line(s) • Trace current to device holding the bus in a stuck condition
Signal Line Short to Vcc or Ground	546A Pulser	545A Probe Current Tracer	• Pulse and probe test point simultaneously (short to Vcc or Ground cannot be overridden by pulsing) • Pulse test point, and follow current pulses to the short
Vcc to Ground Short	546A Pulser	547A Current Tracer	• Remove power from test circuit • Disconnect electrolytic bypass capacitors • Pulse across Vcc and ground using accessory connectors provided • Trace current to fault
Internally Open IC	546A Pulser[1]	545A Probe	• Pulse device input(s) • Probe output for response
Solder Bridge	546A Pulser[1]	547A Current Tracer	• Pulse suspect line(s) • Trace current pulses to the fault • Light goes out when solder bridge passed
Sequential Logic Fault in Counter or Shift Register	546A Pulser	548A Clip	• Circuit clock de-activated • Use Pulser to enter desired number of pulses • Clip onto counter or shift register and verify devices truth table

1. Use the Pulser to provide stimulus, or use normal circuit signals, whichever is most convenient.

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CIRCLE NO. 6

Letters

Can the chips do it?

I have used the March 29 Idea for Design "TV Color-Burst Crystal Generates Clock and Interrupt Signals for μP" (p. 115), in Z80A systems before. As a result, I quickly saw that a design specification was being exceeded and would have to be compensated for. The MM5369 oscillator/divider is only rated to 2 MHz at V_{DD} = 6 V (pin 8) and consequently is out of spec at V_{DD} = 5 V and f = 3.579545 MHz.

The supply voltage must be raised to 10 V where the part is rated at 4.5 MHz. Then, the output buffer at pin 7 must be a 10-V-to-TTL converter, so that the 8085/Z80A input-pin spec will not be exceeded. Likewise, a 10-V-to-TTL converter will be needed at the divide output (pin 1) in the interrupt circuitry.

Jim Norman, Design Engineer
Vital Industries
3700 N.E. 53 Ave.
Gainesville, FL 32601

Ask the chips

Jim Norman is correct in stating that the published specifications for the MM5369 programmable oscillator divider gives a maximum frequency of oscillation of 2 MHz at V_{DD} = 6 V. However, the chips themselves appear not to have read the specs, and all of them seem quite happy at 3.58 MHz and V_{DD} = 5 V.

The MM5369 is used with the crystal that is specified in several 60-Hz frequency sources. My application also makes use of the fundamental frequency. The circuit is alive and well and running. Admittedly, out of specs!

One thing I did not invent, but which exists widely, is the practice of using parts at other than rated specs. Excepting, of course, maximum dissipation. If the circuit proves convenient, reliable and inexpensive, why complain?

Ken Barbier
Borrego Engineering
P.O. Box 1253
Borrego Springs, CA 92004

Another operating system joins the majors

Your special report on microcomputer operating systems (March 15, p. 225) deserves a lot of praise. However, I was disappointed to find that our REX-80 operating system is not on your list of "major" operating systems for microcomputers.

REX-80 is a real-time operating system for 8080/8085 and Z80 microprocessor-based systems. It has been adopted by several major companies.

The primary objectives of REX-80 are to provide programming standards for the design team and engineering disciplines for the software design process.

Y.P. Chien General Manager,
Systems & Software, Inc.
2801 Finley Rd., Suite 101,
Downers Grove, IL 60515

Temperature sensors get faster yet

In "Temperature sensors get smaller to get faster" (Apr. 26, 1980, p. 250), an error was made in the package designations for the temperature sensors and their reported thermal time constants.

(continued on page 16)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

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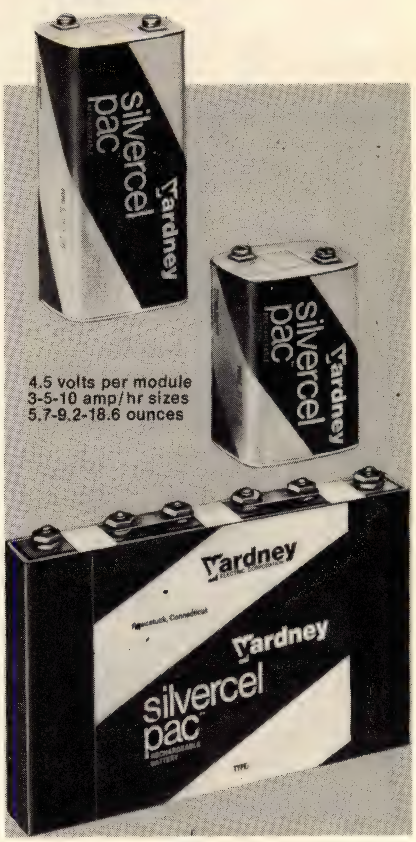

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CIRCLE NO. 7

Meetings

DATACOMM International Mini/Microcomputer, Microprocessor Exposition, June 17-19. Palais des Expositions, Geneva, Switzerland. ISCM, 222 W. Adams St., Chicago, IL 60606.

Power Electronics Specialists Conference (PESC), June 17-19. Dunfey Atlanta Hotel, Atlanta, GA. IEEE, 345 E. 47 St., New York, NY 10017.

Chicago Spring Conference on Consumer Electronics, June 18-19. Arlington Park Hilton, Arlington Heights, IL. IEEE.

International Quantum Electronics Conference, June 23-26. Sheraton-Boston Hotel, Boston, MA. IEEE.

Conference on Precision Electro-Magnetic Measurements, June 23-27. Stadthalle, City of Braunschweig, Federal Republic of Germany. IEEE.

Power Systems Monitoring and Control International Conference, June 24-26. London, England. IEEE.

Power Engineering Society Summer Meeting, July 13-18. Radisson Hotel, Minneapolis, MN. IEEE.

Nuclear and Space Radiation Effects Conference, July 15-18. Cornell Univ., Ithaca, NY. IEEE.

Quartz Crystal Conference, Aug. 12-14. Radisson Muehlebach Hotel, Kansas City, MO. K-N Enterprises, Inc., 630 S. Rogers Rd., Olathe, KS 66061.

Intersociety Energy Conversion Conference, Aug. 18-22. Olympic Hotel, Seattle, WA. IEEE.

Engineering in the Ocean Environment, Sept. 8-10. Olympic Hotel, Seattle, WA. IEEE.

International Congress on Transportation Electronics, Sept. 15-17. Hyatt Regency, Dearborn, MI. IEEE.

European Solid-State Device Research Conference, Sept. 15-18. University of York, York, England. IEEE.

Optical Communication European Conference, Sept. 15-19. University of York, York, England. IEEE.

Electromagnetic Compatibility, Conference, Sept. 15-19. University of Southampton, Southampton, England. IEEE.

International Symposium on Subscriber Loops and Services (ISSLS '80), Sept. 15-19. Bayericheoss, Munich, W. Germany. IEEE.

International Fiber Optics and Communications Exposition, Sept. 16-18. Hyatt Regency, San Francisco, CA. Information Gatekeepers, Inc., 167 Corey Rd., Suite 111, Brookline, MA 02146.

Western Electronic Show and Convention (WESCON), Sept. 16-18. Anaheim Convention Center, Anaheim, CA. IEEE.

Broadcast Symposium, Sept. 17-19. The Washington Hotel, Washington, DC. IEEE.

International Broadcasting Convention, Sept. 20-24. Metropole Conference Center, Brighton, England. IEEE.

Compcon Fall '80, Sept. 23-25. Capitol Hilton, Washington, DC. IEEE.

European Conference on Optical Systems and Applications, Sept. 23-25. Utrecht, The Netherlands. IEEE.

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CIRCLE NO. 8

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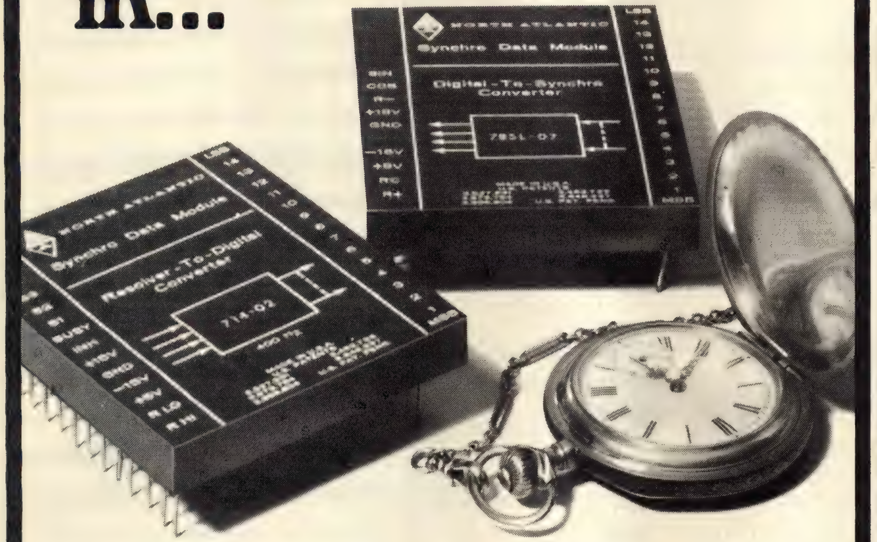

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CIRCLE NO. 9

Letters

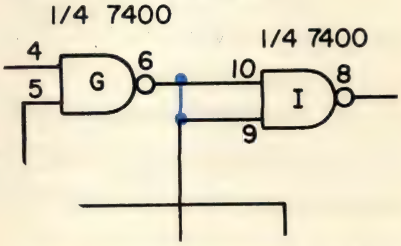
(continued from page 13)

The older TSP102 is housed in the TO-92 package and exhibits thermal time constants of 4.3 s in oil and 30 s in still air. The newly introduced, miniature packaged TSF102 (tabbed package) and TSU102 (untabbed package) exhibit thermal time constants of 0.20 s and 0.25 s in water; 2.5 s and 4.0 s in moving air; and 8.0 s and 10.0 s in still air, respectively.

Wayne Tarpley, Sensor Development Manager,
Electronic Devices Div.
Texas Instruments, Inc.,
13500 N. Central Expwy.
Dallas, TX 75222

Glitch catcher gets caught with a glitch

Irving Simon's glitch-catcher design (Dec. 6, 1979, p. 124) has an error in the schematic. The latch formed by gates G and H was incorrectly drawn. The correction is as follows:



Mr. Simon mentioned catching glitches in the 100-ns region. This figure may have come from the Texas Instruments' TTL Data Book, which states that the 74123 has an output pulse width of > 100-ns duration ($R_{ext} = 5\ \mathrm{k}\Omega$. $C_{ext} = 100$ pF). However, when I converted the design to a PC card, I could not trigger on glitches less than 260 ns, which meant that the design could not distinguish between glitches and normal signals on now-standard 2 and 4-MHz microprocessor systems.

Fred Seelig
Satcom Modems Section
Government Communications Systems Div.
Harris Corp.
Melbourne, FL 32901

Here's the state of the art in low-cost hard-disk computers

11 MEGABYTES OF FAST HARD-DISK STORAGE

Yes, the Cromemco Model Z-2H is in a class by itself in the computer field.

These Z-2H features tell you why:

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And more all the time.

FIELD PROVEN

The Z-2H is clearly in a class by itself. We introduced it last summer. It's field proven. It's reliable.

And it's rugged. Housed in a sturdy, all-metal cabinet.

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As always with Cromemco, you get expandability. The fast 64K RAM in this Model Z-2H can be expanded to 512 kilobytes. That amount of RAM combined with 11 megabytes of hard-disk storage gives you enormous computer power—the equal or even beyond what much larger computers sometimes offer.

What's more, this computer gives you a 12-slot card cage. That's to plug in your special circuits as well as additional RAM and interface cards.

This expandability is supported by still more Cromemco value — the Z-2H's heavy-duty power supply that gives you 30A at 8V and 15A at ±18V to support plug-ins.

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CIRCLE NO. 10

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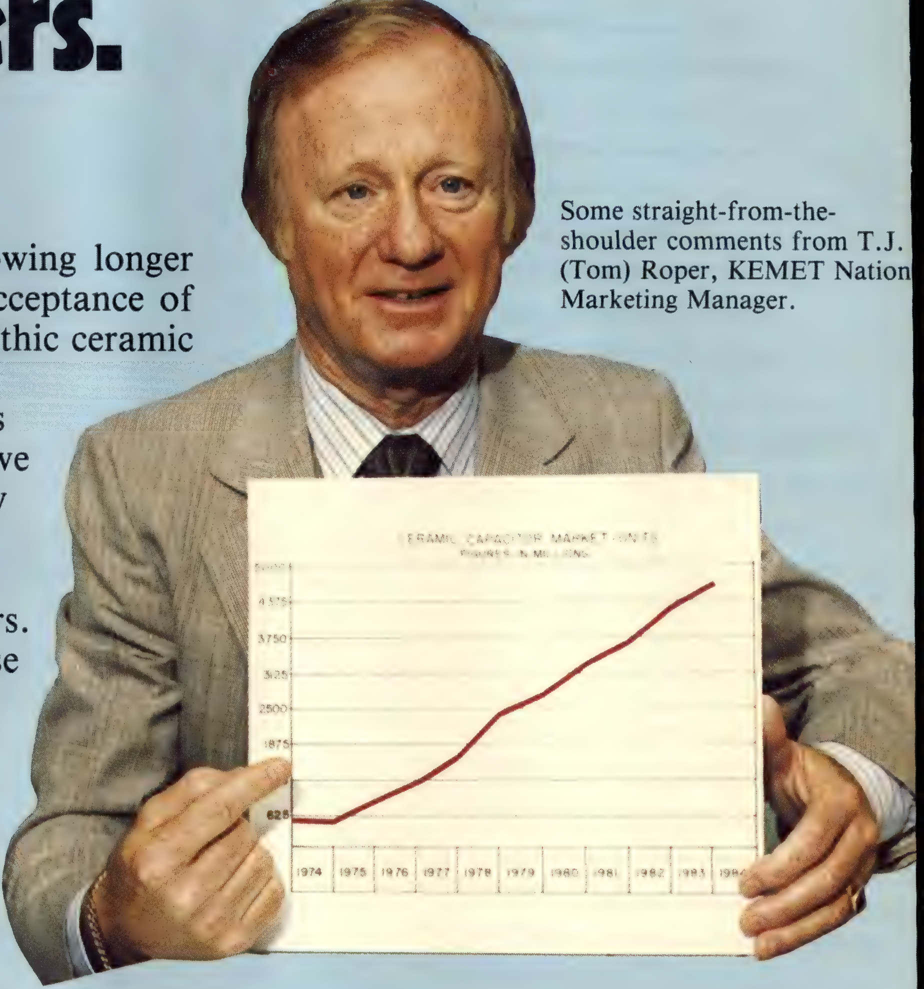
Our list of customers is growing longer every day, thanks to your acceptance of KEMET quality-built monolithic ceramic capacitors.

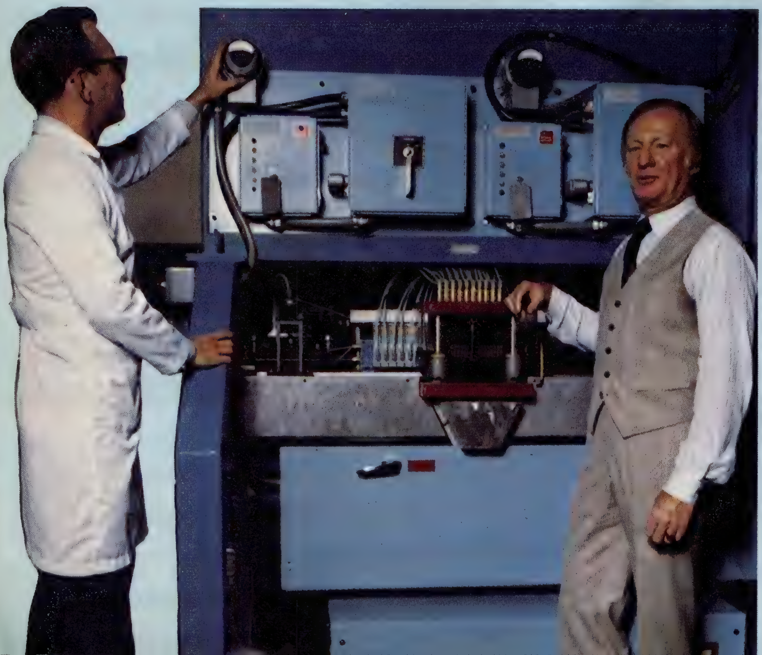
Fact: Our sales volume has grown 50% per year—since we entered this dynamic industry in 1968.

This growth has provided great things for our customers. It has permitted us to increase our production facilities and quality assurance programs immensely. So KEMET customers can continue to take our quality and availability for granted.



Some straight-from-the-shoulder comments from T.J. (Tom) Roper, KEMET Nation Marketing Manager.

The only way we can get the machines we need is to build 'em.

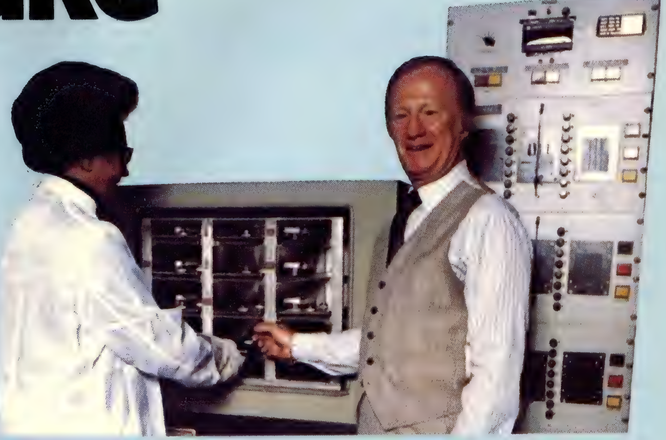


No other manufacturer takes greater care in the manufacture of monolithic ceramic capacitors than KEMET. Because no other manufacturer has more extensive Research and Development facilities and unique manufacturing methods than Union Carbide. More than 70 staff equipment designers, engineers, chemists, draftsmen, technicians and machinists work full-time to keep KEMET out front. With computer controlled testers, ceramic sheet casters, laminators and dozens of other ingenious innovations.

Quality is built in, not inspected in.

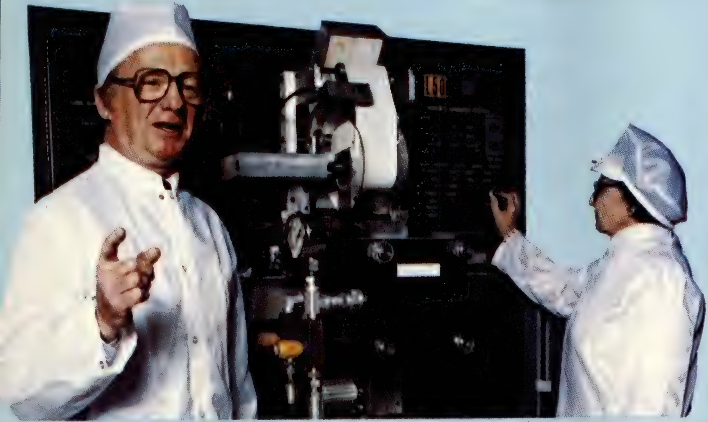
Every step of production ends with an in-process quality control inspection. You never see the products that don't make the grade. If they fail our rigid tests, they fail. Period. Our testing procedures put greater stress upon the capacitors than they will probably ever see in actual circuit application.

eople who take or granted.



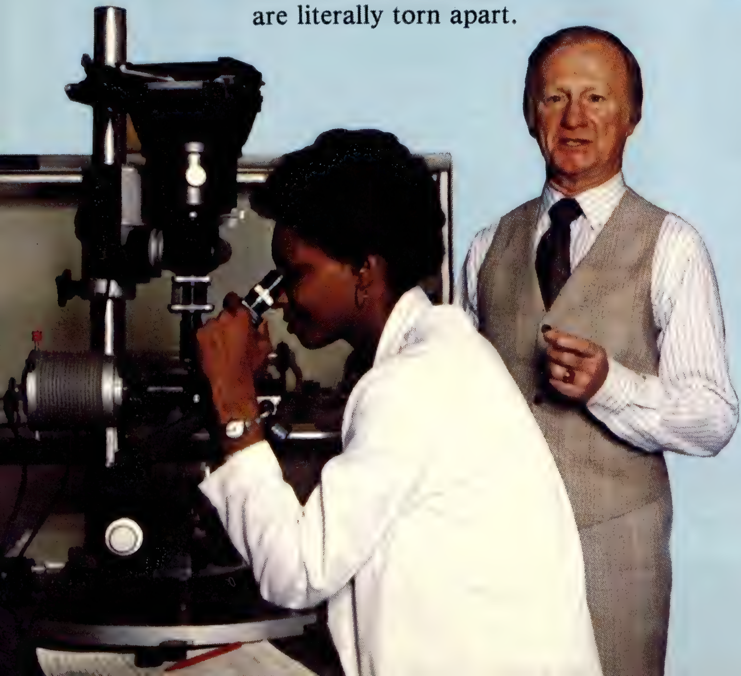
At KEMET, we take reliability very seriously.

This multi-million dollar, Federal Class 100 clean room is where KEMET High-Reliability ceramic capacitors are born. This "plant within a plant" is totally isolated from other production areas, is operated by its own support group and is completely equipped with its own technically advanced processes and equipment. This specialized facility is your assurance that KEMET High-Reliability ceramic capacitors are specifically built to meet or exceed **MILITARY requirements.**



With KEMET High-Reliability ceramic capacitors, customers get a "life" history.

KEMET customers get only the best when they order High-Reliability ceramic chips or molded radial or axial leaded capacitors – we back these products with performance data and destructive physical analysis (DPA) results. Each capacitor undergoes in-process testing and ultrasonic scanning to detect voids and delaminations. The proof of quality is demonstrated in the DPA lab, where samples are literally torn apart.



Here, the good parts get burned-in; the rejects just get burned.

Every KEMET ceramic capacitor undergoes in-process testing at each production operation, plus stringent final quality control inspection. But that's not enough for us. All Military grade products are subjected to 100-hour burn-in at 125°C. Only the strong survive and earn the KEMET brand name – and get shipped to our customers.

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For more data, write to Electronics Division, Union Carbide Corporation, Box 5928, Greenville SC 29606. Phone: (803) 963-6300; TWX: 810-287-2536; Telex: 57-0496. Or see your local KEMET representative.

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CIRCLE NO. 11

Catch the fastest C-meter in its price class...the autoranging 830

It's happened again. B&K-PRECISION was the first company to offer a really cost-effective lab-quality C-meter. Now we've done the same for autoranging. The new Model 830 autoranging capacitance meter is fast, accurate and built with famous B&K-PRECISION dependability.

The 830 offers features that are tough to match at any price, such as 0.1 pF resolution, large 3½ digit LCD display and fuse protection against charged capacitors. Basic accuracy is 0.2%, much greater than the tolerance of most capacitors.

Ease of operation is another strong suit for the 830. On the production line, even untrained workers can be quickly instructed on proper operation, making the 830 ideal for component sorting and selection. If capacitors to be measured are limited to a narrow value range, the "range hold" capability of the 830 can freeze it onto one range—an added time saver. This feature, along with the fast reading time of the instrument, makes the 830 especially valuable for incoming inspection applications. On the engineering bench, the 830 is an excellent means of pre-testing critical capacitors.

For applications suited to manual ranging, B&K-PRECISION offers the 820 at an even lower cost. In fact, for the cost of some autoranging units, you could almost purchase both the 820 and 830! The 820 also provides 0.1 pF resolution. With full 4-digit LED display, readings extend to 1 Farad.

With either B&K-PRECISION C-meter, you can measure unmarked capacitors . . . verify capacitor tolerance . . . measure cable capacitance . . . select and match capacitors for critical circuit applications . . . sample components for quality assurance . . . measure complex series-parallel capacitor networks . . . accurately set trimmer capacitors . . . check capacitance in switches and other components. Both instruments have front-panel lead insertion jacks for fast in-out testing.

For details contact B&K-PRECISION or your local distributor:
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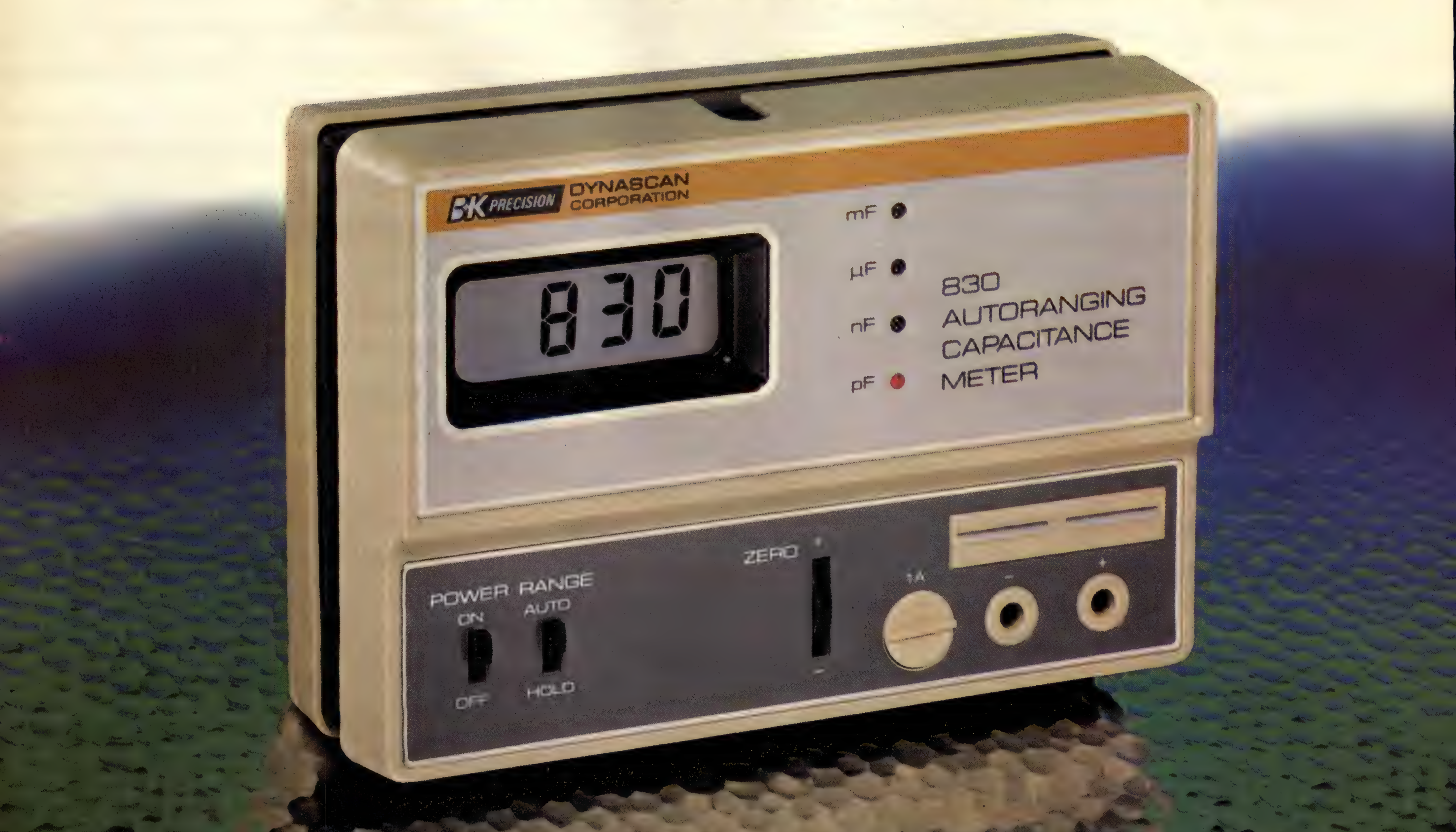

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FREE DEMONSTRATION CIRCLE NO. 12

ADDITIONAL INFORMATION CIRCLE NO. 13

LateNews

LCD controller, 4-bit μC on one chip

Almost ready for sampling, a single chip from NEC Microcomputers carries a 4-bit CMOS microcomputer and a programmable liquid crystal display controller. The Wellesley, MA, company will also offer a ROM-less intelligent LCD controller for more general-purpose applications. Both the μC-based μPD-7502G and the ROM-less μPD-7225G will come in space-saving flat packages. The 7502 package has 64 leads (12 each on two sides and 20 each on the other two), and the 7225 has 52 leads (13 on a side).

The stand-alone 7502 controller/microcomputer offers 97 instructions. With 2048 bytes of ROM, 128 nibbles of RAM and four independent display registers, it can drive four backplane lines and 24 segment lines, one 4-bit input port, one 4-bit output port, and three 4-bit I/O ports. It operates with a 15-μs instruction cycle.

Externally programmable, the 7225 controller has two on-chip 32-byte RAMs. One is a normal data RAM. The other stores data that will be highlighted by a blinking display. The controller has a repertoire of 19 commands, while the display drive section drives up to 32 segment outputs. An on-chip decoder handles 7 and 14-segment displays.

DIP holds entire data acquisition system

A complete hybrid 12-bit data acquisition system in a double-wide 40-pin ceramic DIP package will soon be announced by Micro Networks (Worcester, MA). The linearity at 25 C is typically ±¼-LSB. The MN7140 is among the few hybrid data acquisition systems qualified for hi-rel environments and −55 to +125 C according to MIL-STD-883B. The system includes an eight-channel input multiplexer, instrumentation amplifier, track-and-hold amplifier and successive approximation a/d converter. The acquisition time for a 20-V step input is less than 10 μs. The a/d conversion time is within 50 μs, and overall system throughput is better than 20 kHz.

796-bus standard—ready for comments

The IEEE Task P796 Microcomputer System Bus Group Workshop has issued a proposed standard for the 796 bus, which is based on Intel's Multibus. The bus itself is continuing to evolve, with several revisions still being considered, according to group chairman Richard W. Boberg (Microbar Systems Inc., Palo Alto, CA). These include four more address lines, to bring the total to 24 for 16-Mbyte addressability; compliance levels that will allow products to implement well-defined subsets of the bus standard; and additional edge connectors and board sizes. National Semiconductor and Advanced Microcomputers, among other companies, have supported the standardization effort, says Boberg, while Intel has designated its own 796-bus specialist, Gary Fieland, at its Aloha, OR facility.

Custom logic comes in three technologies

A custom logic design process that results in no unused gates or left-over areas is moving into the general market; it had been reserved by the developer, Signetics (Sunnyvale, CA), for certain specialized customers. Aimed at arrays of 500 gates or less, the Composite Cell Logic process draws on a library of SSI and, eventually, MSI functions and interconnects them on a computer before diffusions and metal depositions are made.

Three semiconductor technologies can be implemented in a CCL array: Low Threshold Logic, with typical gate delays of 3 ns for a low power version and 2.5 ns for a version with slightly higher power; Integrated Schottky Logic, with typical delays of about 4 ns/gate; and Extended Performance Logic, with typical delays of 3 ns for low-power versions and 2 ns for high-power. From the time the circuit is designed and layout is ready to begin, the turnaround is about 11 weeks to first samples. Chips cost from a few dollars to about $25, excluding the nonrecurring cost of mask generation (about $24,000 to $37,000).

Amplifier speeds up for data acquisition

Data acquisition circuits will be able to count on a sample-hold amplifier from Teledyne Philbrick (Dedham, MA) for a 1-μs acquisition time, 0.002% nonlinearity and a 5-MHz bandwidth. The 24-pin hybrid TP4857 will respond to logic signals by either reproducing the input signal at the output or holding the input signal indefinitely. The decay rate and system gain can be externally trimmed. The company also is using ceramic packaging to save up to 20% of the cost of metal packaging in a line of v/f converters. The −70 versions of the 4731, 4733, and 4735 converters convert input voltages ranging from ±10 μV to ±20 V into TTL pulses with 10-kHz, 100 kHz and 1-MHz full-scale outputs.

Ceramic-chip capacitors to come in every EIA size

While no rapid automatic-insertion equipment for chip components has been announced yet, many manufacturers anticipate that this equipment, once available, will encourage the use of discrete components in chip form—for example, ceramic-chip capacitors. Anticipating this, manufacturers like AVX Ceramics (Myrtle Beach, SC) and Murata (Marietta, GA) will soon be supplying chips in EIA standard sizes ranging from No. 0805 through No. 1505 (including the controversial No. 1206). They will come on 8-mm punched tape and disposable reels intended to facilitate rapid automatic insertion.

Fiber-optic link doubles trunking rates

Data rates for fiber-optic trunking have been doubled from the usual 45-Mbit/s T-3 rate to 90 Mbits/s (T-3C) in Central Telephone Co.'s 8.57-km link between central offices near Humble, TX. Terminals from NEC America (Melville, NY) multiplex two 45-Mbit/s streams into a 90-Mbit/s aggregate for optical transmission by a near-infrared diode laser and detection by APD-based receivers.

Even more traffic could be accommodated by wavelength-division multiplexing of the optical signals through the double-window fibers in the link's cable, which is made by Valtec (West Boyleston, MA). The double-window fibers offer low dispersion and attenuation in near and far infra-red regions: 3.5 dB/km at 830 nm and less than 2 dB/km at 1200 nm.

Late Briefs

A $2000 rechargeable battery-backup unit that will keep power going to the CPU and memory for up to two minutes during temporary ac power failures is being added by Data General Corp. for its top-of-the-line Eclipse S/250, C/350 and M/600 minicomputers. For extended ac failures, the Westboro, MA company has enhanced its Advanced Operating System (AOS) software not only to provide an orderly processing shutdown but also to permit the computer to resume processing, with minimal operator intervention, once ac power is restored...... **A dual version of the micropower OP-20 amplifier, the OP-220, will draw as little as 85 μA from a single-supply voltage of 3 to 30 V.** On the way from Precision Monolithics Inc. (Santa Clara, CA), the OP-220 has an input offset voltage as small as 100 μV, input bias current of approximately 20 nA, and voltage gain of approximately 1000 V/mV. The OP-220 is also pin-compatible with the LM158 and 747 dual op amps.

MEM-EBAUCHES and Xicor, Inc. announce a joint international effort in semiconductor products.

X2201 FABRICATION FACILITIES

MEM-Ebauches Electroniques SA of Switzerland, a world leader in electronic time pieces, and Xicor, Inc., a new California semiconductor firm are engaged in a joint effort producing microprocessor-related products.

The initial products are nonvolatile semiconductor memories with unprecedented ease-of-use features.

MEM-EBAUCHES announces a breakthrough

NONVOLATILE 5V STATIC RAMS

MEM's X2201 and X2202 are the first easy-to-use nonvolatile 5V only static RAMs. They open up exciting new product opportunities.

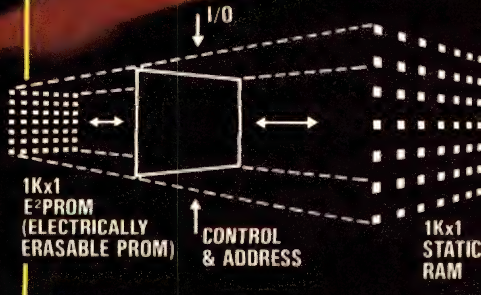
POWER-FAILURE PROTECTION: One simple TTL signal saves your entire RAM database! A snapshot nonvolatile copy of all RAM data s internally stored safe without power and will reappear automatically in the RAM when power returns—ready to use. No battery backup needed!

NONVOLATILE PROGRAM STORE: The X2201 and X2202 each contain 2K bits of memory organized as a conventional 1K static RAM overlaid bit-for-bit with a nonvolatile 1K Electrically Erasable PROM (E^2PROM). You can store a nonvolatile bootstrap program in the E^2PROM and at the same time access an independent program in the RAM memory. At any time, data can be transferred back and forth between the RAM and E^2PROM by simple store and ecall signals.

5V ONLY: You will never need high voltage pulses or supplies. A single 5V supply is the only power source ever required for any function!

EASE-OF-USE: Unprecedented simplicity. All inputs and outputs are directly TTL compatible. Fully static timing.

PERFORMANCE: RAM cycle time is less than 250ns. During operation, data can be recalled from the E^2PROM an unlimited number of times.



MEM's X2201 and X2202 are fabricated with reliable n-channel floating gate MOS technology. For systems where RAM nonvolatility or *in-the-circuit* ROM changes by TTL signals are important, the MEM X2201 *(array recall)* and X2202 *(bit recall)* are the only choice!

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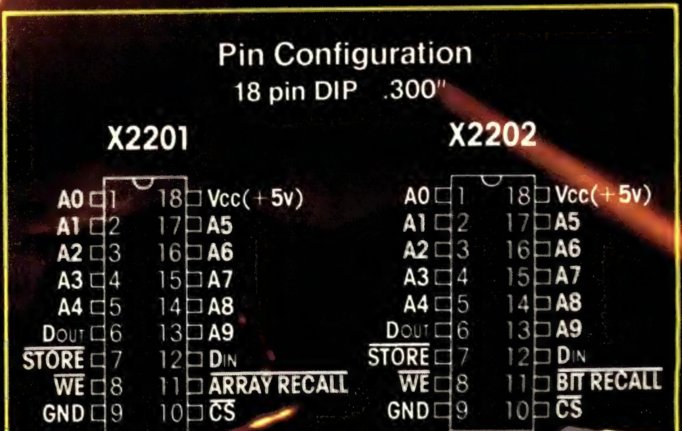
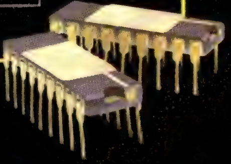
Applications

- Power-failure and crash protection
- Microprocessor systems
- Field-programmable control modules
- Instruments
- Nonvolatile electrical meters
- Cash registers and smart terminals
- Portable nonvolatile electronic databases
- Remotely codable security systems
- Electronic office equipment
- Consumer products
- Replacement of EPROM in applications where unsocketing, uv light data erasure and high-voltage programming are undesirable.





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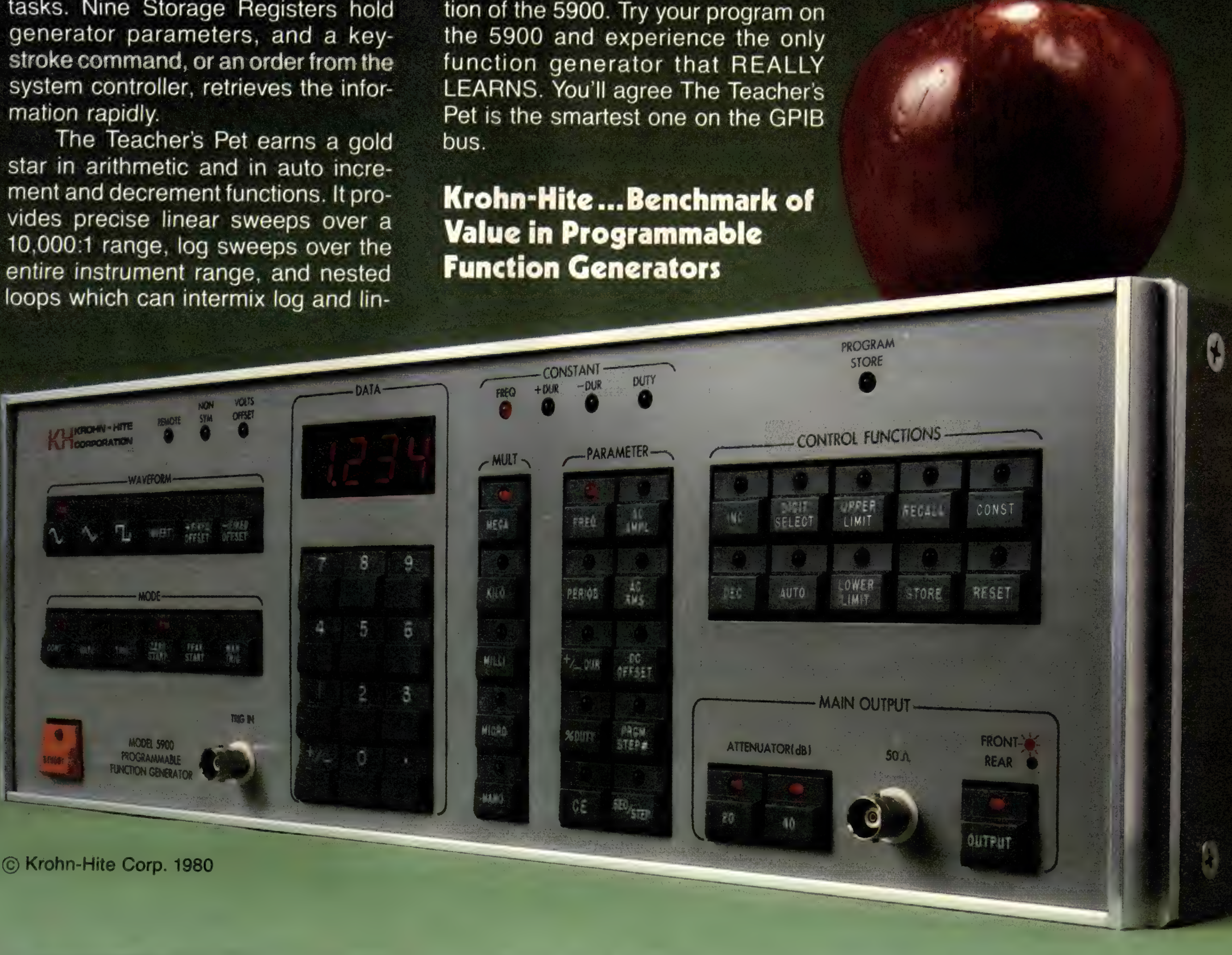

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CIRCLE NO. 15

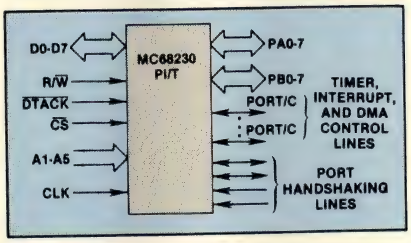
Six news chips provide the I/O and other support needed to deliver the powerful performance promised by the MC68000.

Support chips bring out the MC68000's best

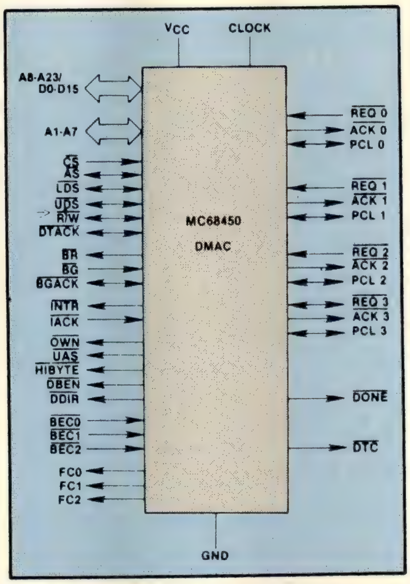
Powerful 16-bit microprocessors like the MC68000 stand ready to help system designers build complex μP systems that can work like yesterday's minicomputers. Now, an entire new generation of 16-bit support circuits from Motorola (Austin, TX) stands ready to get the most out of such powerful CPUs. Though the MC68000 was designed to work with the older MC6800 family of support circuits, pairing the 16-bit CPU with support chips originally designed for 8-bit μPs would prove inadequate for 16-bit systems.

The new crop of support provides all the necessary I/O and other functional help. The chips include the MC68120 intelligent peripheral controller, the MC68230 combination parallel interface and timer circuit, the MC68450 direct-memory-access controller, the MC68451 memory-management unit, the MC68340 dual-port RAM and the MC68560 serial DMA interface.

The MC68120, described at the recent Electro/80, features an enhanced MC6801-μC architecture. The chip includes semaphore registers and a dual-port RAM to permit the μC to be used in multiprogramming applications. The MC68230 (Fig. 1) can operate interrupt-driven, DMA-driven or polled, and can be set up so that the 16 I/O lines function as two unidirectional 8-bit ports, two bidirectional 8-bit ports, one 16-bit unidirectional port, or one 16-bit bidirectional port. The timer subsystem also offers a choice of operating modes, thus permitting either periodic interrupts or a timeout interrupt output signal.



1. The MC68230 combination parallel interface and timer circuit offers versatile I/O operations.



2. The MC68450 DMA controller comes in a 64-pin package and offers a 16-Mbyte addressing range.

Housed in a 48-pin package, the 68230 takes advantage of the CPU's asynchronous bus, MOVEP and RESET instructions, and vectored interrupt capabilities.

Four independent DMA channels are provided by the MC68450 DMA controller (Fig. 2), which will come in a 64-pin package and provide a 16-Mbyte addressing range to take full advantage of the CPU bus. Capabilities include memory-to-memory or memory-and-device block transfers; multiple data-chaining modes; byte, word and long-word modes; two interrupt vectors per channel.

Moving memory resources

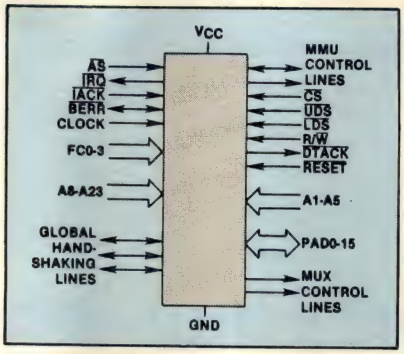
Working hand in hand with the 68000 and the 68450, the MC68451 memory-management unit (Fig. 3) will provide flexible and efficient allocation of memory resources during task execution. It's also expected to be housed in a 64-pin package.

Besides supporting many independent tasks that can share access to common resources, the 68451 provides protection from unauthorized or unintentional access to data or other memory resources, detects obviously incorrect use of memory by an executing task, separates users from system functions, and provides translation and protection for use with DMA operations. In addition, management features include the support of virtual memory, write protection for selected areas of memory, bus-error detection, quick context changes, address translation to simplify programming models of address space, and a simple, compact description of the segments.

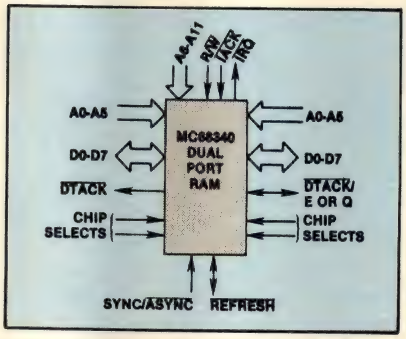
To help share resources, the MC68340 dual-port RAM (Fig. 4) will provide a 2-k × 8 storage area suitable for CRT refresh memories, multiprocessor communications, parallel I/O and disk interfaces. Housed in a 48-pin package, the RAM will be bus-compatible with both the 6800 and 68000 CPUs, and multiple 68340s can be used to expand the dual port memory to any depth or width.

The RAM is pseudostatic, using dynamic RAM cells and internal refresh controls. Also contained in the RAM is logic for generating up to 16 interrupt vectors, and for handling up to 16 semaphores for multiprocessor interfaces. Interrupt modes include priority, round robin, and FIFO.

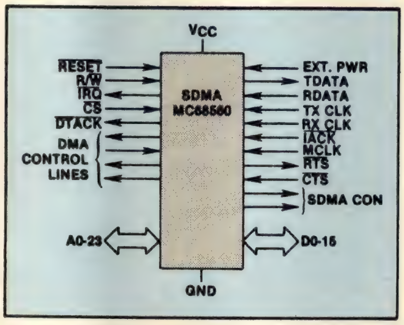
To provide a serial-DMA interface, the MC68560 (Fig. 5) offers both the 24-bit address bus and 16-bit data bus for full 68000 compatibility. It also uses NRZ data and contains internal byte synchronization. However, both external clocks and external data recovery are required. What's more, communicating via a subset of the SDLC protocol with either half or full-duplex operation, the circuit permits DMA command-chaining capabilities, and offers point-to-point, multidrop, and loop modes.



3. The MC68451 memory-management unit, also housed in a 64-pin package, supports multiple independent tasks.



4. The MC68340 dual-port RAM provides a 2-k × 8 storage area and acts as a pseudostatic RAM.



5. The MC68560 serial DMA interface offers both a 24-bit address bus and a 16-bit data bus.

Additional support circuits are being defined for introduction in 1981 and 1982. Some of these include a cluster-terminal controller (MC68122), an advanced CRT controller, a bubble-memory controller, a hard-disk controller (MC68454), a general-protocol serial-I/O controller (MC68561), a USART, a multiprocessor interface unit, a memory error-correction circuit (MC68540), and a floating-point math ROM (MC68341) with position-independent code.

Not only that, but Motorola has also developed some new support for its 6809 microprocessor, notably the MC6829 memory-management unit and the MCM6839 floating-point ROM. The 6829 comes in a 40-pin package and permits the 6809 to expand its memory space from 64 kbytes to 2 Mbytes in 2-kbyte pages. It also permits up to 32 independent tasks and contains programmable mapping registers, override controls and access-protection bits.

The floating-point ROM will provide position-independent code that enables the 6809 to perform scientific calculations in single-precision, double-precision and double-extended-precision formats compatible with the IEEE Draft 5 floating-point standard. The software uses no absolute RAM, thus making the programs totally reentrant. And operands are either in registers or in the stack (Pascal style). Software operations include addition, subtraction, multiplication, division (with remainder), square root, compairsons (any precision), converting between integer and floating point, and binary-to-decimal conversion.

Dave Bursky

Compatibility—the key to board computers

Having witnessed an explosion over the last few years of diverse architectures, buses and interfaces from board-level computer makers, Gordon M. Watson thinks it's time to change the strategy. The biggest challenge for the board-level producer is to provide a family of products across the price/performance spectrum that have software, bus and packaging compatibility, according to the vice president and general manager of Computer Automation's Naked Mini division. Pointing out that mainframe makers have used compatibility to a definite advantage over the years, retaining customer base through hardware interchange and software portability, Watson suggests that now is the time for board-level makers to do the same:

"The mini and microcomputer companies proliferate architectures at an alarming rate to get position in their little niches, but what they don't realize is that they create tremendous migration problems for people."

One group that figures to applaud such compatibility will be the OEMs, who are looking to expand into market segments closest to their successful products. But if doing that means a new architecture, a new bus or a new software program, they'll forget about it, says Watson. The key is to expand vertically without having to start from scratch.

Pointing to his own suppliers, the chip manufacturers, Watson does not see much reason for them to go heavy on speed or versatility improvements.

"I don't see any major technology displacement occurring in the next two or three years," says Watson. "The things that appeal to me are low power and nonvolatility. With low power, you just save all along the road. The whole issue of volatility is really a tough system issue today. We're getting more and more memory for less and less, but we don't have the ability to keep it alive."

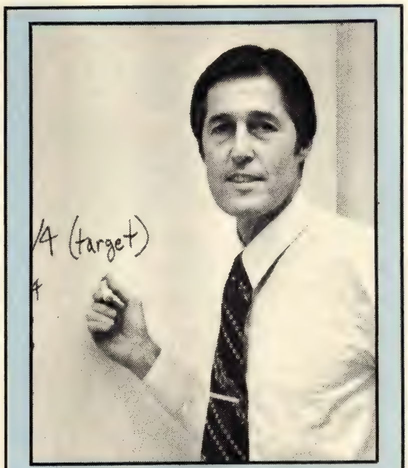
And as for speed:

"We don't need any tremendous speed improvements. I'm willing to accept speed improvements through improved chip geometries, clever implementations, and the building of hierarchies of memories within computers: These are much better ways of beating the speed race than just raw ECL."

In fact, Watson notes, a look at the speed curves will show that the big speed race is over, having flattened out in the 150 to 300-ns region. "It just isn't worth it to try and get the basic engine much faster when you can do so much more through hierarchies," Watson explains.

For that matter, quite a bit more can—and should be—done in the area of packaging, especially in what Watson calls the "carcass"—the sheet metal, connectors, backplanes, power distribution and so forth.

"The attention toward packaging, I think, has always been much less than it should be," Watson believes. "Much of the reliability of a system—manufacturability, maintainability, cost—is tied up in the package. I see a higher emphasis on packaging in the 1980s as the electronics shrink in their contribution to the cost line. I also see an emphasis on packaging because of the opportunities to integrate computers into the terminal."



Gordon M. Watson has been active in programming and computing electronics for over 20 years. Since receiving a BSEE from UCLA in 1963, Watson has taught and designed computer software for both military and commercial applications, and has spent a good deal of the past two decades in upper management.

He came to Computer Automation from TRW Electronics where he had been the principal technical contributor working on new business ventures. He also spent two years at TRW as technical director for hardware and software development of retail-credit and point-of-sale systems.

Before that, he spent seven years at Varian Data Machines (now Sperry-Univac Minicomputer Operations), where he became vice president of engineering and was responsible for all hardware, firmware and software development, including the V77 family of 16-bit minis.

Having been a part of TRW's point-of-sale development, Watson is keen on finding ways of getting computing power under the finger tips. In fact, his goal at Computer Automation is to build a multiuser operating system right in the terminal. So getting a megabyte of memory under the keyboard is very appealing to him.

"In the 1980s computers will move closer and closer to the user. If the user is putting a specimen into a centrifuge to analyze it—setting type, dispensing cash, or whatever—the computer will have to fit into that envelope," according to Watson.

Getting real-time response out of computing is not the only reason for proximity to the user, Watson says. When the cost of transporting comes down—no modems, line charges, cables, interfaces, etc.—reliability goes up.

"People that can develop their computer in a well-packaged configuration that is flexible, low-cost, reliable and cool will have a good market in the 1980s," Watson states.

Now, failures run about 50-50 between packaging and components, but he expects reliability to go up as component counts decrease. Long-term problems, then, will be packaging related.

Another strong area of interest for Watson, and backed up by a sizable chunk of Computer Automation capital, is software development. Watson brings more than interest to this concern, being one of the few top-level managers to come essentially through programming ranks. So it's more than theory when he says that one of the ways to better address the user is to provide a variety of languages that emit good code for "small" machines—this means small address space or small program space. Another way is to provide languages that can be mixed and matched when it is desirable to link up modules in different languages.

"Some of the more elegant languages that are available for small machines today require a large amount of support code at run time to allow execution," Watson notes. "In many cases, that eliminates the possibility of using that language in the application, because you're reselling it thousands of times and you may have to throw in an extra 16 k of memory—so it's cost prohibitive."

Language barriers still

Indeed some languages that fit the hardware don't fit the sophisticated applications. As far as the quality of high-level languages for small computers is concerned, Watson is critical.

"There's a lot more talk than action today in terms of these high-level languages. I remember back in the early 1960s when we put Algol on the Bendix G-15 computer that had 2 k of memory. We proved it could be done, technically, but it was almost worthless as a product. I still see some of that going on today with these small machines.

"I think the vendors have yet to demonstrate they can really deliver good, high-level languages that are optimized for these small machines. To solve the problem, it will take a real vendor commitment. The technology's there. It's deciding how to fracture the language to the point where there's enough left to be useful, yet subsetted down to where you have a chance of fitting it in."

Watson believes that all the languages should have compatible interfaces so that the user can mix and match languages to optimize his application. However, a proliferation of languages is again underway, which could run counter to the standardizing efforts of the past two decades.

"We got a Fortran standard out in 1966, and the vendors ignored it," Watson recalls. "They all built standard compilers with extensions, so they basically dug the moat, filled it with alligators, and then invited their users to walk across. Any user who has done any kind of high-level programming and tried to port it across different systems has realized that compatibility's a state of mind."

While he believes that standardizing efforts have helped, Watson believes that languages that are more application-oriented are still needed. And structured languages are needed to produce correct code that is easily understood and has a longer life cycle. This will take the acceptance of several languages, which can be easily interchanged.

"I see a trend in the 1980s toward correctness—program reliability, validation. And that will be attacked through documentation, through utilities that assist in validating and debugging languages," Watson predicts.

"It's interesting to note that if one were to write a Fortran program today on most computers, particularly the small ones, and then attempt to debug the program, it would be done almost the same way I did it 22 years ago," Watson muses. "So, we've made very little progress in the area of program verification."

One of the key problems for an essentially noncomputer-oriented OEM is measuring the productivity of his programming effort. Watson sees programming productivity as one of his rarest resources—hard to get, hard to keep, hard to understand, hard to measure, hard to estimate—"and with very few standards," Watson adds. This gives the vendor an opportunity to deliver systems that are instrumented so that the OEM can get some metrics on his programming staff—for example, the number of compiles required to get from the first program to the released version, what failures occurred and in what areas. This documentation could indicate areas of training needed, individual productivity and so forth, which would all lead to getting software up while the machine is being developed.

"Building a home-grown computer in the 1980s is one of the most unsound business decisions a company could make," Watson states unequivocally, "and I will argue that on the basis of any numbers they want to show."

Ron Shinn

Math package for μCs does algebra, calculus

An interpreter and several math modules, packaged together, can manipulate algebraic equations on a small computer, as effectively as a mini or mainframe. Created by Al Rich of Soft Warehouse (Honolulu, HI) and distributed exclusively through Microsoft (Bellevue, WA), the muSIMP/muMATH-79 works with computers like the RTS-80/1, with 32 k of memory, for as little as $75. An upcoming CP/M version, requiring 64 kbytes of RAM, will take on differentiation, integration and matrix operations at $250.

muSIMP (μC structured implementation language) is an interpreter written in a LISP-like language for 8080 and Z80-based systems. It must be present at

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all times. However, because of the modular tree-like structure of muMATH, only the muMATH module under use and those modules linking it to muSIMP need to be in memory (see Figure). For instance, the two trigonometry modules require the assistance of just the elementary algebra and rational arithmetic modules and muSIMP.

The math package is easy to set up since it comes with an interactive tutorial program. After some work with the basic arithmetic functions, the user learns from the rational arithmetic module how to use numbers with any radix from 2 to 36. Radix 16 (hexadecimal) uses numbers 0 to 9 and letters 0A to 0F (the leading zero prevents confusion with literals).

The real fun begins with the elementary algebra module, for operations with unbounded variables (those that have no assigned values). The program will expand products, when desirable; for instance, to simplify the expression:

$$(x+1)^2 - x^2 - 2x - 1.$$

This comes out to zero, regardless of the value for x. The program also handles complex roots, extracts numerators and denominators, performs logical operations on strings and undertakes several other jobs.

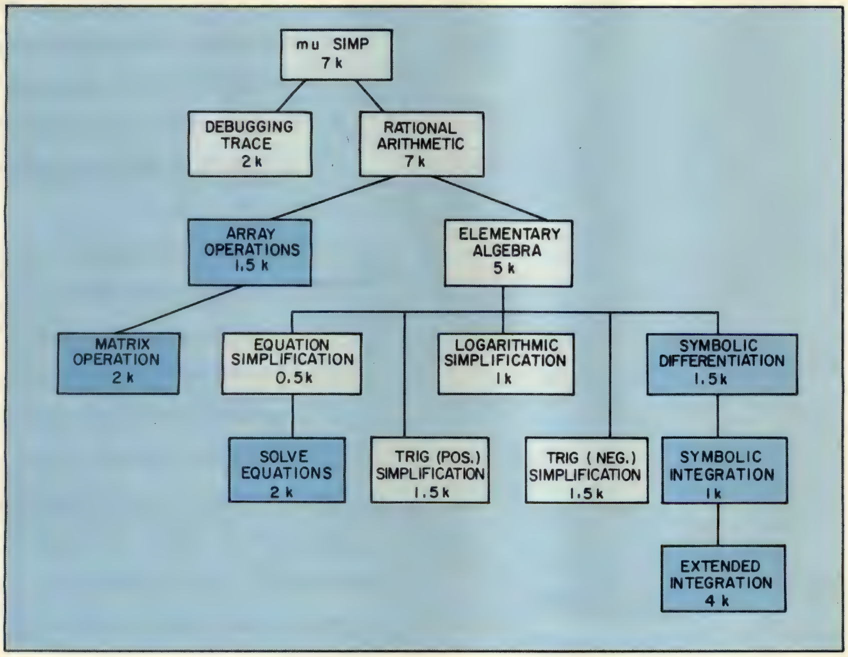
The solve-equations module returns solutions like:

$$\ln(\arctan(x-1))=b, \text{ namely } x = 1 + \tan e^b.$$

Or, if several solutions exist, as for $x^2 = 4a$, they are listed in sequence:

$$x = 2a^{1/2}$$
$$x = -2a^{1/2}.$$

Even simultaneous linear equations can be solved if the matrix operation module is loaded.



Hierarchy of muSIMP/muMATH 79: To run any module, only those other modules must be in the computer that form a complete branch to muSIMP. The numbers indicate approximate memory requirements in kbytes, in a compressed format.

The array package lets the user set up generalized arrays, extracts their components and performs element-wise operations between arrays or between arrays and scalars. The matrix package goes one step further. It provides the following matrix operations on arrays: transpose, multiply, divide, invert and raise to integer powers. Messages warn of improper operations, such as raising a singular matrix to a negative power.

The trigonometrics packages simplify equations by exploiting symmetry, angle reduction, multiple-angle expansion, angle-sum expansion, elimination of reciprocals and certain products, simplifications of trig functions and their inverse, and even replacements of sines and cosines by complex exponentials.

The differentiation package returns the symbolic first partial derivative of the first argument with respect to the second one, for example:

$$\text{DIF}(ax^2,x) \text{ yields } 2ax;$$
$$\text{DIF}(\ln(x+a),x) \text{ yields } 1/(x+a).$$

Higher-order partial derivatives can be requested by nesting DIF commands; if a differentiation rule is not known to the system, the input is not evaluated. However, the user can incorporate additional rules.

The integration package works similarly, for instance,

$$\text{INT}(ax+\sin x,x)$$

yields

$$ax^2/2 - \cos x.$$

If a closed-form integral cannot be found, the solution contains unevaluated integrals. Many of these can be tackled with the extended integration module. Nested integration will request an iterated integration; for example, yx^2 can be evaluated:

$$\text{DEFINT}(\text{DEFINT}(yx^2,y,0,(1-x^2)^{1/2},x,-1,1).$$

Max Schindler

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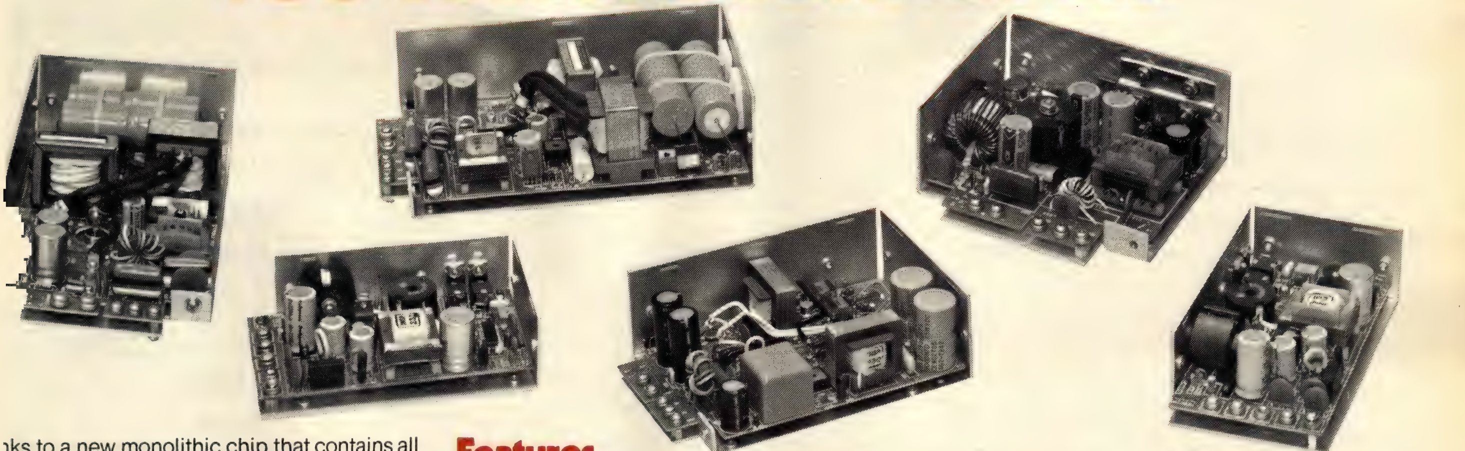

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DC Output. See charts.

DC Output Adjustability. ±10%

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S-15C	15 VOLTS	1.2 AMPS
S-24C	24 VOLTS	0.75 AMPS
S-28C	28 VOLTS	0.65 AMPS
S-36C	36 VOLTS	0.5 AMPS

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MODEL	VOLTAGE	CURRENT
ES-5D	5 VOLTS	6 AMPS
ES-12D	12 VOLTS	3 AMPS
ES-15D	15 VOLTS	2.4 AMPS
ES-24D	24 VOLTS	1.5 AMPS
ES-28D	28 VOLTS	1.3 AMPS
ES-36D	36 VOLTS	1.0 AMPS

ES-E Series $89. 4.62" x 4.88" x 2.00"

MODEL	VOLTAGE	CURRENT
ES-5E	5 VOLTS	10 AMPS
ES-12E	12 VOLTS	5 AMPS
ES-15E	15 VOLTS	4 AMPS
ES-24E	24 VOLTS	2.5 AMPS
ES-28E	28 VOLTS	2 AMPS
ES-36E	36 VOLTS	1.5 AMPS

S-F Series $149. 7.10" x 4.88" x 2.37"

ODEL	VOLTAGE	CURRENT
ES-5F	5 VOLTS	20 AMPS
ES-12F	12 VOLTS	10 AMPS
ES-15F	15 VOLTS	8 AMPS
S-24F	24 VOLTS	5 AMPS
S-28F	28 VOLTS	4 AMPS
ES-36F	36 VOLTS	3 AMPS

ES-G Series $189. 8.60" x 4.88" x 2.37"

MODEL	VOLTAGE	CURRENT
ES-5G	5 VOLTS	30 AMPS
ES-12G	12 VOLTS	15 AMPS
ES-15G	15 VOLTS	12 AMPS
ES-24G	24 VOLTS	8 AMPS
ES-28G	28 VOLTS	7 AMPS
ES-36G	36 VOLTS	5 AMPS

ES-H Series $229. 10.60" x 4.88" x 2.60"

MODEL	VOLTAGE	CURRENT
ES-5H	5 VOLTS	45 AMPS
ES-12H	12 VOLTS	22 AMPS
ES-15H	15 VOLTS	18 AMPS
ES-24H	24 VOLTS	12 AMPS
ES-28H	28 VOLTS	10 AMPS
ES-36H	36 VOLTS	8 AMPS

ıns: Crowbar up to 8 Amps $8, greater than 8 Amps $16; Add Suffix V to Model No. Cover $6, Add Suffix C to Model No. Logic Inhibit $8; Add Suffix I.

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CIRCLE NO. 16

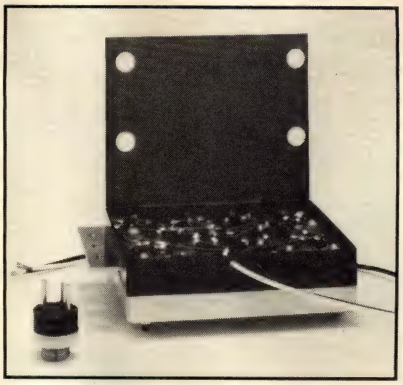
Compact module passes 700 A through 14 transistors

As if designing power transistor arrays that pass hundreds of amps were not difficult enough, PowerTech (Fair Lawn, NJ) has invented a method for squeezing the devices into a deceptively small package. The high-current transistor specialists mount 14 copper-metallized transistors in a solid copper block that measures just 6.4 × 3.9 × 1.3 in.

The new compact power module handles 700 A, withstands 400-V collector-to-emitter breakdown and drops only 3 V (V_{CESAT}) at 700 A. Because of the special manufacturing techniques that create the power transistors, the module boasts a minimum overall gain of 100 at 700 A.

The 14 transistors—two drivers and 12 paralleled output devices—each sit in a threaded hole in the module block. Each transistor is a very large chip, 570 mils diameter. After the diffusion process, PowerTech attaches a heavy copper metallizing grid to the base-emitter area. The grid allows excellent SOA capability and very low saturation voltage. On the bottom of the device, a copper-molybdenum heat sink is mounted to provide the proper thermal match when the chip is finally set into its studded copper header. Since the stud's threads match the holes in the copper block, the transistors are simply screwed into the block.

Because the heat sink is integral with the chip, transistors can be completely tested and characterized at high current levels before being mounted. All devices are 100% tested and sorted into many categories: from 40 A, 600 V breakdown to 200 A, 80-V breakdown. The devices are either ultra-rugged single-diffused or ultra-fast triple-diffused. Production spreads are so tight that transistors can be easily matched for V_{BE} and gain. They can be paralleled without concern for the current-sharing problem that usually arises with bipolar transistors. No current-sharing resistors are used, and the transistors track well over a wide temperature and current ranges. In effect, each transistor becomes a power module or building block in itself.



Inside the black box sits a solid copper block into which fourteen power transistors are mounted. The device has an overall current carrying cabability of 700 A. A typical power transistor is shown at the lower left.

To finish the package, copper plates slip over the mounted transistors. Each plate is cut out to match the hole arrangement of the block. The plates allow for the interconnection of devices and also serve as the module's input and load-current buses.

Flexibility is the key to the PowerTech system. The 14-transistor configuration is only one of many that can be built. Many of the company's products are built to specialized packaging and electrical specifications. Thus, a powerblock can be fabricated in any size or shape and can contain any number of power transistors.

This power handling ability does not come cheaply. But the PowerTech system has few competitors, especially for military specification devices.

Gene Heftman

µP-based devices simplify data-comm networks

Microprocessor-based devices will bring both flexibility and economy to data-comm-equipment design—across the board. With applications ranging from long-haul data-transmission systems to local data-distribution networks, systems designers, for one thing, will be able to integrate the special requirements of such formerly diverse areas as distributed data processing, word processing and electronic offices. The tools? Such µP-based devices as long-haul modems, limited-distance data sets, message switches, statistical multiplexers and programmable data-comm analyzers.

These developments and directions came to light at the annual Data Communications Techniques seminar presented in New York by Instrument Sales Co. (Ridgewood, NJ).

One example of the growing impact of µP devices on data-comm equipment is modems. By the mid-1980s, single modems will probably handle multiple data rates of 0 to 300, 1200, 2400 and 4800 bits/s, predicts Ray Jenkins, eastern regional manager of Sunnyvale-CA-based Racal-Vadic. It should prove a welcome impact. According to Jenkins, future data-comm networks will need this kind of flexibility to ac-

Table 1. Cost estimates for long-haul modems

Data rate (bits/s)	Mode (duplex)	Price ($ per end)
0 to 300	Full	300
1200	Half	500
1200	Full	900
2400	Half	900
2400	Full	1500
4800	Half	3000
9600	Half	9000

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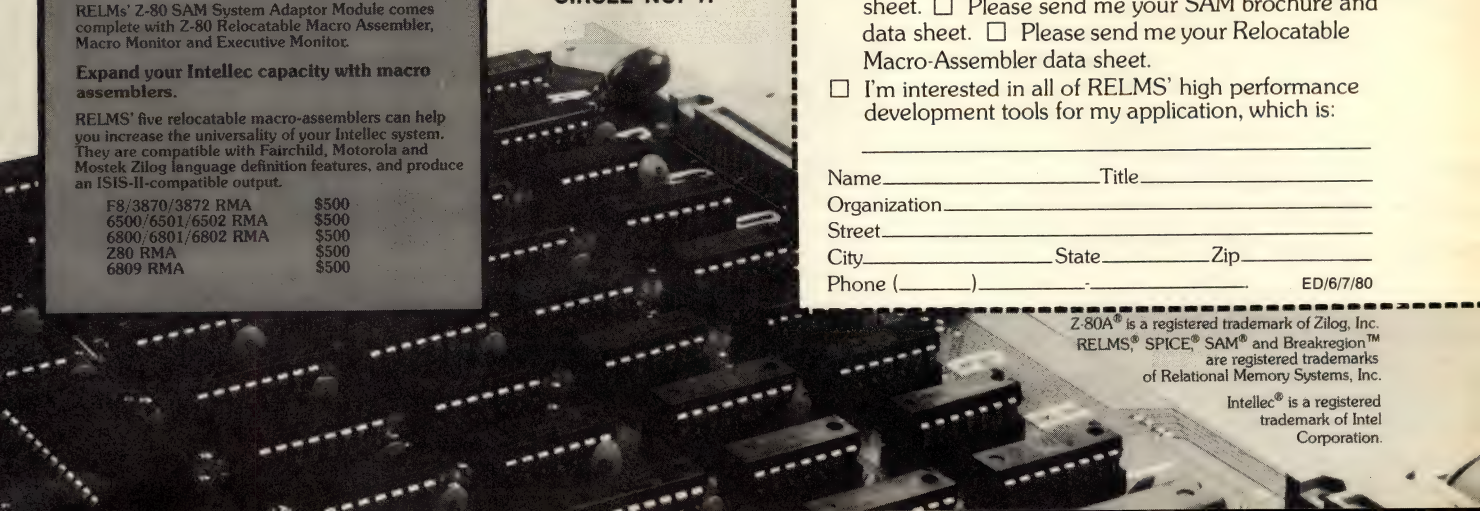

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commodate different kinds of terminal equipment. Multiple-data-rate modems should also bring economics to data-comm system designs.

Roughly 95% of today's data-comm traffic passes over analog telephone-company lines and therefore uses modems, Jenkins estimates. But as more powerful equipment is distributed over more locations, more sophisticated data-comm network equipment will be needed. The trend is clearly towards augmenting such basic units as Bell-103/113-compatible sets, which operate asynchronously in full-duplex mode over two-wire lines, with modems that support such higher speeds as 1200, 2400, 4800 and 9600 bits/s.

Besides their capability, of course, the per-end cost of these long-haul devices goes up with the bit rate (Table 1). Combining many of these capabilities in a single μP-based set would cut cost and provide the flexibility needed in networks that service equipment operating at different data rates.

For that matter, Jenkins sees equipment integration going beyond just combining multiple bit rates. Another combination he believes will become popular is the telephone handset with an integral modem. Racal-Vadic now offers a 300-bit/s unit and Jenkins expects a 1200-bit/s unit by 1985. In the same time frame, Jenkins also foresees a 4800-bit/s data set, compatible with Bell's 208, costing perhaps $2000 as compared with the 300-bit/s device's $3000 price tag. Special features like automatic dialing should also become popular.

One cost-effective alternative to long-haul modems operating with telco-DDD lines could be limited-distance links that connect to digital-transmission services like AT&T's DDS or satellites, according to another seminar participant, Bo Sullivan, eastern regional manager of Avanti Communications (Newport, RI). Often, limited-distance modems can halve the data-set cost in systems that access long-haul transmission trunks via local concentrators. In addition, relatively inexpensive limited-distance data sets could hold down costs of local-area data-distribution systems confined to industrial plants, buildings, campuses, cities and counties. What's more, with many limited-distance sets operating effectively only on leased lines and not on the switched circuits of the DDD network, AT&T's decision to impose time charges on local DDD calls could help tip the scales in favor of limited-distance data sets working into leased lines.

The only real difference between medium-distance modems and their long-haul counterparts is in the equalization, Sullivan states. Long-haul sets use adaptive equalizers, or complex filters that change (train) characteristics to match the transmission medium. Medium-distance sets get by with less expensive, fixed, compromise equalization circuitry. Reducing the equalization cost makes a great difference in the final cost, says Sullivan. Modems servicing 100-mile links at 4800 bits/s cost from $1200 to $1500 per end depending on the diagnostics included. Similar long-haul data sets cost about $3000 per end. The cost difference is even wider at 9600 bits/s: $3000 to $3500 for medium-distance vs $9000 for long-haul.

Cost effective modems

Avanti's specialty—μP-based medium-distance modems—may be a cost-effective choice for 2400, 4800, and now 9600 bits/s (see ELECTRONIC DESIGN, May 24, 1980, p. 168) over up to 100 miles of 3002-type voice-grade leased lines. But they are not always the best choice for much shorter distances, Sullivan adds.

For example, in systems that work over unloaded twisted pairs or EIA cable, non-μP short-haul modems and even the simple-modem eliminators (or line drivers) sometimes cut costs dramatically. To present a complete cost picture, Sullivan has tabulated the costs of several different sets when used to transmit data synchronously (with a separate clock) at 4800 bits/s from, say, the first to the fourth floor of an office building (Table 2). The most expensive, a 208 modem, works into switched voice-grade lines. The second most expensive, a medium-distance set, is not intended to work into switched lines and so must be used with a dedicated (leased) circuit. Going down another step in cost, the short-haul modem works into an unloaded twisted pair. And the least expensive set, the modem eliminator, works into at most 400 ft of 12 or 24-conductor EIA cable. What's more, a modem eliminator is required at only the transmission end of its cable and

Table 2. Intrabuilding data-distribution options (4800 bits/s)

Data set	Medium required	Data set cost	
		(unit)	(total)
Bell 208	Switched v-g lines	$3000	$6000
Medium-distance modem	Leased lines	1300	2600
Short-haul modem	Unloaded twisted pairs	800	1600
Modem eliminator	EIA cable (400 ft)	360	360

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hence is even more economical than its cost implies. But cable costs are a separate matter, reminds Sullivan, and especially serious when considering a modem eliminator.

Paperless storage

There's more to the story than the coming modems and data sets. Various line types, equipment categories, protocols and end uses are fast becoming part of the integrated electronic office. Nowhere is this union better illustrated than in electronic mail, a growing phase of office automation that Cloyd Marvin, vice president of Compression Labs (Cupertino, CA) describes as "paperless storage." Marvin envisions store-and-forward message-switching stations as the logical way to coordinate information passing on such media as Telex, TWX, DDD, leased lines and EIA cables to such equipment as facsimile machines, printers and CRT-based terminals or host processors.

Multifunctionality is the key to practical message switching. Marvin sees disk-based μP-controlled message switches efficiently tying together a variety of communications lines, protocols and bit rates. In addition, a store-and forward switch could even convert among codes and compress data.

Multiplexers can concentrate data onto high-speed lines for efficient transmission. The most efficient concentration method is statistical time-division multiplexing, explains Charles Grutzius, data-comm manager at Digital Communications Corp. (Germantown, MD). Holding that assigning fixed time slots to specific equipment on a high-speed digital channel could result in unused capacity when a device is inactive, Grutzius proposes multiplexing statistically (on demand) with high-speed channel time assigned only to active terminals. Anticipating the use of its Stat-Muxing equipment in complex data-comm networks as well as in point-to-point links, Digital Communications Corp. controls data transmission over the high-speed (multiplexed) line via level 2 of the X.25 protocol.

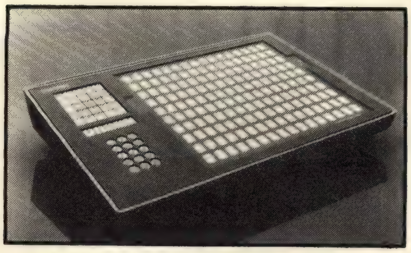
As data-transmission networks get more complex, specialized instruments are needed to maintain peak operating efficiency. One such instrument, described by J. Lightsey Wallace, assistant director of new product development at Atlantic Research (Alexandria, VA), is a data analyzer with plenty of features: a CRT display, tape storage of line signals, a functionally labeled keyboard, a machine-prompted test-selection menu and support for such popular data-comm protocols as X.25 and X.75 HDLC/SDLC.

Sid Adlerstein

μP-controlled keyboard generates 19,200 symbols

A keyboard that supplies 19,200 characters or symbols under the guidance of an 8085 microprocessor can symbolize each product in a full inventory, every check or control stage of a manufacturing process or specific locations on a map (for military tactical operations). The 8085 contains 512 bytes of RAM and 1 kbyte of ROM. The ROM holds data on character code conversions that transform a keyboard entry into a binary word representing a symbol or a Chinese, Japanese or Korean character.

Each character or symbol is defined by two binary 8-bit codes. Thus, it can be transmitted and handled by all data processing equipment using the ASCII code for data transfer, so long as the equipment treats the information like a character string without regard to content.



The 10 × 16-key array of the Ideographix keyboard puts 19,200 characters under μP control.

Made by Ideographix, Inc. (Sunnyvale, CA), the keyboard contains a main field of 160 keys (in a 10 × 16 array) called GROUP. The selection of a key closes a pressure-sensitive switch mounted on a flat rigid panel. Each switch closes under 3-oz of pressure with only 0.0007-in. travel. To select the desired one of the five different characters accessible with each GROUP key, the operator presses a shift key. The shift function is handled by a CHARACTER array of keys.

Two other arrays modify the GROUP array. With the five MASK keys, the operator can choose from four overlays for the keyboard (one key provides for future expansion). One of the overlays contains the most commonly used characters in, for example, Chinese, to cut down on changes from overlay to overlay in pursuit of a specific character. For each new overlay, the operator must press the appropriate shift key before keying in the character.

According to the keyboard's inventor and the president of Ideographix, Inc., Chan Yeh, an operator can easily record 50 characters/min. (Each Chinese or Japanese character is the equivalent of one English word.) Transmitted data displayed at a remote location require a computer terminal that can handle the special language characters.

Jonah McLeod

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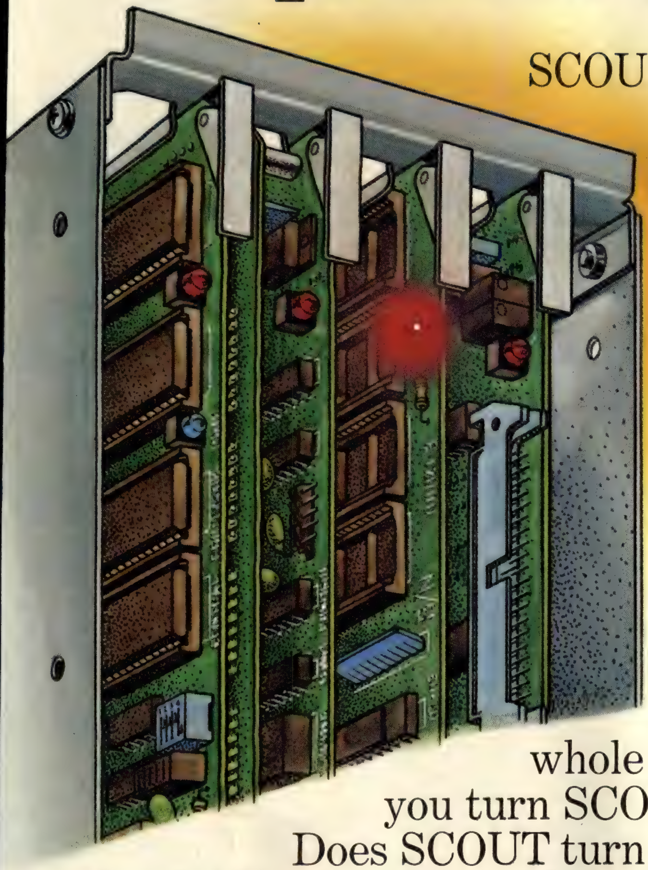

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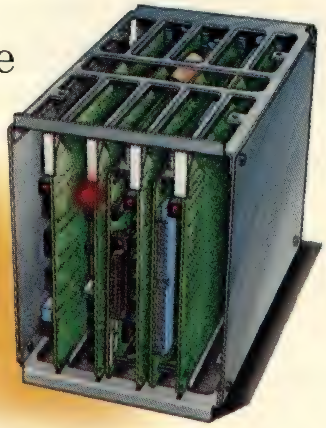

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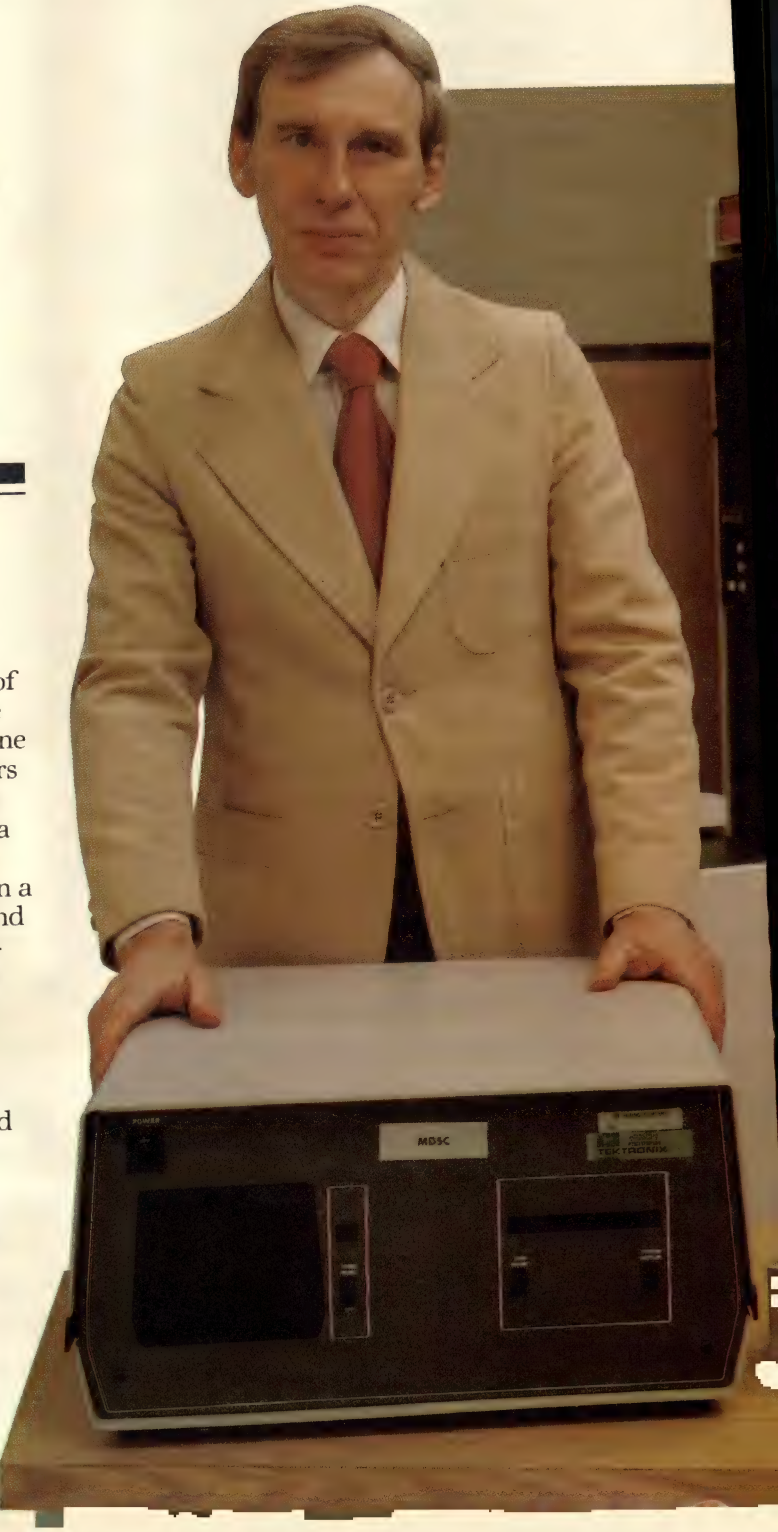
CIRCLE NO. 19

At Boeing forty dedicated systems Tektronix 8001s



The Microprocessor Design Support Center (MDSC) is Boeing's innovative answer to large scale microprocessor development. Tektronix makes it possible.

Boeing now supports over 120 engineers working on 35 projects.

Before the creation of the MDSC, Boeing used a variety of different vendors' stand-alone development systems. Each one supported only three engineers at a time, and more than one system was often needed for a single project.

Now, software is developed on a DEC PDP 11/70® computer and transferred to six 8001 Microprocessor Development Labs for in-circuit emulation, debugging, and prototype integration.

By using one multi-user host computer with six distributed 8001s, Boeing is able to more efficiently support 120 engineers. With 8001s costing half as much as stand-alone development systems.

ouldn't do what six
re doing.

Development isn't limited by dedicated, single-vendor systems.

The 8001 supports every microprocessor Boeing uses, so, they're free to choose the right microprocessor for the job. And whether it's the Texas Instruments TMS9900, Zilog Z80A, Intel 8048, Motorola 6800, RCA 1802, or 14 others — the 8001 emulates it. Tek's multi-vendor support doesn't lock Boeing into one vendor's family of microprocessors.

Engineers get on board much faster.

When every engineer uses the same equipment and the same operating system for every project, it translates into a faster learning curve. And a more efficient, flexible team. For Boeing — or for you.

The world over, Tektronix supports your team with our team, assisting you with everything from development system configuration planning to training to service. Whether your development plans include our 8001 MDL, or our stand-alone 8002A MDL, we'll back you with quality — every step of the way. For a closer look at Boeing's innovative use of the 8001, please call your local Tektronix Field Office or write to us for our Boeing Application Note.

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R TECHNICAL DATA CIRCLE NO. 20
R DEMONSTRATION CIRCLE NO. 21

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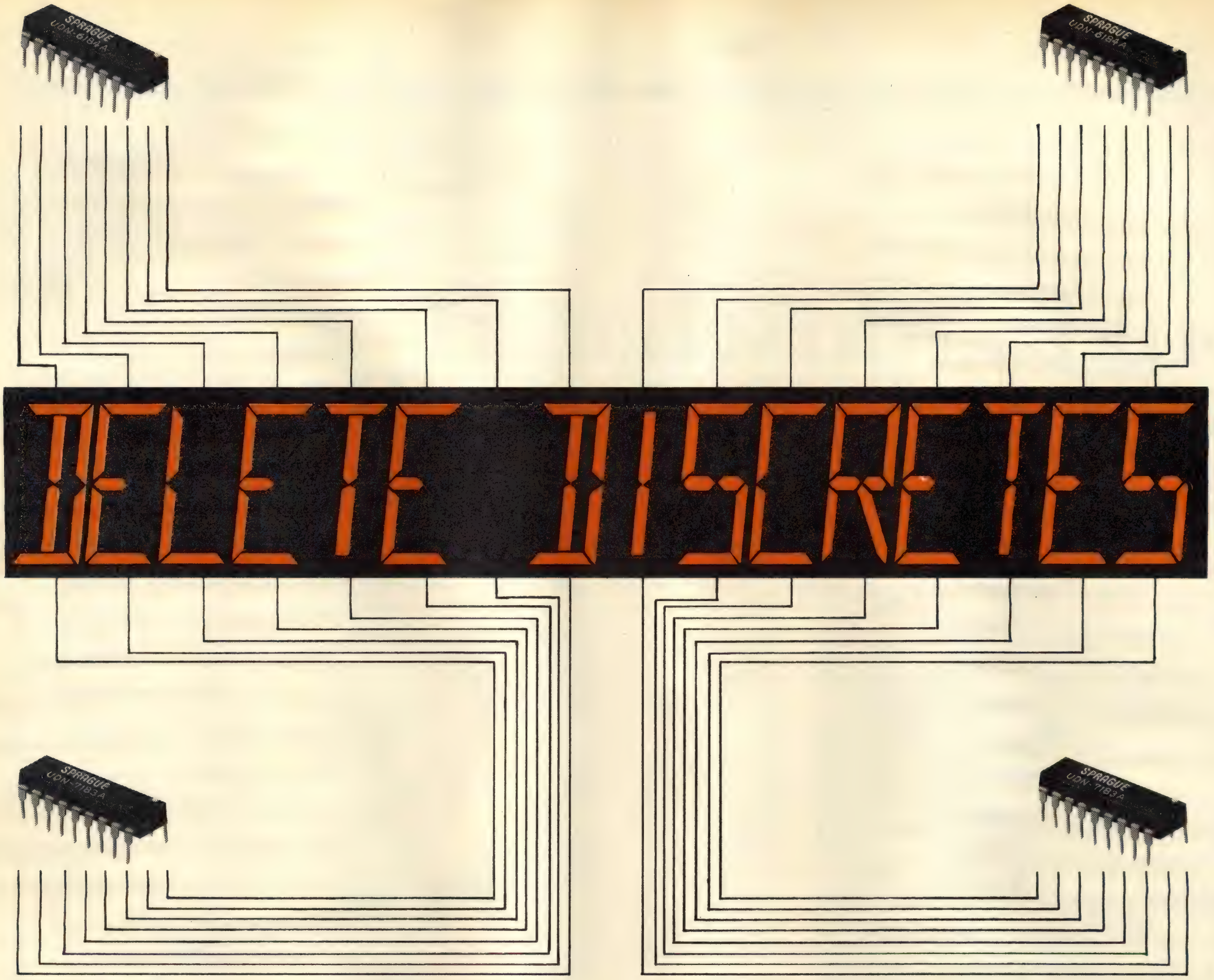

Now...A Series of Sprague ICs that simplify gas discharge display interface

Sprague Series UDN-6100/7100 Display Drivers offer the systems designer a simplified, low-cost interface with planar gas discharge displays that essentially eliminate the need for discrete components. Designers can now take advantage of the superior aesthetics of gas discharge panels with their low power consumption, relative ease in customizing, and large digit capability without the need to use large quantities of discrete components.

With broad commercial/industrial applications, these unique drivers find wide usage in business calculators, POS systems, cash registers, scales, appliances, clocks, electronic games, instrumentation, computer peripherals, industrial controls, avionics, and a variety of other display products.

Series UDN-6100 Digit (anode) Drivers are rated with a supply voltage of +120 V max. and an output current of 70 mA max. They are available with 4, 6, or 8 drivers per device, in 14, 16, and 18 pin plastic and hermetic DIP packages, respectively.

Series UDN-7100 Segment (cathode) Drivers operate at a max. supply voltage of −120 V. Circuits are available with nominal output current ratings from 0.6 mA to 14 mA. Each device has 8 drivers and is available in an 18-pin plastic or hermetic DIP package.

For application engineering assistance, write or call Paul Emerald, Semiconductor Division, Sprague Electric Company, 115 Northeast Cutoff, Worcester, Mass. 01606. Tel: 617/853-5000.

For Engineering Bulletins 29311 and 29312 as well as WR-172A 'Quick Guide to Interface Circuits', write to: Technical Literature Service, Sprague Electric Company, 347 Marshall Street, North Adams, Mass. 01247.

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CIRCLE NO. 22

WashingtonReport

It takes a computer to catch a thief. . .

The International Association of Chiefs of Police will test an advanced microcomputer system that follows the progress of pending investigations and makes staff assignments according to the priority of each probe.

Under a $138,985 grant from the Justice Department's Law Enforcement Assistance Administration, the microcomputer and software package will first be installed in two cities, not yet selected, and then in several major cities around the country.

. . .Or to tempt one

Computers that are the targets of criminals or the tools for committing a crime are now the target of a training/instruction manual to help law enforcement officials.

Developed by the Justice Department, through a grant to Battelle Institute (Columbus, OH), the textbook suggests that investigators and prosecutors enlist the services of engineers, programmers and systems analysts in their investigations. "One can no more investigate a complex 'computer crime' alone than one could investigate an art forgery without help," the manual says.

Justice Department officials predict that one day, the computer professional will assist law enforcement to the same extent as doctors and similar experts.

NASA, SBA agree on contracts for small firms

A voluntary agreement between the National Aeronautics and Space Administration and the Small Business Administration will open up high-technology NASA contracts to small and minority-owned businesses. SBA already has the authority to direct government contracts to small firms in some cases; but the pact with NASA is a separate program. The space agency will have the final say over all contract awards.

Meanwhile, to keep its field offices up to date on the latest programs and policies in Washington, SBA has awarded a $1.8 million contract for a network of 149 computer terminals in SBA offices nationwide. The contract was awarded to a Washington-based, minority-owned electronics firm, International Business Services Inc., which will install, operate and maintain the computer links.

U.S. casts $2.59 billion of semis on the waters

Shipments of semiconductors overseas shows a healthy increase, from $1.92 billion in 1978 to $2.59 billion by the end of 1979. At the same time, imports rose from $1.76 billion to $2.42 billion, for a trade surplus of $179.1 million last year.

The figures from the Commerce Department indicate that 33% of the semiconductor shipments went to overseas assembly facilities; 85% of the imports consisted of finished products containing semiconductors.

Overall, the trade in components in 1979 included $3.9 billion in exports and $3.6 billion in imports, giving a total trade surplus of about $300 million in favor of the U.S.

Opponents deflect the MX missile system

The advanced MX missile system has met opposition from several directions—including the Joint Chiefs of Staff and residents of Utah and Nevada, where the missiles would be placed. Although the Carter administration has tentatively approved the MX, it may be rethinking the concept as it was originally planned.

In testimony before a Senate Defense Appropriations Subcommittee, a group of military experts (including retired Adm. Thomas Moorer, former chairman of the Joint Chiefs of Staff) called for the MX to be abandoned in favor of improved submarine based missiles, a space-oriented antimissile system and redeployment of the Minuteman III land-based missile system. The military men argued that Soviet submarines would be difficult to eliminate by MX missiles in the event of a Soviet first strike. By contrast, the space antimissile system would deter a Soviet launch in the first place. The Minuteman system could be deployed in three years, they said, but the MX will take ten years.

Because of opposition from residents of Utah and Nevada, the Defense Department may abandon the oval "race-track" deployment system for MX missiles in favor of a "straight line" scheme. The straight-line arrangement takes less land for missile sites and will save money. The basic concept, in which a fixed number of ICBMs are moved among a network of silos at random, remains unchanged.

Patents may protect federal-sponsored inventions

More of the inventions that are developed through federal contract research will become commercial products, under a bill approved in a 91 to 4 vote by the U.S. Senate. As sponsored by Sens. Birch Bayh (D-IN) and Robert Dole (R-KS), the bill would permit small businesses, nonprofit organizations and universities to obtain a 17-year patent on inventions created as a byproduct of federally sponsored research and development. Larger firms would get similar patents or exclusive licenses, but the term would vary.

Current policies on the subject are vague and often contradictory. In many cases, title to the invention must be turned over to the government, which issues nonexclusive licenses to all comers. According to backers of the Bayh-Dole bill, those conditions make companies reluctant to market their inventions.

The measure now goes to the House, where similar efforts are pending and the reception is expected to be positive.

Capital capsules:

To win broadcasters to its AM stereo broadcast system, **Magnavox Consumer Electronics Co. will not exercise patent rights** against broadcasters or broadcast equipment manufacturers. The company, which recently won FCC approval for the system, will charge a "reasonable license fee" to receiver manufacturers. . . . **The FCC is returning petitions for certification** filed by the makers of handheld computing devices. A change in FCC regulations eliminated the need for certification for those products. Manufacturers of the handhelds will still be responsible for making sure the devices do not interfere with other electronic products. . . . **Commerce and Treasury Department officials have reached agreement with Japanese television makers** on the payment of antidumping duties owed by the Japanese firms. The U.S. will drop the dumping cases in return for a $75 million payment over and above the $70 million already collected. . . . In a similar case, however, a federal judge has ruled that **dumping charges against other Japanese television companies could not be pressed** (except for battery-operated units). The court ruled that the power supply and tuner design of Japanese products exported to the U.S. differ substantially from those of models sold in Japan.

TM 500 lets you fill in the blank.

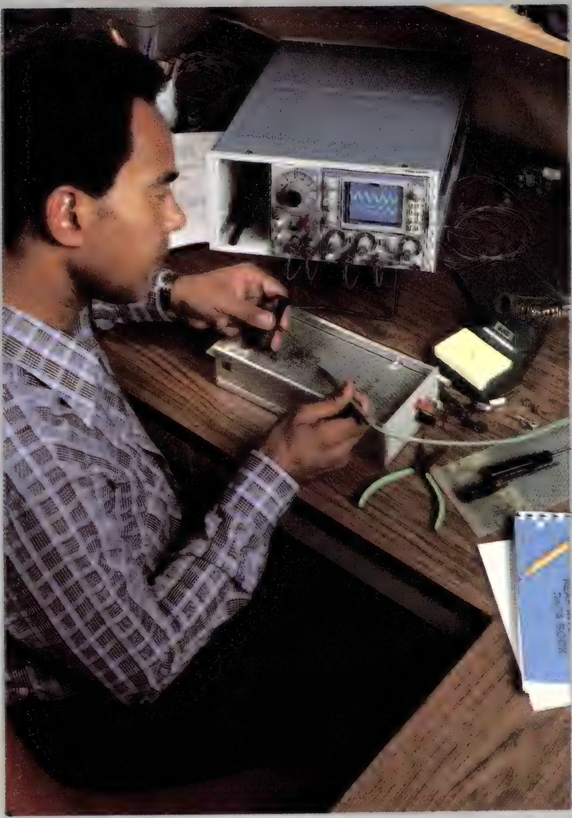
Our custom plug-in kit spans your measurement gap.

Sometimes test and measurement problems demand solutions standard instruments just can't provide. So instead of drawing a blank, TM 500 lets you fill one in. With the product of your own ingenuity.

It's done through our blank custom plug-in kits, either one or two compartments wide. You get a perforated main circuit board for easy assembly of both ICs and discrete components. And, the necessary mechanical parts. Plus complete *information* on use of the power supplies in the TM 500 mainframes.

There's even a one-compartment kit complete with power supply components to power your own creations.

Now you can have those specialized devices that make the difference. Like signal switching circuitry, preset oscillators, or a/d converters. And for new ideas, we can supply a series of Construction Notes with complete schematics and parts lists for building a number of custom plug-ins.



We also offer nearly 40 standard plug-in modules, covering everything from DMMs to oscilloscopes to generators.

To find out more about TM 500, contact your local Tektronix Field Office, or write Tektronix, Inc.

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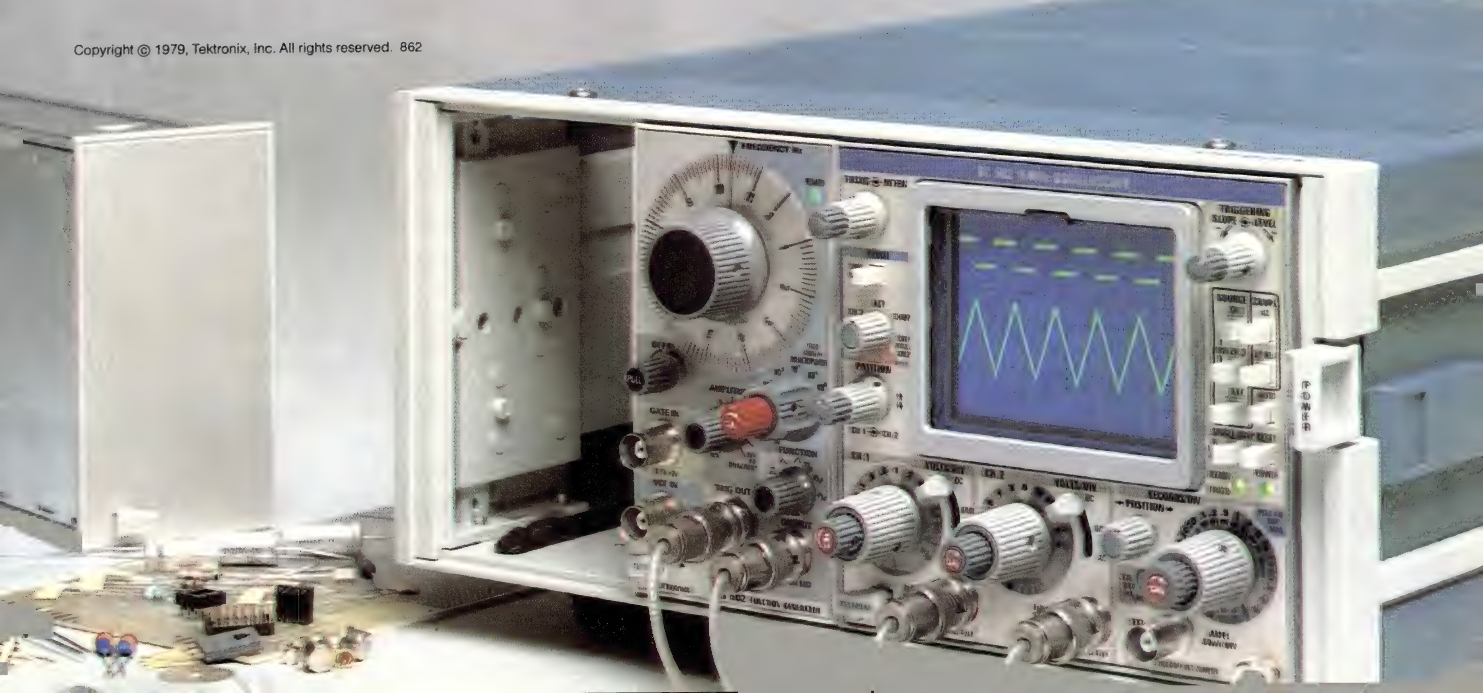

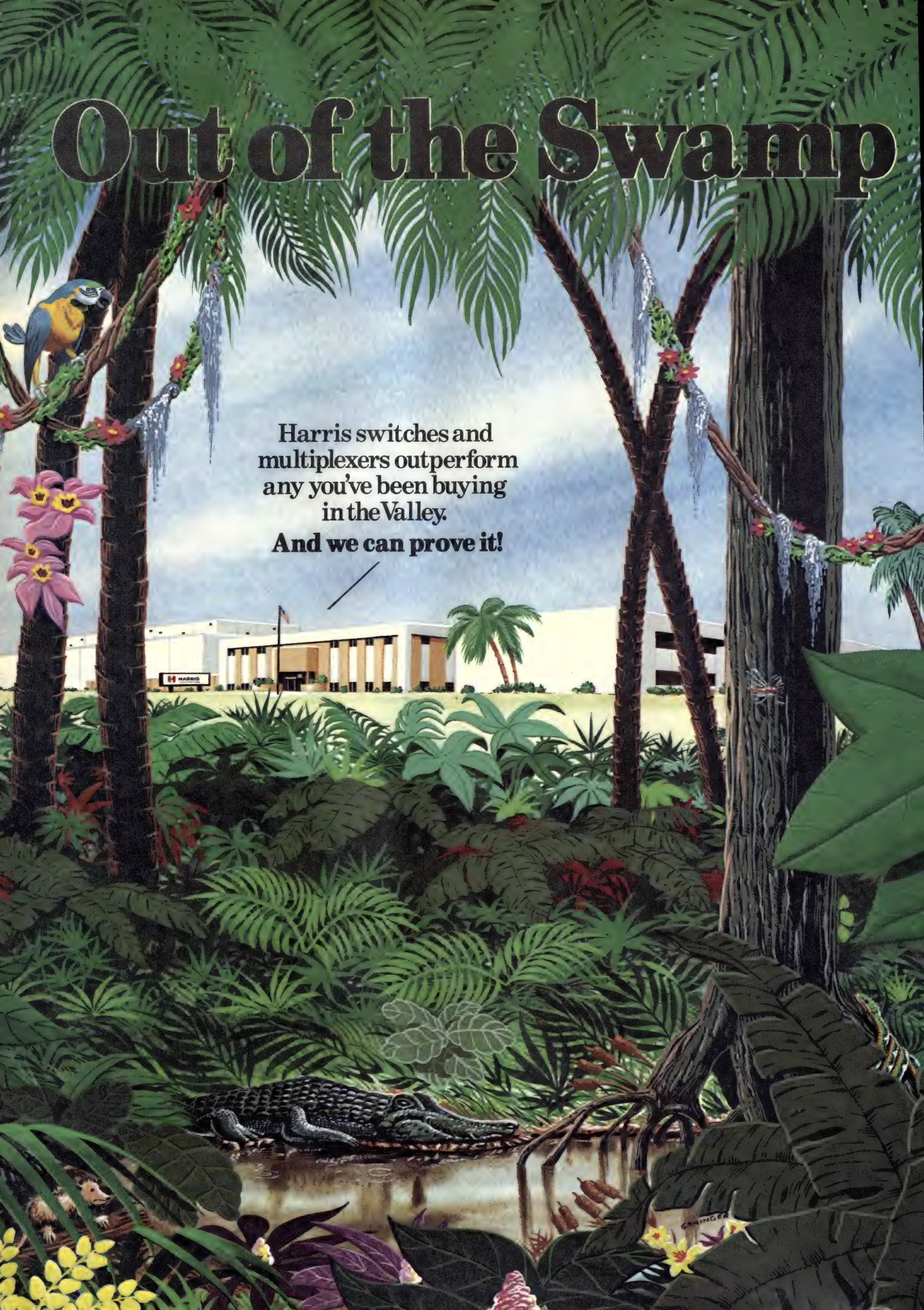
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Harris switches and multiplexers outperform any you've been buying in the Valley.
And we can prove it!
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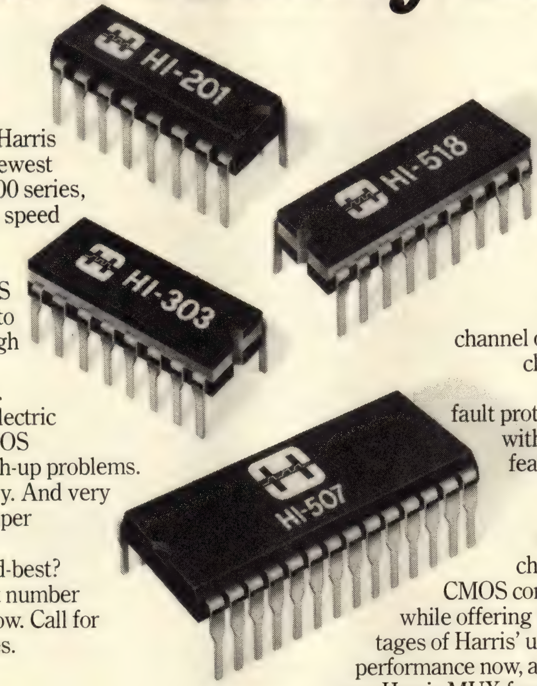
(And a new family of products!)



Swift switches.

You're way ahead when you switch to Harris monolithic analog switches. And the newest member to our switch family, the HI-300 series, is setting the pace for the industry—in speed and quality.

There's a broad range of parts offering DTL, TTL, CMOS and PMOS compatibility for easy incorporation into your data acquisition systems. Plus high current capability (typically 80 mA) and wide analog signal range (±15 V).

Each switch employs unique Dielectric Isolation (DI) and Complementary CMOS processing, so there are never any latch-up problems. No overheating when switching rapidly. And very low input and output leakage—plus super switching speeds.

Why continue to settle for second-best? You'll find the replacement Harris part number in the chart below, to help you order now. Call for prompt delivery and competitive prices.

The switch is on—to Harris!

Max MUXes.

Now Harris offers a complete family of analog multiplexers. The line includes devices featuring ultra-high speed, overvoltage fault protection, and pin-for-pin replacements of all popular multiplexer products.

The new HI-516 and HI-518 offer unprecedented speed—1 μs settling to 0.01% accuracy. They can be configured under logic control for 16-channel or 8-channel differential (HI-516) or 8-channel or 4-channel (HI-518) operation, for maximum flexibility.

Several Harris multiplexers provide overvoltage fault protection. They withstand overvoltages up to 20 volts without faulting the output or any other channels. This feature is unique to Harris products—**and gives you a competitive edge in system reliability!**

Other popular Harris multiplexers include 16-channel/8-channel differential and 8-channel/4-channel differential versions that are TTL, DTL and CMOS compatible. They directly replace other multiplexers, while offering the outstanding performance and reliability advantages of Harris' unique Dielectric Isolation (DI) processing. Get max performance now, at competitive prices and off-the-shelf delivery. Pick your Harris MUX from the chart below. Then call the Harris Hot Line, or write: **Harris Semiconductor Products Division, Box 883, Melbourne, Florida 32901.**

ANALOG SWITCHES

Competitive Part Number	Harris Pin-for-Pin Replacement
DG 200	HI-200
DG 201	HI-201
DG 300 DG 301 DG 302 DG 303	HI-300 HI-301 HI-302 HI-303
DG 304 DG 305 DG 306 DG 307	HI-304 HI-305 HI-306 HI-307

Competitive Part Number	Harris Pin-for-Pin Replacement
IH 5040 IH 5041 IH 5042 IH 5043	HI-5040 HI-5041 HI-5042 HI-5043
IH 5044 IH 5045 IH 5046 IH 5047	HI-5044 HI-5045 HI-5046 HI-5047
IH 5048 IH 5049 IH 5050 IH 5051	HI-5048 HI-5049 HI-5050 HI-5051

ANALOG MULTIPLEXERS

Competitive Part Number	Harris Pin-for-Pin Replacement	Harris Pin-for-Pin Replacement with true Input Overvoltage Fault Protection
DG506AR DG506BR* DG506CJ	HI1-506-2 HI1-506-5 HI3-506-5	HI1-506A-2 HI1-506A-5 HI3-506A-5
DG507AR DG507BR* DG507CJ	HI1-507-2 HI1-507-5 HI3-507-5	HI1-507A-2 HI1-507A-5 HI3-507A-5
DG508AP DG508BP* DG508CJ	HI1-508-2 HI1-508-5 HI3-508-5	HI1-508A-2 HI1-508A-5 HI3-508A-5
DG509AP DG509BP* DG509CJ	HI1-509-2 HI1-509-5 HI3-509-5	HI1-509A-2 HI1-509A-5 HI3-509A-5
No comparable parts No comparable parts No comparable parts No comparable parts	HI1-516-2 HI1-516-5 HI1-518-2 HI1-518-5	— — — —
No comparable parts No comparable parts	— —	HI1-1840-2 HI1-1840-5

*Industrial temperature range

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CIRCLE NO. 23

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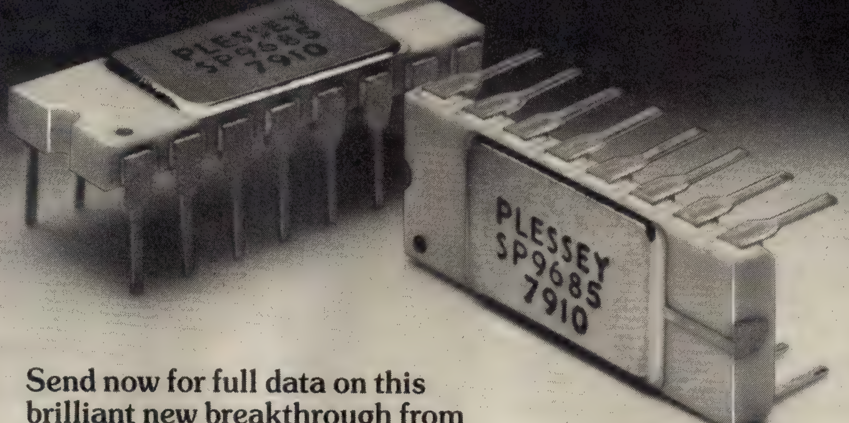

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CIRCLE NO. 150

P236

ElectronicDesign

INTERNATIONAL

June 7, 1980

Process controller automates small test assemblies

Switching-supply series offers 40 choices

Desktop computers get flexibility from disks

Modular power supplies vary to suit requirements

Multiple choice test.

Philips now gives you a wider choice in low frequency oscilloscopes, so you can better tailor the scope to your application.

Need a 25MHz/single time base scope? Choose the PM3212. A 25MHz with delayed time base? Choose the PM3214.

If your application requires a higher bandwidth and shorter rise time, choose one of the new 35MHz scopes from Philips.

Our PM3216 has a single time base; the PM3218 has delayed time base. Both have a maximum sweep speed of 10ns/div. and a trigger hold-off facility that eliminates double triggering on digital signals, making it unnecessary to use the time base in the uncalibrated mode.

All four oscilloscopes feature trigger selection from either channel, line, external source or composite triggering for asynchronous signals. The alternate time base displays of the PM3214 & 18 allow them to do the work of much more expensive instruments. Just press delayed time base and main time base simultaneously and both time base sweeps are displayed for one or both channels.

In addition, all four feature wide trigger bandwidth plus 10kV CRT for high light output and excellent resolution. Of course they are strong, rugged and lightweight.

Now, more than ever, Philips wants to make *your* next scope. And your next Logic Analyzer. And your Microcomputer Development System. We're going to give you a better multiple choice so you'll buy from us.

For more information contact the Philips organisation in your country or write to Philips Industries, Test & Measuring Instruments, TQ III-2, 5600 MD Eindhoven, The Netherlands.

From Philips, of course.

Test & Measuring Instruments

PHILIPS

CIRCLE NO. 152

Process controller automates small test assemblies

A process controller from Rohde & Schwarz makes automation attractive for small test assemblies by handling many mathematical, electronic and administrative tasks with the programming power of expensive computers.

Working with an extended Basic language, the PPC controller takes advantage of powerful editing instructions to ease program development. In addition, a 5-¼-in. floppy-disk drive offers 80 kbytes of memory space and split-second transfer of programs and data between disk and main RAM. The RAM itself has a capacity of 16 or 32 kbytes, depending on the model.

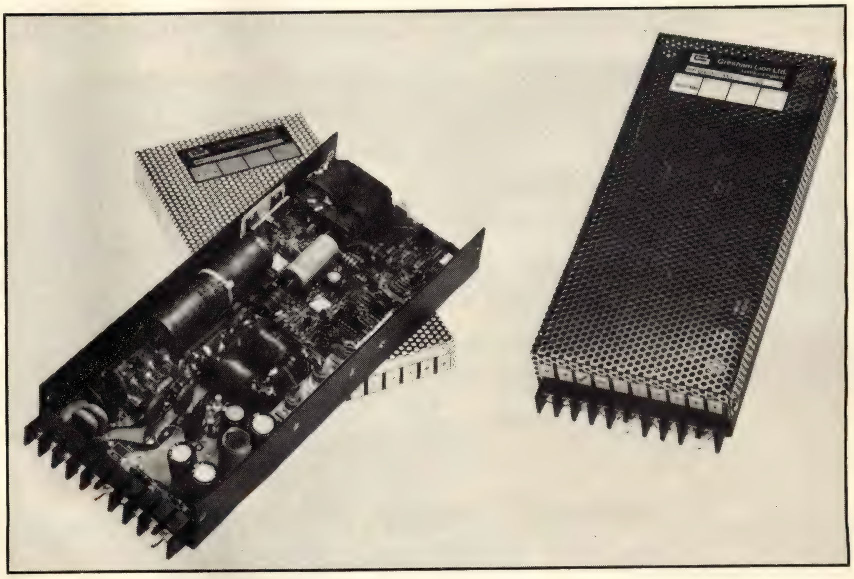
A 228-mm (diagonal) screen can be used both for program development and for displaying measurement results in graphic or tabular form. A cursor can be moved to any position on the screen by means of X and Y direction keys.

A standardized IEC-bus interface helps connect the PPC to other test-system components, such as measuring instruments and control units, and to such peripherals as external memory, printers and plotters. A standard Centronix interface ensures direct connection to a printer.

Rohde & Schwarz GmbH, Muhldorfstrasse 15, Postfach 80 14 69, D-8000 Munich 80, West Germany. (089) 41292625. Telex: 523703.

CIRCLE NO. 501

Switching-supply series offers 40 choices



An ideal switching power supply can now be selected from one source without compromise; over 40 different single and multi-output versions are available from Gresham Lion's GOS series.

The output power ratings of the units range from 100 to 250 W and all popular output voltages from 5 to 48 V dc are offered. Current ratings of up to 50 A can be specified for single-rail units. Each open-frame supply is available with up to four separate output rails. Typical operating efficiencies range to 75%, the result of the switching design. Brownout, short-circuit and overvoltage protection are standard in all units, as is special "soft start" circuitry to limit load surge currents.

Line regulation is ±0.1% for a full input swing while load regulation (from half to full load) is ±0.2% for the main output rail and ±2% on auxiliary rails when the main rail is held constant.

Gresham Lion, Gresham House, Twickenham Rd., Feltham, Middlesex TW13 6HA, England. 01-894-5511. Telex: 27419.

CIRCLE NO. 502

Desktop computers get flexibility from disks

Four desktop microcomputers from Ai Electronics use double-sided, double-density floppy-disk drives to increase their operating flexibility. Moreover, they offer a variety of data-entry and storage options.

Models ABC-21, 24 and 25 use 5-1/4-in. disks while the ABC-26 handles 8-in. disks. The ABC-21 has a 9-in. CRT screen while the other three use 12-in. CRTs.

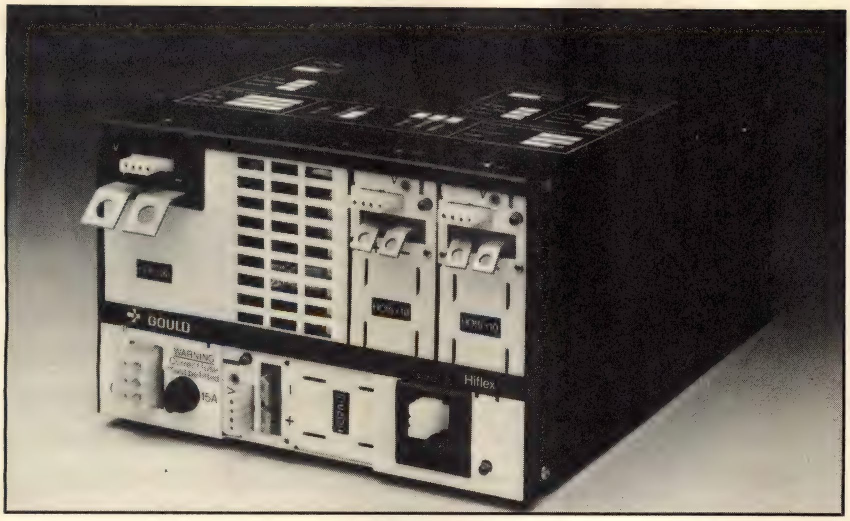
All four models use a Z80A microprocessor on a single-board computer. Options include printers, light pens, Winchester drives, cartridge drives and paper-tape readers.

All four models also have separate RAM for CRT display refresh, which shortens CPU execution times. In addition, their keyboards, which have 101 keys and may be detached from the displays for more convenient use, are easy to modify to accommodate different languages.

Software for the series includes disk operating systems, Basic-2 Basic-2G (for GPIB support), CP/M 2.0 and 2.2, Pascal II.0A, Cobol 3.0, PL/3 and data-communications support software.

Ai Electronics, 2-28-16, Shimomaruko, Ohta-ku, Tokyo 146, Japan. 03-756-4111. Telex: 246-6176 aielec. **CIRCLE NO. 503**

Modular power supplies vary to suit requirements



Over 1800 variations of the Hiflex power supply system help shorten design lead times and allow quick large-volume delivery of custom units. The modular systems have a standard fan-cooled input unit in common and are individualized by a selection from six independent output modules.

The basic unit is available in 400, 600 and 750-W power ratings. The input unit accepts the mains supply, filters out transients and prevents feedback of electrical noise into the power lines. A low-loss, high-efficiency circuit converts the input into a high-frequency (30-kHz) signal suitable for driving the output modules. The output modules then convert this signal to a stable dc voltage using a magnetic-amplifier feedback technique.

The Hiflex system is designed to meet IEC435, VDE0730 and UL478 specifications.

Gould Electronic Power Supply, Raynham Rd., Bishop's Stortford, Hertfordshire CM23 5PF, England. (0279) 55155. Telex: 81510.

CIRCLE NO. 504

Only TEAC makes both on-site and in-lab cassette data recording equipment.

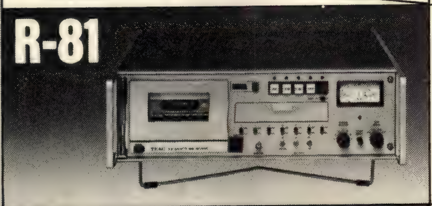
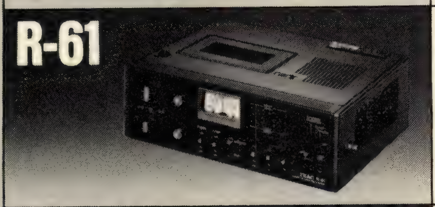
Have you been going to one manufacturer for your portable data recorders, and to another for recorders for your lab? TEAC makes things easier for you by offering a complete line of data acquisition equipment including both portable and lab models. Complete compatibility allows you to collect data in the field with a convenient portable recorder and bring it back to the lab for analysis on a full-feature lab recorder.

Of all our models, you'll find that our cassette-format recorders are the most convenient. The R-60, R-61 and R-61D portable cassette data recorders have proven extremely popular because of their ruggedness, stability of operation and light weight. They can record four channels of data in a choice of DR or FM format.

Back in the lab, the R-80 and R-81 provide big-recorder performance and features without using up a big amount of space or budget. Both can be mounted in standard E.I.A rack panels if desired.

These five cassette data recorders are part of a complete line of data acquisition equipment. Only TEAC can handle *all* your data acquisition needs.

Feature Comparison Chart

Feature Model	Channels	Record System*	Tape Speed	Freq. Response	Power	Weight
R-81 	7	FM (DR: option)	4 speeds (7½, 3¾, 1⅞, 15/16ips)	FM: DC – 5k Hz at 7½ips	DC Car Battery (AC with AD-80)	12kg approx.
R-80	4	FM (DR: option)	4 speeds (7½, 3¾, 1⅞, 15/16ips)	FM: DC – 5k Hz at 7½ips	DC Car Battery (AC with AD-80)	12kg approx.
R-61 	4	Ch-1: FM/DR Ch-2: FM/DR Ch-3: FM Ch-4: FM	1 speed (1⅞ips)	DR: 50 – 8k Hz FM: DC – 625 Hz	DC Car Battery with CL-61 (AC with PA-2)	4.7kg approx.
R-61D	4	Ch-1: DR/FM Ch-2: DR/FM Ch-3: DR Ch-4: DR	1 speed (1⅞ips)	DR: 50 – 8k Hz FM: DC – 625 Hz	DC Car Battery with CL-61 (AC with PA-2)	4.7kg approx.
R-60	4	FM	1 speed (1⅞ips)	FM: DC – 625 Hz	AC	6.5kg approx.

* Noise Comp. & Memo capable

TEAC

TEAC CORPORATION: 3-7-3 Naka-cho, Musashino, Tokyo, Japan Tel: (0422) 53-1111

●U.S.A. B.J. Wolfe Enterprise Inc., Tel: (213) 877-5518 ●Canada R.H. Nichols Co., Ltd., Tel: (416) 661-3190 ●Hongkong Dah Chong Hong Ltd., Tel: 5-261111, 5-226258 ●Australia & New Zealand Jacoby Mitchell Ltd., Tel: 6307400 ●South Africa Mayfair Sales (Pty) Ltd., Tel: 011-834-2131 ●Belgium & Luxemburg Simac Electronics S.P.R.L., ●Denmark Danbit, Tel: (03) 141515 ●France Tekelec Airtronic S.A., Tel: (027) 7536 ●Holland Simac Electronics B.V., Tel: 040-533725 ●Italy A.E.S.S.E. S.R.L., Tel: 54.64.741-2-3 ●Switzerland Wenger Datentechnik, Tel: 061-34 50 96 ●Spain Ataio Ingenieros S.A., Tel: (215) 3543 ●Sweden teleinstrument ab, Tel: 08-380 370 ●United Kingdom International Recorders Ltd., Tel: 04427 5959 ●West Germany & Austria nbn Electronik Starnberg, Tel: (08151) 13036

CIRCLE NO. 153

Capacitance box spans 100 pF to 10 μF

Beta-Cap, a capacitance decade box, offers 100 calibrated positions from 100 pF up to 10 μF, with a resolution of 100 pF for each position set. Capacitance values in each decade are set by four slide switches. The unit's die-cast aluminum case measures 110 × 115 × 40 mm.

Betatron Svenska AB, Box 8181, 163 Spånga, Sweden 08/761 00 20

CIRCLE NO. 505

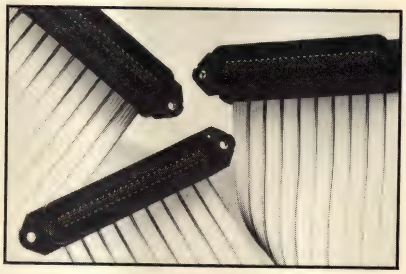
Programmable oscillator gives 225 frequencies

A single programmable oscillator module, part of the PG series, produces up to 225 frequencies from one source. Signals from built-in basic oscillators are divided or combined to generate the multifrequency output. Model PG-101 supplies sinewaves from 457.5 to 1267.5 Hz; PG-102, 352.5 to 997.5 Hz; PG-103, 952.5 to 1912.5 Hz. All three modules generate square waves from 7.5 to 1912.5 Hz. Power requirement is 9 V at less than 40 mA. Frequency accuracy is less than 100 ppm. Load resistance is 600 Ω.

Fuji Electrochemical, 5-36-11, Shinbashi, Minato-ku, Tokyo 105, Japan. 03-434-1271.

CIRCLE NO. 506

Connector terminates ribbon cables



Champ latch connectors offer a fast, reliable means of mass terminating 1.27-mm center-line ribbon cable. The connectors also convert from ribbon cable within equipment to circular cable. Standard 14, 24, 36, 50 and 64-way versions are offered. The Champ connector terminates both solid and stranded ribbon cable using an insulation displacement technique. The connector is compatible with other connectors of similar design and is mateable with any other Champ connectors, including the British Post Office approved PO 226, which meets the D.2635 specification.

AMP of Great Britain, Terminal House, Stanmore, HA7 4RS, England. 01-954-2356.

CIRCLE NO. 507

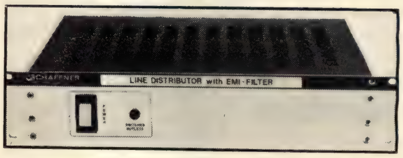
Prescaler chip divides from GHz range

Designed for use in digital frequency division and high-frequency up-conversion, the CA3179G IC divides frequencies as high as 1.25 GHz. The chip operates from a single 5-V supply and has a dissipation of only 325 mW. The prescaler divides by 256 in its UHF mode and by 64 in the VHF mode. Either single or double-ended inputs can be applied. Sensitivity is typically 15 mV rms at 900 MHz. The output of the CA3179G is a complementary emitter-coupled stage capable of driving a 33 pF or equivalent load.

RCA Solid-State-Europe, Sunbury-on-Thames, Middlesex TW16 7HX, England. Sunbury-on-Thames 85511. Telex: 24246.

CIRCLE NO. 508

Line distributor suppresses EMI



A rack-mount line distribution system, FR 400, suppresses symmetrical and asymmetrical interference by more than 70 dB over a 150 kHz to 300-MHz range. The system uses built-in EMI filters. Six outlets are provided on the back panel; four of the six outlets can be remotely controlled. The distributor is rated at 10 A and can be used to distribute power to peripheral equipment.

Hans Schaffner AG, 4708 Luterbach, Switzerland. 065-423-131.

CIRCLE NO. 509

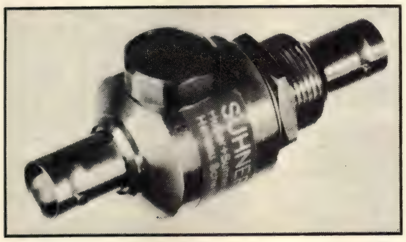
Reversible jaws clamp PC boards

A multi-purpose clamp work holder securely grabs PC boards in its reversible jaws. One side of the jaws has a series of holes to grip objects from 1 mm in diameter (such as component leads) up to 20 mm in diameter. The reverse side is serrated to firmly hold PC boards and other flat items. The clamp is mounted to a universal joint which allows 360° rotation and 180° tilt. The clamp is detachable from its metal stand. Metal and soft nylon jaws are supplied as standard.

Tele-Production Tools, Stiron House, Electric Ave., Westcliff-on-Sea, Essex SSO 9NW, England. (0702) 352719.

CIRCLE NO. 510

Inline protector limits surges



Series 3401 EMP protectors limit surge voltages in coaxial systems. The devices consist of a section of coaxial line with a surge protector mounted directly between the inner and outer conductor. Dangerous surges, induced by lightning strokes, etc. spark over the gas-filled protector in 3 ns typical, allowing the current to flow to ground. VSWR is only 1.3 at 900 MHz while attenuation is only 0.05 dB typical.

Huber and Suhner, CH-9100 Herisau, Switzerland. 071 53 15 15. Telex: 77 426.

CIRCLE NO. 511

Open-frame switchers replace linear types

LMG Series open-frame, switching power supplies replace linear supplies in applications requiring a supply with less weight, smaller size and less heat dissipation. Single and triple-output versions are available. All outputs are fully regulated. Operation from 120 or 240 V ac is selected at the input. Regulation is 0.6% for line and load; ripple, 50 mV pk-pk maximum. Transient response is 5% maximum for 50% load change. Regulation is restored within 500 μs.

ITT Instrument Services, Edinburgh Way, Harlow, Essex, England. (0279) 29522. Telex: 81525.

CIRCLE NO. 512

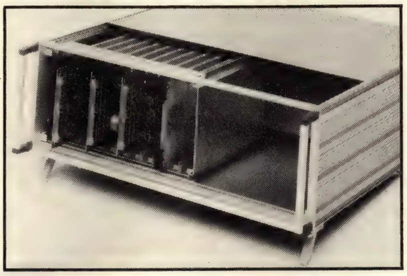
Op amp stands tall in military service

A precision operational amplifier, the 3510VM/MIL, offers military users very low drift characteristics over a −55 to +125 C range. Voltage drift is less than 2 μV/°C. In addition, laser trimming results in an initial input offset voltage, at 25 C, of less than 120 μV. Open loop gain is 120 dB minimum; common mode rejection, 110 dB; input bias current, less than ±25 nA.

Burr-Brown International, Cassiobury House, 11-19 Station Rd., Wetford, Herts. WD1 1EA, England. (0923) 33837. Telex. 922481.

CIRCLE NO. 513

Easy-to-assemble frame holds PC boards



An easy-to-assemble card frame, Type 13, allows vertical or horizontal insertion of PC boards. The frame is made of aluminum sections with removeable top and bottom covers. The frame can be assembled in any height, width or depth specified by DIN standard 43 700. For insertion of European-size cards measuring 100 × 160 mm, a special inner frame is supplied. Only a few bolts are required for assembly of the entire frame. Small plastic holders, pressed into slots in the side panels, allow vertical or horizontal mounting of print plates.

Jendee Trading, 4 Bamborough Gardens, London W12 8QN, England. 017 490853.

CIRCLE NO. 514

Mini CRT works in portable cameras

A high-resolution, miniature viewfinder CRT produces bright, sharp pictures, even at the corners. Based on CRTs developed for military helmet-mounted display systems, the new CRT, the 08C/117, is suitable for direct view without the need for a magnifier. Useful screen area is 60 × 45 mm; tube neck diameter, 14 mm. The tube operates at a final anode voltage of 7 kV and fully resolves a 625-line picture. The light output from the type T4 phosphor is high enough for normal outdoor operation.

Thorn Brimar, Gem Mill, Chadderton, Oldham OL9 8NP, England, 061-624-0515.

CIRCLE NO. 515

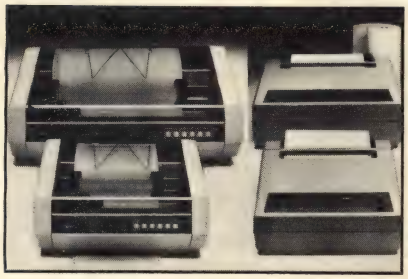
Meter goes digital for analog price

A pocket-sized, 3-1/2 digit multimeter, the 8022A, provides digital capability at an analog price. The LCD instrument is rugged and can withstand 6-kV transients of 10-μs duration. Functions include high and low-power ohms. Autozero and autopolarity are standard. Operating temperature range is 0 to 50 C. Battery life is up to 200 h.

ITT Instrument Services, Edinburgh Way, Harlow, Essex, England. (0279) 26811. Telex: 81146.

CIRCLE NO. 516

Low-cost printers meet high printing demands



A family of low-cost printers, 4520, 4521, 4525 and 4526, match the needs of low-noise, continuous operation and high print quality applications. Models 4520 and 4521 have 80-column formats with a 9 × 7 dot matrix. The 4520 uses friction feed for journal rolls while the 4521's pin feed suits continuous forms. Models 4525 and 4526 print 150 char/s with a 9 × 9 dot matrix and true descenders. Formats are 80-columns for the 4525 and 132 columns for the 4526. Serial and parallel interfaces are standard. Various European language versions are available.

Facit Data Products, S-105 45, Stockholm, Sweden. 08-738 73 68. Telex: 11600 elhead s.

CIRCLE NO. 517

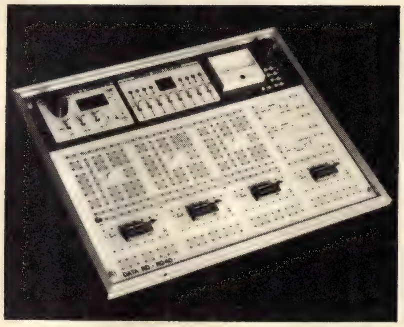
Two chips simplify synthesizer design

A frequency-generating circuit, using just two chips, simplifies the design of synthesizers for radio applications. The circuits are intended for use in low-power hand-held equipment, general-purpose applications up to 500 MHz and use in equipment operating at up to 1 GHz. Each application requires one bipolar high-speed divider and one NMOS control circuit. The synthesizers interface directly with memories and microprocessors. The SP 8901 and its controller, the NJ 8811, operate at up to 1 GHz. Current consumption is 100 mA at 5 V. SP 8906 and NJ 8811 work in 500 MHz circuits and draw 80 mA from a 5-V supply. In equipment for 200 MHz, the SP 8793 and NJ 8812 require only 12 mA at 5 V.

Plessey Semiconductors, Kembrey St., Crowdy's Hill Estate, Swindon SN2 6BA, England.

CIRCLE NO. 518

Simulator aids circuit designing



An electronic simulator, RD40, contains the power supplies and test equipment to assist circuit prototyping and design. Four supplies, a function generator, a frequency meter, hexadecimal displays and an electronic chopper allow analysis of digital circuits. Several models are offered, including one with a logic analyzer to determine circuit status.

Data Recherche et Development, 21, rue Florian 26000 Valence, France. (75) 42-27-25.

CIRCLE NO. 519

Transducers monitor differential pressure

Differential pressure transducers, BHL-4301 and BHL-4305, measure fluid pressures with respect to clean, dry, non-corrosive gas reference pressure. The compact stainless-steel parts are available for uni or bidirectional measurement from 35 millibar up to 10 bar in the presence of common line pressures extending to 35 Bar.

Bell & Howell Electronics and Instruments, Lennox Rd., Basingstoke, Hampshire RF22 4AW, England. (0256) 20244.

CIRCLE NO. 520

Call IC contains coder/decoder on chip

A selective-call IC, the CZN 139, contains both an encoder and a decoder on one chip. The circuit operates in paging systems and alarm circuits via radio, telephone lines or alarm lines. Keyboard entries are made at the sending location with the chip providing a digital display output of the numbers entered. The receiver portion displays the code of the calling station. Up to three incoming codes can be stored. The chip compares an incoming code against those stored in its memory. The chip uses CMOS circuitry for low power consumption.

Medel, P. O. Box 135, 9300 AC Roden, The Netherlands, 05908-18941.

CIRCLE NO. 521

Pin locks handles to PC boards

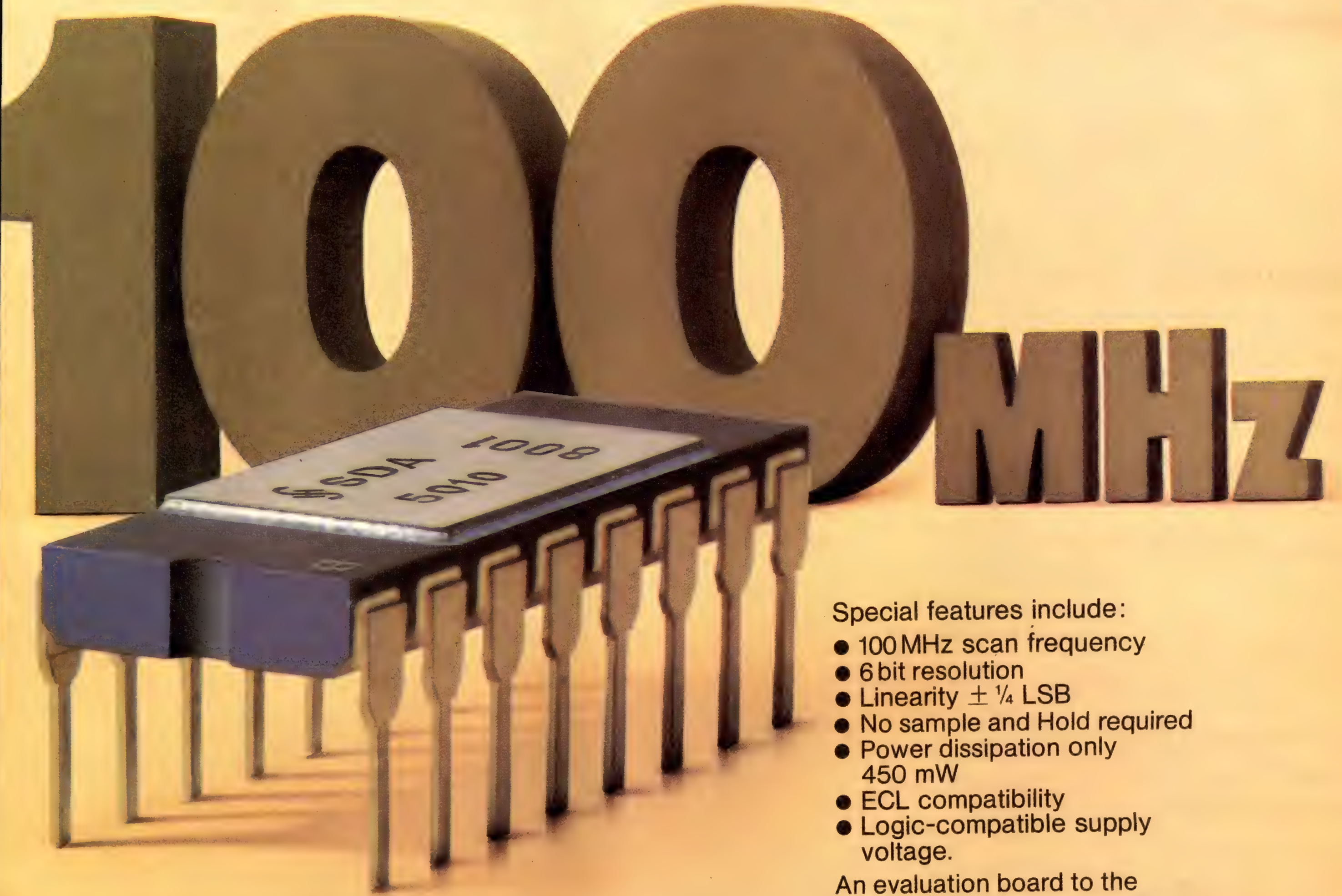
A range of PC-board handles are securely locked to a board without the use of nuts and bolts. A retaining pin is inserted through a hole in the handle and through a corresponding hole drilled into the board. The handle can be fixed permanently in position by use of a soldering iron. The pin is simply softened with the iron and its pins are spread for a permanent fit.

Sangria Designs, Garland Works, Desborough Ave., High Wycombe, Bucks HP11 2RN, England. (0494) 28914.

CIRCLE NO. 522

SIEMENS

In Ten Nanoseconds from Analog to Digital



Special features include:

- 100 MHz scan frequency
- 6 bit resolution
- Linearity ± ¼ LSB
- No sample and Hold required
- Power dissipation only 450 mW
- ECL compatibility
- Logic-compatible supply voltage.

An evaluation board to the SDA 5010 is, of course, available.

In only 10 billionths of a second it converts analog signals into digital 6-bit words. This is the new extraordinary device from Siemens – the SDA 5010.

It's the first 6 bit/100 MHz A/D converter in bipolar, monolithic technology, it's reasonably priced, and its applications range from radar, ultrasonics and instrumentation to X-ray and medical engineering.

And that's only half of it. This device has many other technical refinements. Find out about them from Siemens AG, Components Group, ZVW 104, Postfach 103, D-8000 Munich, quoting "Integrated A/D Converter".

B 8008.101

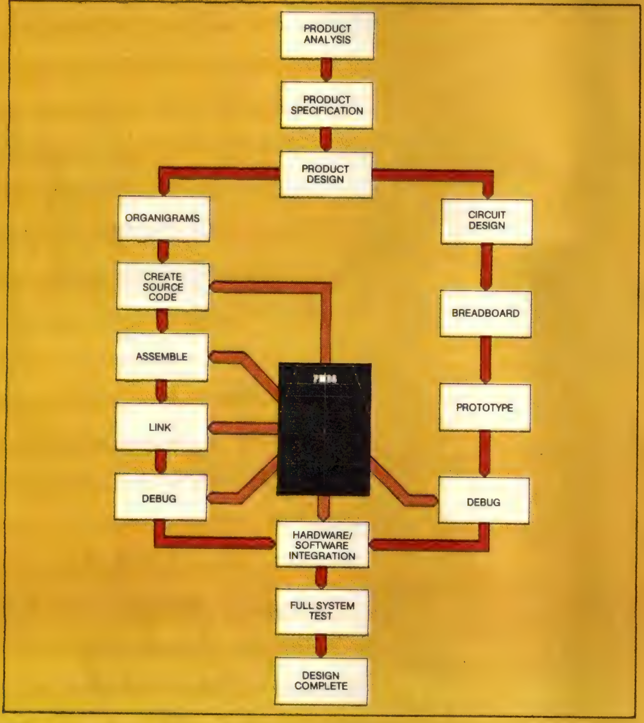
The ultrafast, integrated A/D converter from Siemens

new '80

CIRCLE NO. 154

Microcomputer imple
the direct route
Philips Microcomputer Develo

In the development of new microcomputer applications, the Philips MDS - Microcomputer Development System - can help you take the direct route to successful, economic system implementation. By shortening your development lead-time, PMDS helps you maintain your competitive edge. And by greatly reducing the man-hour input needed to realize your system, it helps you minimize your overall development costs. Another important cost-cutting factor is the easy-to-learn, interactive PMDS software providing full operator guidance and eliminating start-up delay.



True system emulation
Using PMDS, your hardware and software engineers can work closely together throughout each development phase. Testing and debugging can be carried out even before prototype hardware is available, thanks to PMDS' true real-time system emulation capability. Your complete system - hardware and software - can be exercised under actual operating conditions before you make any production commitments. As a result, integration of hardware and software into your final system is quick and problem-free, because both elements are designed and tested together right from the start.

The universal system
PMDS has the essential flexibility to take technological advances in its stride. If you want to take advantage of new microcomputer developments, or if your next project calls for a different chip, PMDS leaves the choice open. Because PMDS was designed as a universal system, it can simply and economically be adapted by a range of Microcomputer Adaptor Boxes (MABs) for all the most important microcomputer systems. So you won't be committed to any single supplier who may not have the new technology you need, or who can't give you the right price/supply conditions.

Philips - your system partner
As Europe's leading manufacturer of electronic instrumentation of all kinds - both analogue and digital - we have extensive experience of all aspects of product testing and development. In addition, we are both a major manufacturer and user of microprocessor and microcomputer products. So we know the problems that arise in developing these systems, and how best to approach and solve them. With PMDS, you can benefit from our experience in applying computer technology to microcomputer development.

For further information about PMDS, contact

Philips Industries, Test and
Measuring Instruments Dept.,
TQ III-2-51, Eindhoven,
The Netherlands.

PHILIPS

Test & Measuring
Instruments

mentation -

nent System

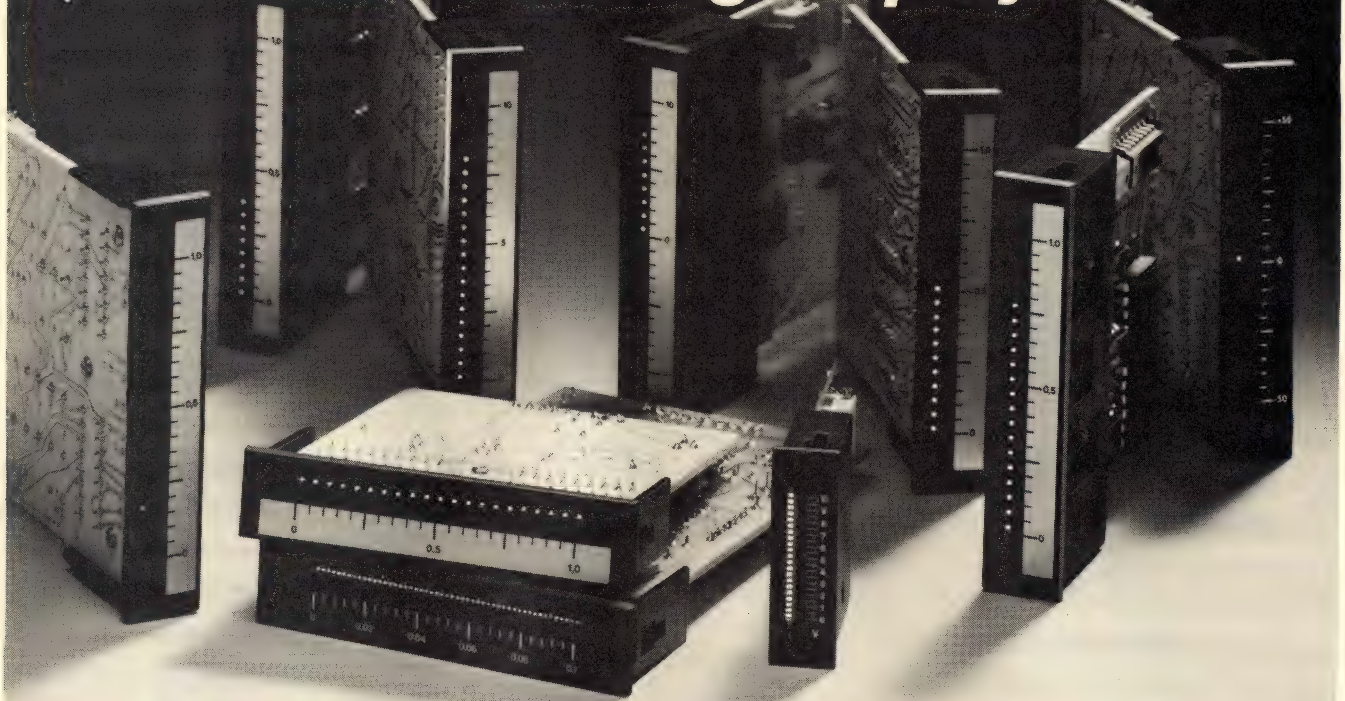
From Philips, of course

PHILIPS

CIRCLE NO. 155

contraves

The new trend: LED-Line by Contraves, the solid state analog display



Today, there is hardly a real alternative to LED components. This applies to analog displays as well. That's why we developed the LED-Line.

These compact panel units feature bright displays with numerous advantages.

Whether you want to display or observe monitoring or tuning operations, one glance is enough to see the results, even several results simultaneously. The units are compact, mount horizontally or vertically, and can be read in darkness, too. Whether your input is analog or digital, LED-Line *is ready for wiring. That's the new trend.*

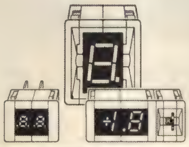
Some technical data:

- *21 and 51 light points*
- *Resolution up to 2%*
- *Bar or floating dot display, even selectable*
- *Zero point offset*
- *Measures positive and negative input voltages*
- *High input impedance*
- ***Analog:** input sensitivity 100 mV FS*
- ***Digital:** up to 6 bit binary, TTL*

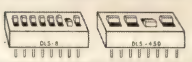
Choose from a line of 14 standard types off the shelf. Send for our brochure.

Further Contraves products

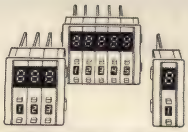
Contraves Multiswitch, *thumbwheel switches*



Contraves Codicount, *7-segment LED displays*



Contraves DIP-Switch, *dual in-line switches*



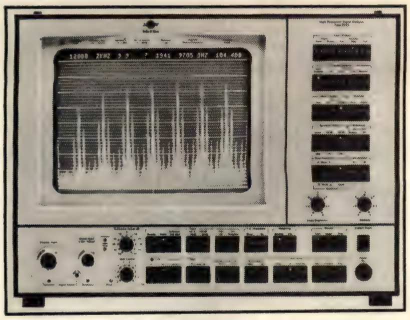
Contraves Multicount, *switch/display modules*

contraves *Contraves AG, Schaffhauserstrasse 580, Postfach, CH-8052 Zürich, Telefon 01/306 22 11*
Contraves Industrial, Products Ltd., Times House,
GB-Ruislip/Mddx HA4 8LH, Telefon (08956) 30 196

Subsidiaries: Germany: Contraves GmbH, D-8013 Haar/München, Italy: Prodotti Industriali Contraves S.r.l., I-20 133 Milano, Japan: K. K. Codix, 1-9-15 Kaigan, Minato-ku, J-Tokyo

MA/3/80

Added memory gives zoom to signal analyzer



An enlarged input memory capable of holding 10,240 samples of a time signal gives added advantages to a high-resolution signal analyzer, Type 2033. The increased memory provides a nondestructive zoom function, scan analysis and alias-free tracking. In contrast to conventional zoom transforms, the time function is preserved to allow multiple zooms on the same data. This makes the Type 2033 faster than an FFT analyzer processing conventional zoom transforms.

Bruel & Kjaer, 18, Naerum Hovedgade, 2850 Naerum, Denmark. (45,2) 80 05 00. Telex: 37316 bruka dk.

CIRCLE NO. 523

Telecomm cable uses 216 optical fibers

A telecommunications cable uses 216 optical fibers. The fibers are available with attenuations from 3 to 8 dB/km and bandwidths from 300 to 1000 MHz/km. A polyethylene cable sheath, reinforced with glass fibers, provides high tensile strength and good protection for the fibers. Cable diameter is approximately 45 mm.

Felten & Guilleaume Carlswerk AG, 5000 Köln 80 (Mülheim), Federal Republic of Germany. (0221) 676 (1). Telex: 08873261 fug d.

CIRCLE NO. 524

Protocol converter adapts dumb terminals

A protocol converter, the PDS 202, allows use of dumb asynchronous ASCII video terminals and printers as 3270 terminals. The device, a microprocessor-based unit, replaces a 3271 cluster controller for binary synchronous 3270 users. Up to sixteen asynchronous terminals can be attached, either locally or remotely, via the PSTN, to provide dial-up access for 3270 users on a single-user basis. Software can be held on an integral floppy disk memory system or stored in read-only memory. The device is available in card-only form for incorporation into standard terminals.

Nolton Communications, Fieldings Rd., Cheshunt, Herts. EN8 9TL, England. Waltham Cross 33555.

CIRCLE NO. 525

Contact your Electronic Design representative

For Rates and Dates-call, write, twx:

UNITED KINGDOM, SCANDINAVIA
Constance McKinley
50 Essex St., Rochelle Park, NJ 07662
Phone: (201) 843-0550; TWX: 710-990-5071

BELGIUM, HOLLAND, SWITZERLAND
W.J.M. Sanders, S.I.P.A.S.
Raadhuisstraat 24-P.O. Box 25
1484 EN Graft-de-Ryp, Holland
Tel: 02997-1303 and 3660
Telex: 13039 SIPAS NL
Telegrams: SIPAS-Amsterdam

FRANCE
Annick Wolff, Promotion Presse Internationale
7 ter Cour des Petites Ecuries
75010 Paris, France; Tel: 247-12-05

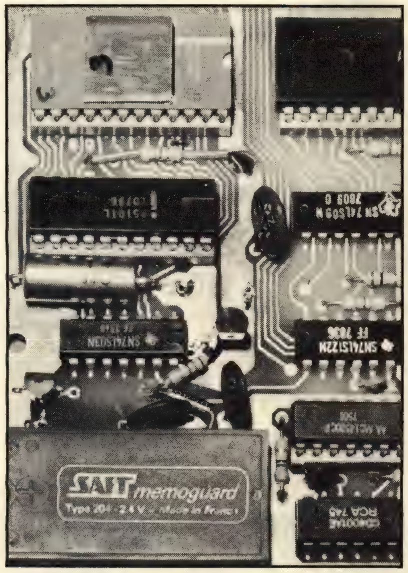
ITALY
Robert M. Saidel, Technimedia International
Piazzale Cadorna 4, 20123 Milan, Italy
Tel: 80 16 46: Telex 25897 Utidioma

GERMANY
Annemarie McCalla
50 Essex St., Rochelle Park, NJ 07662
Phone: (201) 843-0550; TWX: 710-990-5071

TOKYO
Haruki Hirayama, EMS, Inc.
5th Floor, Lila Bldg., 4-9-8 Roppongi
Minato-ku, Tokyo, Japan; Phone: 402-4556
Cable: EMSINCPERIOD. Tokyo

ElectronicDesign

Sealed NiCd modules support on-board RAMs



Dual-inline packaged Memoguard modules provide dependable backup power for PC-board mounted RAM. The modules are nonflammable and solvent resistant and are compatible with standard soldering and cleaning processes. Two sizes (40 and 100 mAh) and two voltages (2.4 and 3.6 V) are available. The modules offer total immunity against accidental leaks through the use of seals and encapsulation. Height above a board is only 0.35 in. Charging current is drawn from the on-board supply.

Saft, 156, Avenue de Metz, 93230 Romainville, France. 843.93.61. Telfex: 220100.

CIRCLE NO. 526

Captivation design aids SMA performance

A captivation design for SMA connectors improves device reliability while providing better rf performance. Epoxy resin is used to captivate the inner conductor in the insulator. Four indentations around the connector body prevent axial and radial displacement of the insulator/contact assembly. The result is no rf leakage through the *outer body*, no axial or rotational displacement of the contact and insulator and low VSWR, even at frequencies to 26 GHz.

Huber & Suhner, CH-9100 Herisau, Switzerland. 071 53 15 15. Telex 77 426.

CIRCLE NO. 527

Inkless chart recorder writes in any position

A temperature chart recorder, Model M2115, uses pressure-sensitive chart paper, allowing it to operate in any position. The unit provides a high-impedance input amplifier, permitting its use with a wide selection of plug-in range cards. Clip-in, interchangeable gear boxes allow a wide variety of chart speeds. The unit is calibrated for iron/constantan or

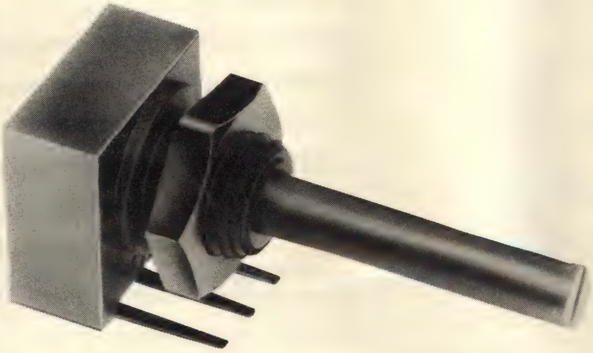
A new PANEL CONTROL
from DIPLOHMATIC

for direct mounting in
printed circuit board

World needs a DOC-TRIM

DOC diplohmatic a/s, Rugmarken 11,
DK-3520 FARUM, DENMARK
Phone +45 2 951677-Telex 37278 matic dk

CIRCLE NO. 157



R7-EP
The professional
Key-Switch

The switches in the R7-EP-series, are panel mounted, designed for use in professional electronic keyboards. cash-registers, high quality calculators and other general control functions in computers and terminals.

- Automatic soldering
- Insensitive to dust and damp
- Sealed reed switch
- Over 25 million operations
- R7-SP–for stepped keyboards

Wirsbo Elektronik AB
Box 20505, S-104 60 STOCKHOLM, SWEDEN
Phone +46 8-743 08 45, Telex 10686

CIRCLE NO. 158

chromel/alumel thermocouples. Accuracy is ±2% of span. Input power is 197 to 255 V at 50 Hz. The recorder measures 92 × 143 × 152 mm and weighs 1.6 kg.

Channel Electronics (Sussex) Ltd., P.O. Box 58, Seaford BN25 3JB, Sussex, England. Seaford (0323) 894961. Telex: 877825.

CIRCLE NO. 528

Potted supplies provide on-board logic power

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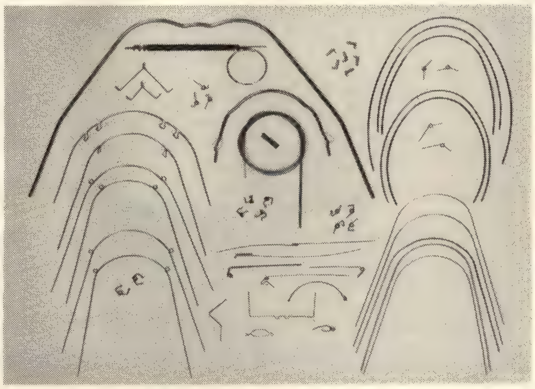

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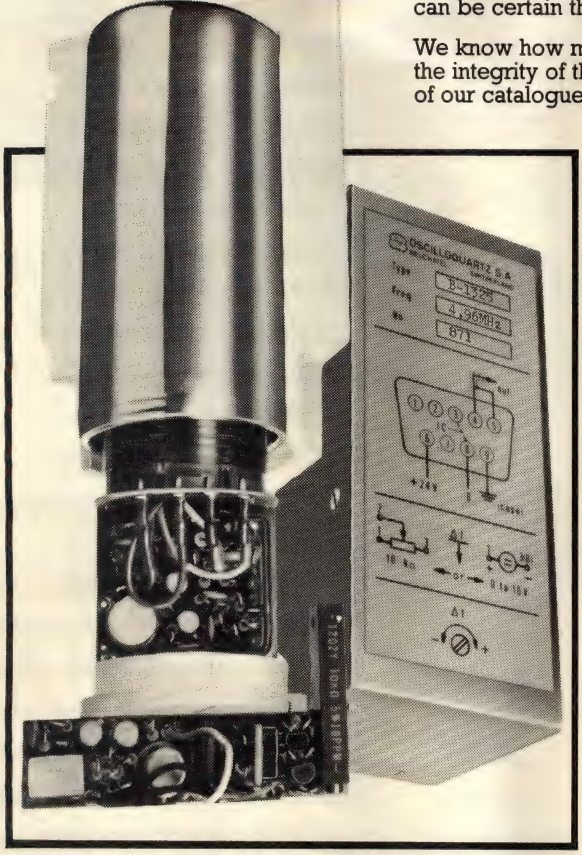

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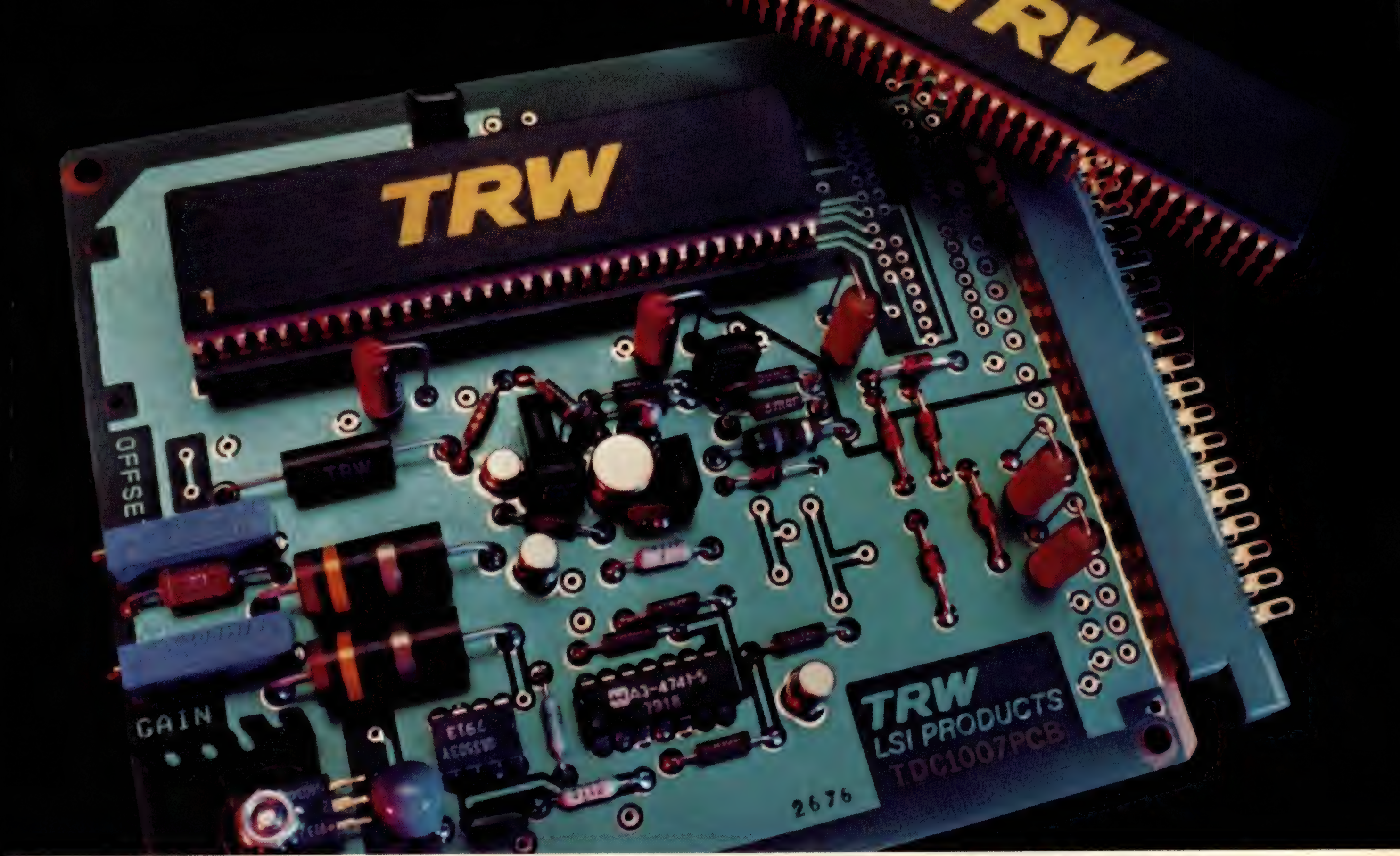

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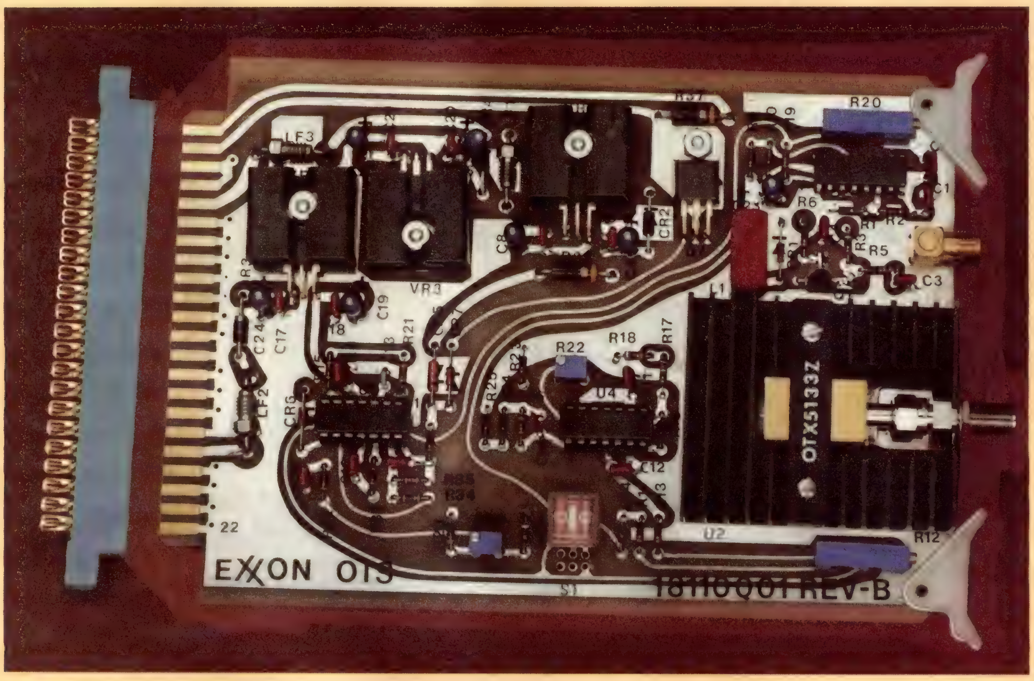

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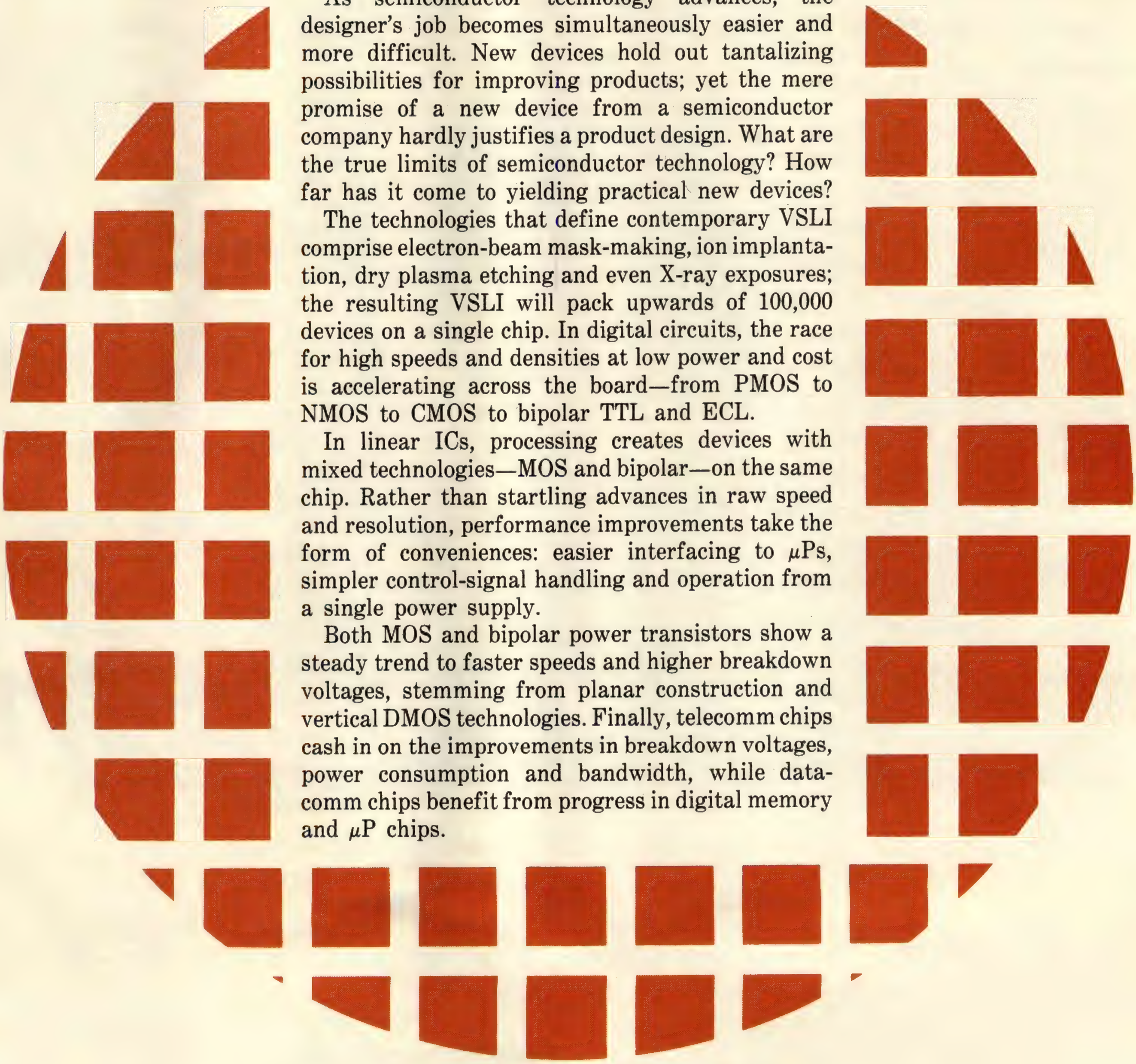
Semiconductor technologies: No limits in sight

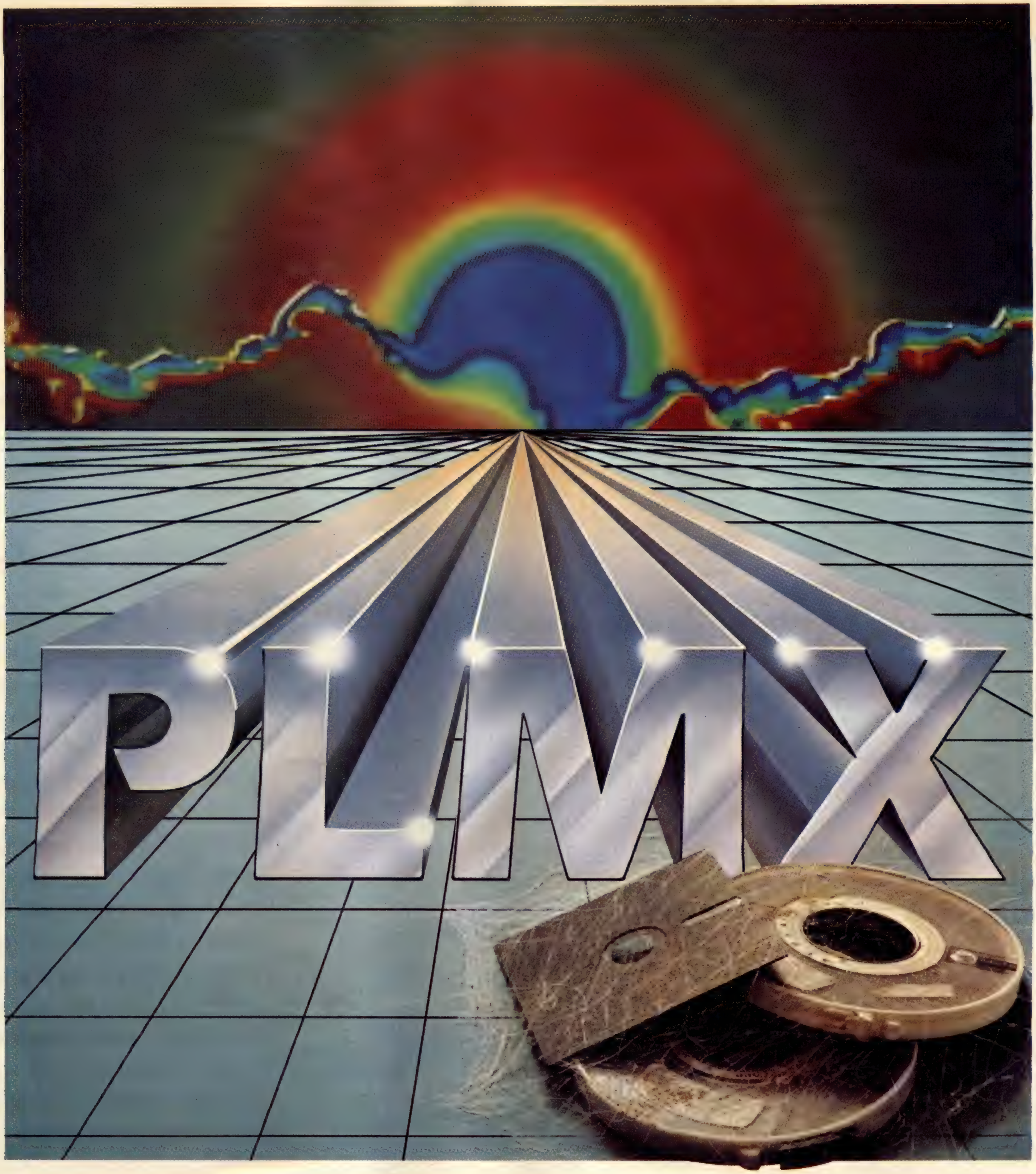


As semiconductor technology advances, the designer's job becomes simultaneously easier and more difficult. New devices hold out tantalizing possibilities for improving products; yet the mere promise of a new device from a semiconductor company hardly justifies a product design. What are the true limits of semiconductor technology? How far has it come to yielding practical new devices?

The technologies that define contemporary VSLI comprise electron-beam mask-making, ion implantation, dry plasma etching and even X-ray exposures; the resulting VSLI will pack upwards of 100,000 devices on a single chip. In digital circuits, the race for high speeds and densities at low power and cost is accelerating across the board—from PMOS to NMOS to CMOS to bipolar TTL and ECL.

In linear ICs, processing creates devices with mixed technologies—MOS and bipolar—on the same chip. Rather than startling advances in raw speed and resolution, performance improvements take the form of conveniences: easier interfacing to μPs, simpler control-signal handling and operation from a single power supply.

Both MOS and bipolar power transistors show a steady trend to faster speeds and higher breakdown voltages, stemming from planar construction and vertical DMOS technologies. Finally, telecomm chips cash in on the improvements in breakdown voltages, power consumption and bandwidth, while datacomm chips benefit from progress in digital memory and μP chips.



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CIRCLE NO. 27

Geometries are moving to 1 μm, propelled by advanced fabrication techniques. E-beam lithography, step-and-repeat optical projection, ion-beam implantation and dry plasma etching—all play a role.

E-beams, new processes write a powerful legacy

With basic improvements in seminconductor technology, a hundred thousand devices now fit easily onto a single-chip VLSI, fulfilling a perennial promise from IC makers. During the past years, these improvements in "1-μ technology" have encompassed E-beam lithography, step-and-repeat optical projection, ion-beam implantation, dry plasma etching and, to a lesser degree, X-ray lithography.

E-beam lithography has left the laboratory and is entering the production process—especially for mask making—although it is still too slow for directly writing on wafers in mass production. X-ray lithography has the potential to take full advantage of the fine structures of 1× masks made by E-beam lithography, but many problems block its use on the production floor.

Step-and-repeat optical projection directly onto the wafer has made giant strides because it frees optical systems from the limitations of the small exposure fields needed to get 1-μm (and smaller) resolution. The limitations are overcome by accurate and rapid alignment between the steps, so that large patterns can be built up quickly.

Ion-beam implantation has become a necessity for manufacturing many discrete and IC devices, especially MOS and JFET devices.

Dry plasma etching, stripping and deposition during wafer processing, though now a "household" word, is not yet used as widely as it might be—however, it, too, is making progress.

An absolute necessity

"E-beam writing equipment? We can't do without it," says Court Skinner, manager of National Semiconductor's Solid State Technology Center. "One year ago E-beam was just coming on stream; now it's an absolute necessity for much of our mask

Photo courtesy of Harris Semiconductor

Morris Grossman, Packaging Editor

making." (See ELECTRONIC DESIGN, March 29, 1979, p. 82.) This sentiment is repeated by most major IC makers.

Despite faster writing and reduced overhead (see table in box), the latest E-beam writers take about 250 seconds to handle a fairly complex pattern for a 3-in. wafer surface (versus about 500 seconds last year). While this throughput is excellent for mask making (and even for the direct writing of prototypes and custom devices), E beams need a fivefold improvement before direct writing on wafers in economical for mass production.

Most IC makers hesitate to reveal specific E-beam resolutions, accuracies and throughputs actually attained; they claim the data are proprietary. But Gilbert L. Varnell, manager of Texas Instrument's electron-beam program, says that TI's latest inhouse E-beam system (EBM-II, Fig. 1) attains throughputs of two to four 3-in. masks (or reticles) per hour, at a resolution of 1 to 1.25 μm, with a pattern overlay accuracy of ±0.25 μm. For direct writing, the potential capability is estimated at about fourteen 3-in. wafers/hr for 1 to 1.25-μm minimum geometries.

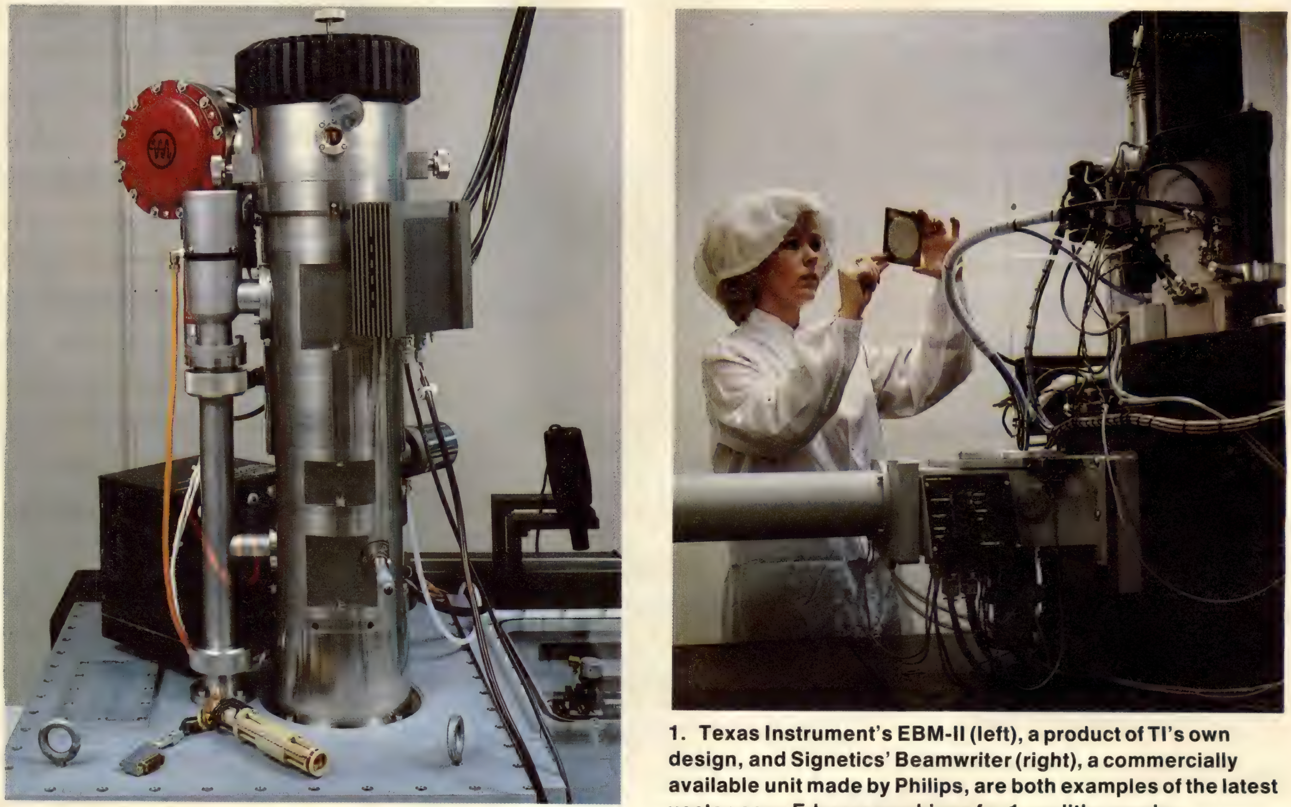
Varnell believes that the EBM-II is merely an interim step to the system that will be required for VSLI device fabrication in the mid-1980s: 0.5-μm resolution, ±0.05 to 0.1-μm pattern-overlay accuracy and 20-slice/hr throughput.

Not all E-beam writers are alike. Two families coexist—vector and raster-scan systems—with several manufacturers for each. Vector-scan types (where each geometrical feature is traced out as a unit) are championed by Texas Instruments, IBM, Philips (Fig. 1), Cambridge Instruments (Fig. 2), Thompson CSF, Electron Beam Microfabrication (EBM) and GCA, among others. (TI and IBM developed the equipment for their own use only.) The simpler raster-scan types (where the geometric features are developed like a TV picture) are offered by ETEC and Varian (Fig. 2) under license from the Bell Telephone Laboratories.

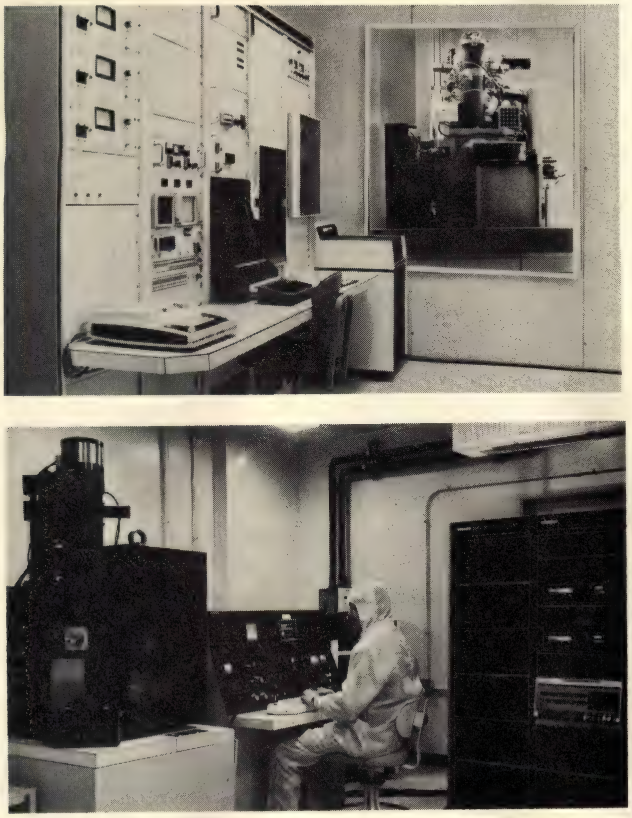
The primary advantage of both types of E-beam units—even the very early raster ones—is their high resolution and fast turnaround time for mask making, mainly because a very time-consuming step can be eliminated from the IC design sequence—the manual fabrication of complex 10× reticles.

The 10× reticle required by conventional optical processing systems is an enlarged optically projectable pattern on a glass plate. It is typically made on an optical pattern generator, and generally requires tedious manual repair and cleanup. The finished reticle must be absolutely free of defects larger than 4 to 5 μm, which show up when the reticle is printed on the final master mask.

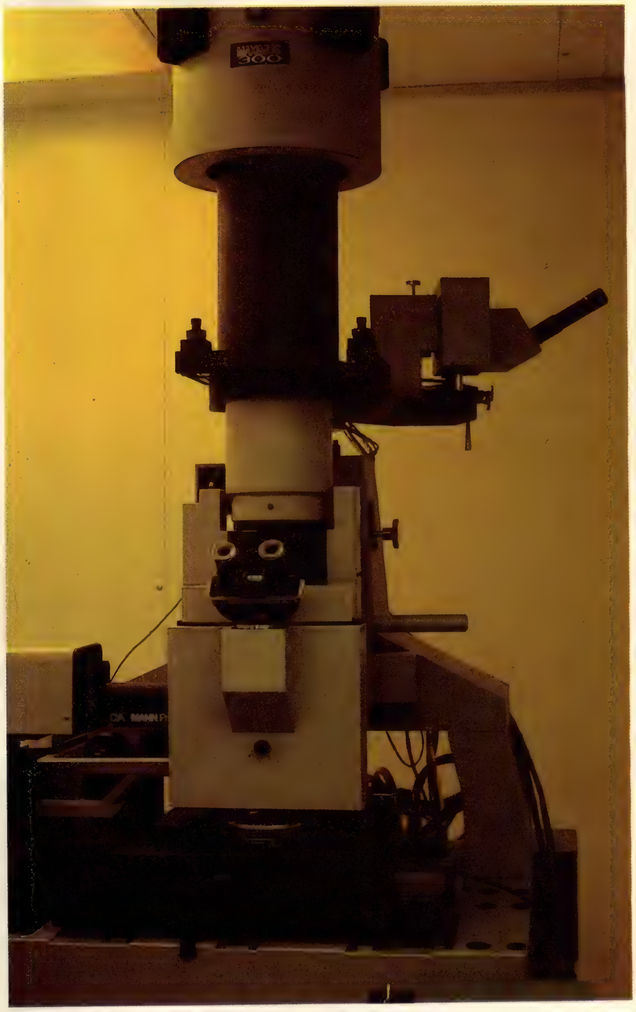
Reticles for the new VSLI chips, with their densely packed features, take more and more time to manufacture, as the chips grow larger. By bypassing this step and going directly from a data-tape or disk to



1. Texas Instrument's EBM-II (left), a product of TI's own design, and Signetics' Beamwriter (right), a commercially available unit made by Philips, are both examples of the latest vector-scan E-beam machines for 1-μm lithography.



2. About $1.7-million buys Varian's latest EeBES-40 raster-scan E-beam writer (top). It has an exposure rate of 5 cm²/min., which can scan a mask for a 4-in. wafer in just 14 min., no matter how complex (or simple) the pattern is. A Cambridge Instrument machine, the EBMF-6 (bottom), which is in operation at Motorola (Phoenix, AZ), is a vector-scan unit that can write 6.4 × 10⁶ exels/s. The time needed to expose a specific wafer size on a vector scanner depends on the complexity of the pattern. However, experts agree that vector-scan units have the potential for higher throughputs than raster-scan machines.



3. Step-and-repeat mask-alignment and exposure systems, such as this unit used by Mostek, make ultrafine geometry possible, by limiting the projector's field of view to small chunks and then accurately aligning them.

a final 1× master mask, the E-beam machine can save hours, or even days, of effort.

The 1× fine-line masks are for contact printing, generally with ultraviolet (or X-rays, where available). They fully exploit the resolution capabilities of the E-beam masks. The wavelength of ordinary light is too long to get through the 1× fine-line apertures of 1 μm or less and still produce a sharp image. (See "Wavelength Limitations and Diffraction Effects," table: 0.72 to 0.4 μm for visible light vs 0.4 to 0.005 μm for ultraviolet.)

Raster scans produce 1× masks *rapidly*

Although the raster-scanning E-beam units have served mainly for the rapid production of precision 1× chrome masks, they can make the 10× reticles for optical step-and-repeat cameras or direct wafer steppers. Bell Laboratories and Western Electric developed the raster-scan method in the early 1970s, but commercial units have been in production for little more than two years. The masks made with these raster machines have been a major tool in the development of many complex ICs, including μPs, RAMs, ROMs and bubble memories.

In raster scanning, the E-beam systematically scans the total exposure field and covers every possible location (address) in the field. The beam is turned off (blanked) where no exposure is needed. The locations are incremental (stepped) and integrally divided according to the machine's addressing bit capability.

Raster scanning places less stringent requirements than vector scanning on the electron beam's deflection system. The user can more easily compensate for distortions from hysteresis and eddy currents in the beam-forming and scanning systems, and the scanning pattern is simple and repetitious. Also, positive and negative images are readily handled, not practical in vector units.

However, vector scanning, which has been commercially available for barely more than a year, has the potential to write three to four times faster than raster scanning. Vector-scan machines are used for making fine-line masks and, to a lesser extent, for direct writing on wafers and for making 10× reticles.

In vector scanning the beam scans only the areas where circuit features are located, not the total field. The beam creates features by filling in the feature with a raster-type motion; varying spot size and shape; or finely outlining the shape's periphery and filling in the outline in large blocks. After a feature is completed, the beam turns off and goes immediately to the next feature. Regions between features are not addressed, and the addressing structure is very flexible.

Since the beam goes directly to features, the writing time depends only on the number of features and the area exposed. Two to three passes may be needed to generate a single feature, with patterns divided into field of 8192 addresses (maximum) on a side.

In the raster-scan, writing time is independent of pattern complexity. Beam-motion rates are faster than with a vector unit because of the regular, simple, scanning pattern. For instance, the Varian Ec-BES-40 has a 40-MHz data rate, but a commercial vector unit made by Cambridge Instrument addresses beam positions at a 2.5-MHz rate. However, the beam in a raster scan must move through many more address points (the Varian machine has a 0.5-μm address structure) than a vector unit. As a result, the vector-scan unit will ultimately write patterns faster, when solutions are found to problems with beam deflection, changes in spot size and high data rates.

For a pattern of moderate complexity, the Cambridge Instruments vector unit can reportedly cover 30% of a 4-in.-diameter wafer with a 1× array pattern in 1.5 to 2.5 hrs. A commercial ETEC or Varian raster-scanning unit does the same job in about 45 min. to one hour—which is, nonetheless, far from the projected potential for the vector-scanning machines.

4. High-energy ion-implantation has found many applications at Motorola. In MOS/LSI fabrication, many products receive four to six different implants at various points in the process. Applications include discrete devices and MOS and bipolar ICs for a variety of purposes, from backside gettering to threshold-voltage adjustment and control.

Some of the problems in a vector machine arise because the target is fixed during E-beam scannings, so the beam must be able to cover the total X-Y exposure area (Z is the beam coordinate)—typically 1 to 5 mm. In a raster machine, the target is also mounted on an X-Y movable stage, but it moves mechanically several millimeters in the X direction, while the beam electronically scans only about 0.25 mm in the Y direction.

For both raster-scan and vector-scan machines, realizing the full potential of E-beam lithography depends on the development of resists optimized for electron exposure. Many laboratories are concentrating their efforts to improve the sensitivity of positive resists—negative resists generally have higher sensitivity and throughput—and to develop negative resists with the resolution, sharp edges and contrast of positive resists.

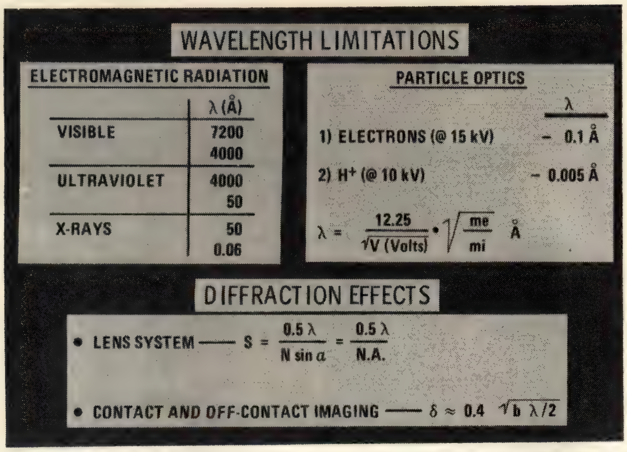
These electron-sensitive resists, like ultraviolet photoresists, are polymeric solutions. After exposure, the resist is developed in chemicals that dissolve unexposed (negative) or exposed (positive) material.

Besides being sensitive to electrons, the resist material must be compatible with the various fabrication steps, other than exposure and development —the material must withstand the temperatures encountered, resist chemicals and plasma processing, adhere to the substrate and provide a stable image throughout all other steps. Also, since resolution is ultimately determined by electron scattering from the resist (and from the substrate), a minimum of resist scattering is desirable.

The number of E-beam-machine installations is indicative of the rapid advances in E-beam technology. Vector-scan units come from Cambridge Instruments at Motorola, from Philips at Signetics and from Electron Beam Microfabrication (EBM) at Burroughs.

Burroughs collaborated with EBM on a vector-scan unit, and EBM plans to offer commercial versions later in the year. Burroughs will employ the unit for direct on-the-wafer writing for IC production. The unit's high intensity gun eliminates the need for creating new fast E-beam resists; existing process-compatible resists are adequate and can be used at production rates, EBM claims.

For small IC manufacturers who can not afford a private E-beam system, Micro-Mask (Sunnyvale, CA) will make available its $1.9 million Varian raster-scan unit. Micro-Mask is an independent E-beam photomask maker, in business since 1978. With



WAVELENGTH LIMITATIONS

ELECTROMAGNETIC RADIATION

	λ (Å)
VISIBLE	7200 4000
ULTRAVIOLET	4000 50
X-RAYS	50 0.06

PARTICLE OPTICS

	λ
1) ELECTRONS (@ 15 kV)	– 0.1 Å
2) H^+ (@ 10 kV)	– 0.005 Å

$$\lambda = \frac{12.25}{\sqrt{V\ (\text{Volts})}} \cdot \sqrt{\frac{m_e}{m_i}}\ \text{Å}$$

DIFFRACTION EFFECTS

- LENS SYSTEM —— $S = \frac{0.5\,\lambda}{N \sin \alpha} = \frac{0.5\,\lambda}{N.A.}$
- CONTACT AND OFF-CONTACT IMAGING —— $\delta \approx 0.4\ \sqrt{b\ \lambda/2}$

this machine (its second), it will be able to handle 7-in. mask plates in a 1-μm mode for direct wafer-stepping machines, at about twice the speed attainable from its older unit.

Like TI, IBM and Bell Laboratories, Hughes Aircraft (Malibu, CA), has been building its own systems for several years. For direct on-wafer writing, the EBS/4 system is said to achieve 0.5 μm features, routinely, with throughputs that are faster than those of lower-resolution commercial units. Its beam can be positioned in 0.05-μm steps over a 2-mm scan field on 3-in. wafers.

X-ray printing lags

Although E-beam writing, especially for mask making, has taken giant strides in the past year, the X-ray printing system remains mostly a research tool. Indeed, direct E-beam writing may eventually replace X-ray methods. Problems with sources, masks and resists persist and limit throughput. The potential nevertheless remains great, but much must be learned before the process can be used in large-scale production.

Many companies, such as Bell Laboratories, Hughes Research, IBM and Texas Instruments, have built X-ray lithography and alignment systems for in-house development work. Some companies plan to offer a line of commercial X-ray equipment, photoresists and masks. But X-ray lithography still needs costly masks, and production rates generally do not come up to the speeds of conventional optical systems.

X-ray masks differ substantially from those for optical systems. They must be very thin so that fine-line geometry structures are not distorted or wiped out by X-ray absorption in the transparent mask areas. On the other hand, the opaque areas must be thick (or dense) enough to block the rays; therefore, dense (and expensive) materials like gold must be used. Masks made from thin materials are difficult to make and handle and easy to distort or break.

Resists also present a problem—they tend to have low sensitivity, thus requiring high radiation intensities or long exposure times. Where several masks must be exposed for a single wafer pattern, the time expenditure becomes uneconomical. Also, since X-ray masks are optically opaque, the method presents serious alignment problems.

For these reasons bubble-memories have been among those few devices reported to attain respectably high, near-economical throughput rates with X-ray techniques: They need only a single mask.

Step-and-repeat upgrade opticals

Optical printers have made significant advances—in particular, in the form of direct, step-on-the-wafer optical systems (Fig. 3), which can take advantage of the high resolution mask-making ability of E-beam machines.

Most authorities are skeptical that 1:1 projection over a wafer's full field in one pass can be improved enough to affect the better than 1-μm resolution needed for future VLSIs. The method is now stalled between 2 and 3-μm resolution.

With optical lenses (reflective for ultraviolet or refractive for visible light), resolution decreases as field area increases—for both theoretical and practical reasons. In addition, shorter wavelengths, although theoretically improving resolution, shorten focal depth (see "Wavelength Limitations and Diffraction Effects"). By printing small fields projected from 1× or even 10× reticles (made on E-beam machines), the problems with resolution and focal depth are overcome.

But the printing of small fields has limited value unless the fields can be accurately and rapidly aligned over a large area—for instance, to cover a full 125-mm (5-in.) wafer. This approach—the step-and-repeat system directly on the wafer—appears to be the direction of the IC industry.

Many small, high-resolution fields are combined to build up the total pattern with the aid of high-performance, mechanical X-Y tables. (Similar tables are employed to expand the small, high-resolution fields of E-beam projectors, as previously mentioned.)

Laser-interferometer distance-measuring systems, like Hewlett-Packard's 5526A laser-measurement system, can accurately resolve and control the mechanical displacements of such precision X-Y tables to about 0.01 μm (about 0.4-millionths of an inch). H-P's system is part of several E-beam systems, such as the Philips and TI units.

GCA (Burlington, MA) has adopted yet another laser-metering arrangement for its production-oriented Mann 4800 DSW (direct step-on-the-wafer system). Having 0.04-μm resolution, it achieves a desired X-Y table-location with a precision of ±0.1

μm. In a closed-loop servo system, the laser interferometer steps a 9-mm interval in just 0.45 s. The loop is critically damped to minimize overshoot and reduce the positioning time.

Like E-beam systems, step-and-repeat on-the-wafer systems are emerging from many companies. Electromask (Woodland Hills, CA) announced a wafer step system a few months ago (ELECTRONIC DESIGN, May 10, 1980, p. 39). Censor, Inc. (Reno, NV) announced a fully automatic unit, the SRA-100, with a claimed alignment accuracy of ±0.1 μm, a throughput of 60 wafers/hr for 100-mm diameter wafers and a working resolution of 1-μm.

Aligning, focusing, leveling and wafer handling are all automatic, under μP control, and parameters are displayed on a CRT data terminal. The unit handles wafers from 75 to 125 mm and reticles to 6 × 6 in. Square dice can be up to 403 × 403 mils; and rectangular dice 252 × 512 mils. The price is $565,000; delivery is six months.

Ion-beams are also essential

Equally essential in making VLSI, ion-implantation has become irreplaceable in a wide range of applications—not only for complex ICs, but also for discrete devices. Some IC products receive as many as four to six different implants at various stages during production according to Motorola (Fig. 4).

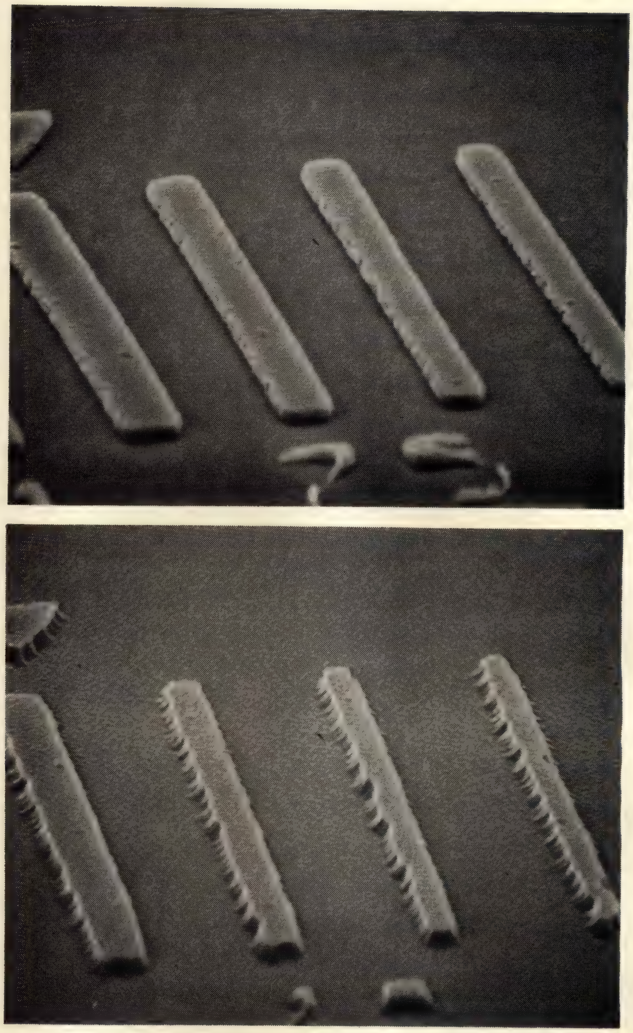
Several factors explain the rapid incorporation of ion-implanting methods as a standard process:

- It gives superior control and is often the only available method to dope certain sustrates.
- It is compatible with existing processes.
- Each application sparks new ones, and improvements broaden the method's usefulness.

One advantage of ion implantation is that it is a low-temperature process. Ordinary photoresists, which cannot withstand high diffusion-furnace temperatures, can act as masks for many low or moderate-dose implants (the low dose tends to keep wafer temperatures below about 100 C). Perhaps even more important, since wafers need not be exposed to the high diffusion-furnace temperatures, prior steps in the process sequence are not upset, and the sequence has more flexibility.

In addition, the beam (like a mass analyzer) delivers a very pure dopant dose, more readily obtained and controlled than with any other diffusion process. Most significant, ion implantation is the only way to obtain the low doping ranges needed for MOS threshold-voltage control and JFET fabrication.

Control is so precise that doping ranges can be adjusted to specific numbers of atoms per unit area. Also, the dopant profile (depth) can be accurately regulated and applied, even through thin layers of silicon dioxide or nitride.



5. Clean, sharp, uniform 2-μm lines are provided on a Texas Instruments (Houston, TX) circuit chip by plasma etching (a); a wet process provides feathered, rough, uneven lines (b) for the same mask and under similar processing conditions.

The ion beam is not limited to implantation. For instance, ion beams can contribute many advantages to lithography. Resists are more sensitive to ion beams than to electron beams—they are more efficiently absorbed, so exposure times can be shorter. Ion beams produce negligible backscatter, unlike electron beams. Backscatter limits the resolution attainable with E-beams. Finally, an ion beam has a shorter effective wavelength, for finer resolution. Hughes Aircraft (Malibu, CA) is experimenting with ion-beam lithograhy and claims major success.

Applications of plasma techniques lag

Plasma processing is apparently lagging behind ion-implanation techniques in actual applications. Judging by the number of published papers, much wider use would be expected. But most IC makers in silicon valley are not exploiting plasma processing to the extent that equipment makers (and some IC

VLSI technology is here

The technology for 1-µm geometries is at hand, say Texas Instruments engineers. To prove it, they scaled down an SBP0400 4-bit microprocessor element that contains approximately 2000 gates (see figure). Not only was the original chip size of 13.5 mm^2 reduced to 3.4 mm^2, but the circuits' performance was improved: Internal gate delays at 100 µA dropped more than half, from the range of 13 to 18 ns to 5.5 to 8 ns; the clock-frequency maximums increased about three times from 1.8 MHz to between 4.8 and 5.2 MHz at 50 mA.

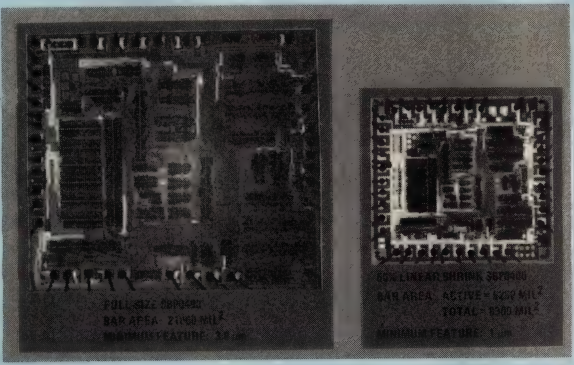
In addition to the overhead time, the key processes in the 1-µm technology included (see tables):

- E-beam slice writing employing a 0.4-µm-diameter beam and a positive, high-resolution resist
- Registration accuracy, level-to-level, of ±0.25 µm for 10-mask double-level processing
- Ion implanting, annealing and oxidizing
- Plasma etching with a Si-to-oxide ratio greater than 10.

With these techniques, geometries as small as 0.9 µm were reliably defined in roughly 2500 Å of oxide over heavily doped semiconductor layers with junction depths as shallow as 0.2 µm. The resulting scaled-down I^{2}L structure was optimized for devices built in 1 and 1.2 µm epitaxial layers.

The processing included 10 E-beam patterning steps (see Table) and started with epitaxial silicon on n$^+$, Si substrates (0.02 to 0.008 Ω-cm resistivity). Alignment markers, patterned and etched into the Si served as physical reference points for all alignment needs.

Nevertheless, the resulting scaled-down structure is a compromise design. A fully optimized design (from scratch), which would employ the full proven resolution of E-beam writing and resist capability could reduce the chip even further, from 3.4 µm^2 to 2.9 µm^2, which is a reduction of almost 33% without changing the design rules. Then the packing density would be 690 gates/µm^2 (including interconnects) vs just 148 gates/µm^2 for the full-sized design—a packing density increase over four times "conventional technology," with more to come.



EBM-II overhead for a 3-in. slice

Pattern geometry overhead	— 0.5 min
Step-and-repeat	— 0.55
Auto-load/unload	— 0.4
Auto-align (every chip)	— 0.25
	1.7
Writing time	2.7
	4.4 min total

Assumptions:
Average 60,000 geometries/level
150 chips (5.08) mm × 5.08 mm)/slice
Courtesy of Texas Instruments

SBP0400E process summary

Level	Minimum geometry	Conditions
1. Alignment markers	10 µm	5 µm Si etch (CF$_4$, O$_2$)
2. Isolation	1.9	5500Å anisotropic Si etch 11,000Å oxidation (1.0 & 1.2 µm EPI)
3. Collector	3.8	As 80 keV 3.5 × 10^{15} ions/cm^2
4. Resistor	5.1	As 100 keV 2.3 × 10^{13} ions/cm^2
5. P+ extrinsic base	1.4	B 50, 70 keV 1.5 × 10^{15} ions/cm^2 6300Å plasma oxide implant mask
6. P$^-$ intrinsic base	8.1	B 300 keV 2 × 10^{12} ions/cm^2 16,000Å resist implant mask
7. Contacts	1.0	
8. 1st level metal	3.0	Pt (200 Å)/TiW (1750 Å)/Al + Cu (4000 Å)
9. Vias	1.1	6000Å plasma-oxide dielectric or 1-µm polyimide dielectric
10. 2nd level metal	3.8	TiW (1750 Å)/Al + Cu (6000 Å)

manufacturers) say they could.

Most processing experts concede that dry-plasma processes will replace all wet-chemical methods—in time. Environmental, disposal, handling and storage hazards of the wet chemicals pose serious problems, which plasma processing substantially avoids.

In addition, plasma materials (gases) can be used more efficiently, and control of the process can be more uniform, especially for the fine-line geometry of VLSIs. The etchants are highly selective, tending to work only on the desired part of the wafer, and provide clean results without undercutting (Fig. 5).

Plasma-equipment makers say that they can provide most of the processing necessary for modern

IC-device fabrication, after the image is exposed on the wafer. Properly deployed, this very flexible tool can increase yields and cuts costs. Texas Instruments is all out for plasma technology: "Plasma processes are now the rule at TI rather than the exception in many stages of modern semiconductor-device fabrication." At least one IC maker takes an opposing stance: "We use plasma techniques to a very limited extent. We're sticking with established procedures as long as we can."

According to TI, "Progress is being made in establishing the chemistry and physics of plasma phenomena, but many steps are still not well understood scientifically, even though they are absolutely essential phases in semiconductor manufacturing."

Even so, several plasma equipment manufacturers offer μP-controlled systems for etching, deposition and photoresist removal (ashing, or stripping). The equipment operate at power levels from a few watts to kilowatts, cover a frequency range from ultrasonics to microwaves and cost from hundreds of dollars to hundreds of thousands, depending on the process and materials involved.

The LFE Corporation (Waltham, MA) offers two new etcher systems, the PFS/FDE/PDS-501 (Fig. 6) and 1002. The 501 has a single planar-etcher changer with a capacity of twelve 3-in. or eight 4-in. wafers. The 1002 has two independent chambers that can operate as a planar system (with twice the capacity of the 501) or as a combination barrel/planar system (one chamber planar; the other barrel). Etching uniformity is ±5%, and dimensions can be controlled to ±0.1 μm with polysilicon.

The LFE system 8000 can deposit SiO_2 at the rate of 2000Å/min. over a temperature range of 20 to 340 C (300 C is optimum). The film's properties are claimed to be superior to those resulting from other methods, such as rf sputtering, chemical-vapor deposition (CVD) or even thermal oxidation. Until recently, plasma deposition presented no challenge to high-quality thermal oxidation of Si, in creating SiO_2 films for intermetal insulation in double and triple-level metal systems or for gate dielectrics.

As a top-level insulation (passivation) layer, however, plasma-deposited Si_3N_2 is the best choice, because it provides a strong barrier against sodium and water vapor. It is becoming a standard process for "overcoating."

Plasma develops photoresists

One process not covered by plasma technology until very recently is photoresist development. A dry photoresist development would supply an important missing link towards an all-dry wafer process. Resist patterning is one of the most repeated steps in wafer fabrication; therefore, a dry process would further the elimination of wet chemical processes.

6. A planar plasma etcher, made by LFE (Waltham, MA), the PFS/PDE/PDS-501 can etch twelve 3-in. or eight 4-in. wafers at one time and control dimensions to ±0.1 μm with polysilicon.

Motorola (Phoenix, AZ) evaluated many commercially available resists, but found none very suitable for production using plasma processing. Its engineers are now investigating the formulation of new photoresist materials, and improvements in their formulation and processing in plasma-equipment reactor.

One result of Motorola's investigation is a negative-acting plasma-developable photoresist (PDP) that "meets all requirements for production in a straightforward way." The resist can define and etch patterns of SiO_2 (5 to 20 kÅ thick), Si_3N_2 (2 to 10 kÅ) and aluminum (10 to 75 kÅ), and will be used this year in production. Expected throughput is about 100 wafers/hr and exposure energy is about 10× faster than with current negative resists.

The initial resist film (9 to 30-kÅ thick) receives a low-temperature prebake and is then exposed to ultraviolet in a contact or projection aligner to polymerize the material. Plasma development in a Tegal barrel reactor with 100% oxygen is followed by a relief bake, which eliminates volatile components from the unexposed and unpolymerized parts of the film and makes the film about 40% thinner.

Plasma technology opens up the captivating possibility of a complete IC factory in one machine—between mask making and the final packaging. In theory, totally dry processing of all the various steps is possible with the same physical equipment—only the gases, pressures, timing and other process variables must be changed for the different phases.

But therein lies the problem: the large number of variables often makes the process difficult to predict and optimize. Cooling the wafer when it gets too hot from ion bombardment is another problem, but it should be less difficult to solve. More development work still remains.□

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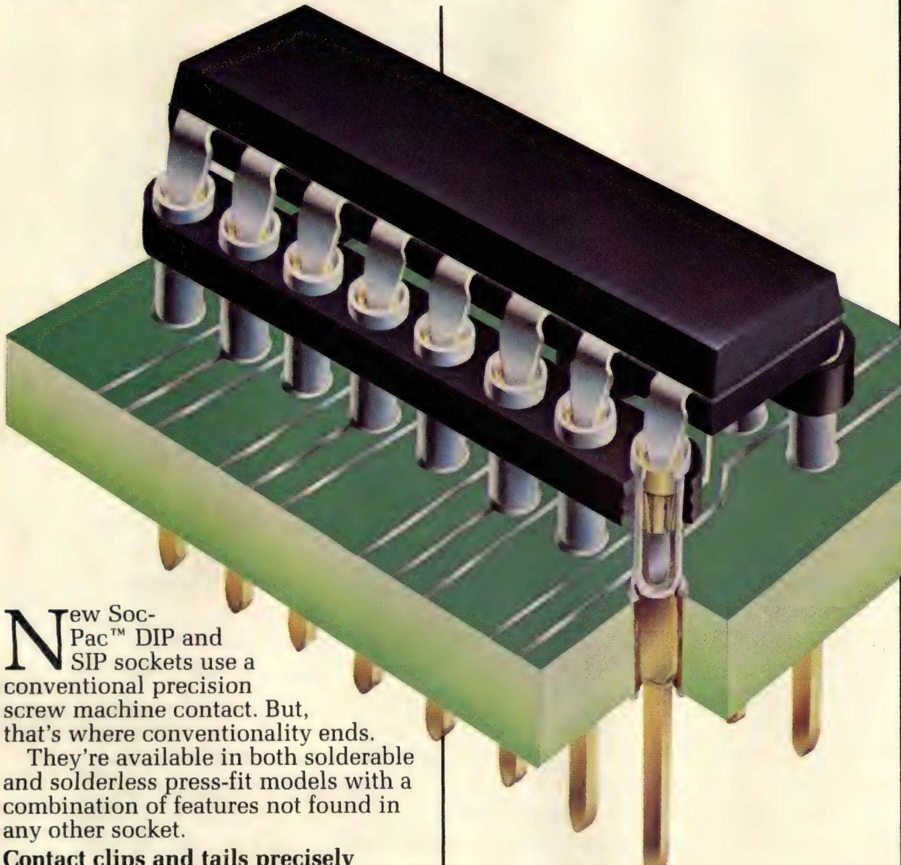

New Soc-Pac™ DIP and SIP sockets use a conventional precision screw machine contact. But, that's where conventionality ends.

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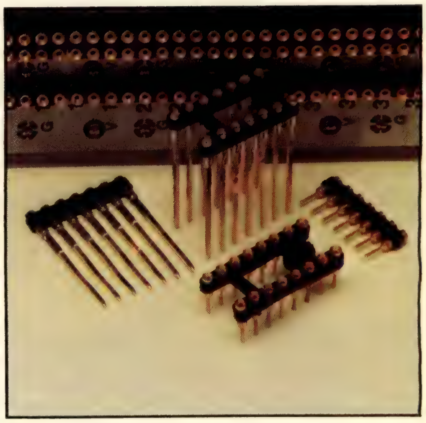

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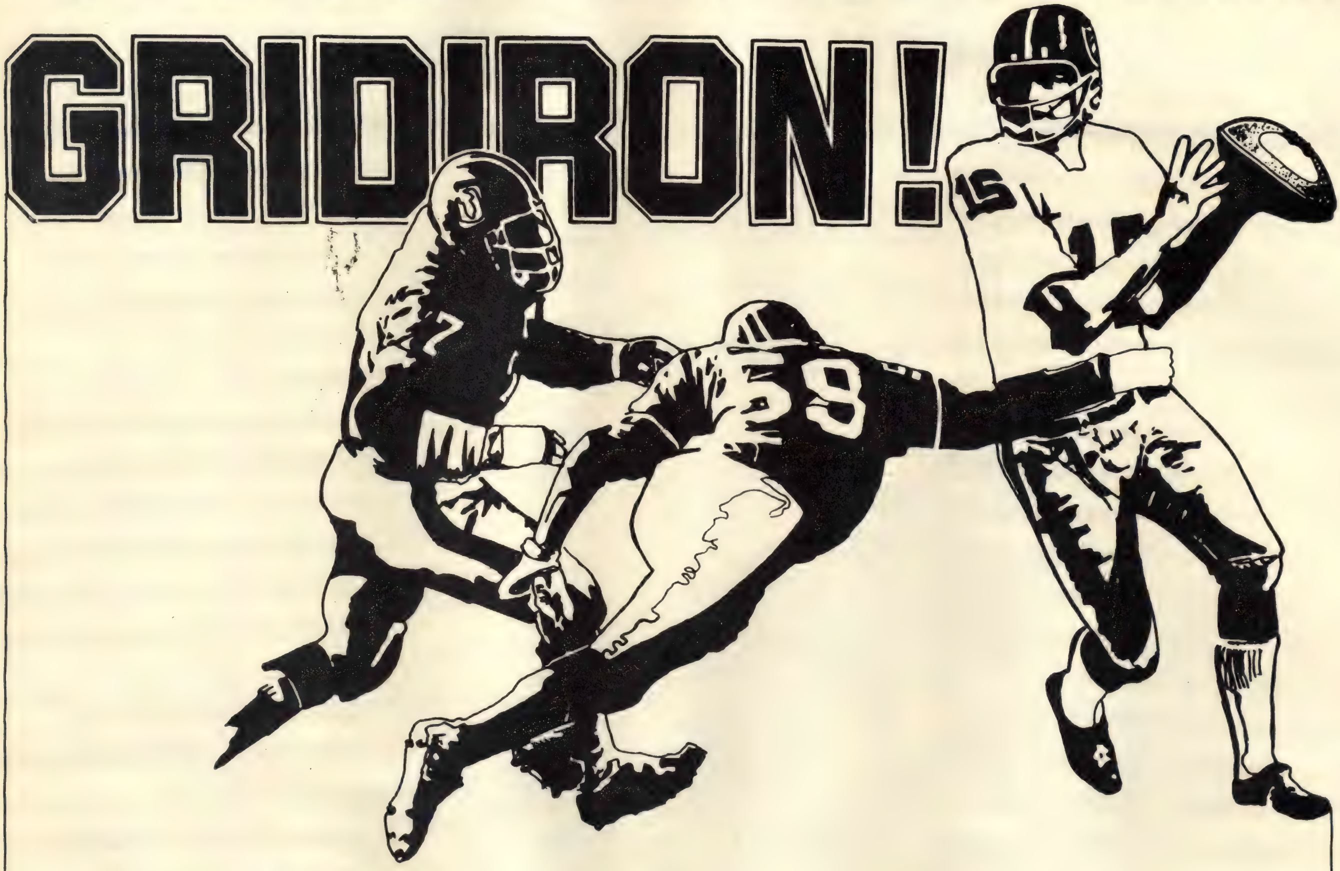

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Processing and innovative structures have boosted densities in the latest memory and μP ICs—and brought memorable performance improvements. Lines are drawn and layouts are ready to keep the products coming.

Memory and μP ICs pack more, consume less

Digital technology is the major driving force behind IC density improvements, and nowhere has this been shown more spectacularly than in the latest memory and microprocessor circuits. Packing more components on a chip does a lot more than save space—both overall system power consumption as well as overall circuit propagation times typically decrease. What's more, all the technologies used to fabricate the ICs benefit—CMOS, NMOS, PMOS, bipolar (TTL and ECL) and even the comer, gallium arsenide (GaAs).

Circuit density is improving thanks to processing and lithography developments that permit extremely fine lines to be drawn and etched, such as with electron-beam generated masks coupled with plasma etching and projection printing. And individual transistor performance is improving thanks to selective ion implantation and the ability to control junction depths to within a few angstroms.

Helping the cause are technologists who have constantly outdone themselves to conceive new device structures that overcome the limitations of the previously used transistor structures and layouts. These innovations, coupled with improvements in the processing equipment, have helped bring an incredible array of products out of the semiconductor-manufacturer ovens, notably 64-kbit dynamic RAMs, speech synthesizers on a single chip, and a growing army of 16-bit microprocessors and their support circuits. Simply put, the performance available off the production line goes well beyond what many designers thought possible in the mid-1970s.

On most MOS and bipolar production lines, manufacturers routinely use lithography rules that include line spacings and widths in the 4.5 to 6.5-μm region. But for some of the latest products, such as the high-performance 16-bit μPs and super-fast

Dave Bursky, Semiconductors Editor

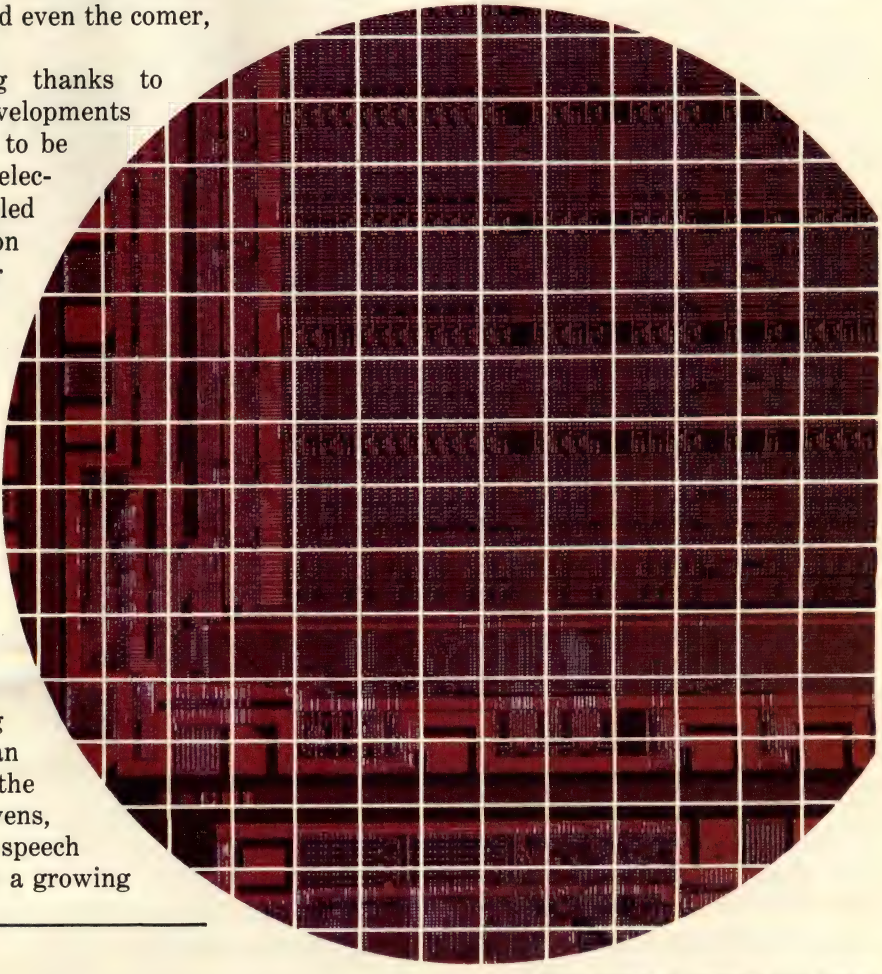


Photo courtesy of Advanced Micro Devices memories, some companies have gone to 3-μm production. Reducing line spacings is not the entire answer—device size must also be reduced to drop individual transistor power requirements, and the voltage stresses that would be imposed have to be cut back. This "scaling" process, already in widespread use, has brought to light new problems that accompany performance gains.

Watch out for alpha particles

One notable problem in MOS dynamic memory arrays is alpha-particle sensitivity. The impact of an alpha particle in certain areas of a semiconductor causes the generation of close to a million electron-hole pairs. And, when scaling reduces the charge stored in the memory cell to about the same size, an alpha-particle hit can effectively wipe out the stored charge and cause a soft error. Depending on where the alpha particle hits the device, it could cause either an error in a binary 1 or 0, or both.

Memories aren't the only circuits to encounter such sensitivity troubles. Microprocessors and peripheral-support chips also take advantage of much dynamic circuitry to save space and power on the chip. Fortunately, as stored charges get even smaller in the forthcoming generations of memories and other digital circuits, better packaging, aided by new layout techniques, will minimize the number of alpha particles generated.

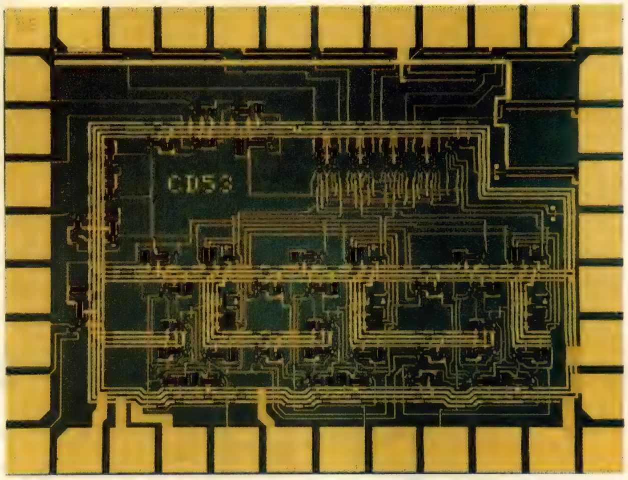
On the positive side, scaling permits NMOS to, in many cases, rival the performance of TTL-type bipolar circuits—but with higher densities and lower power. Scaling also works for bipolar transistors, and although work in the bipolar area seems to have taken a backseat to NMOS, developments are starting to appear that will keep bipolar circuits at the leading edge of performance, if not density.

The relatively new area of GaAs integrated circuits is a different story. Slated for commercial appearances in late 1981, GaAs ICs will offer performance levels almost an order of magnitude faster than even the best ECL. However, GaAs still has limitations to overcome (Fig. 1)—density (actually complexity—few companies have fabricated circuits with more than about 100 gates) and lithography (fabrication requirements include gate widths in the 0.8 to 1.5-μm range). For more on GaAs, see "The Future of GaAs."

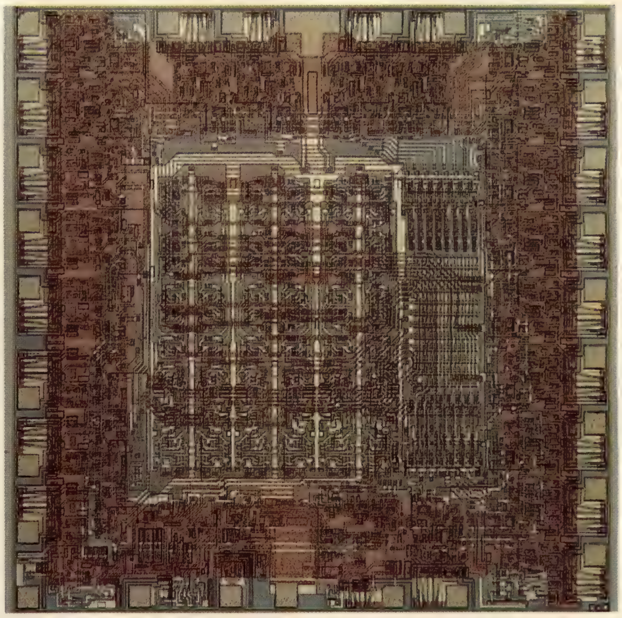
Staying ahead—for now

Over the last five years, ECL products have been the unchallenged high-performance logic-family products, featuring sub-5-ns gate propagation delays and medium-scale levels of integration. And new oxide-isolation techniques such as Fairchild's (Mountain View, CA) Isoplanar and Motorola's (Phoenix, AZ) Mosaic I promise subnanosecond logic functions with LSI circuit-packing densities. At the same time, however, the latest processing tricks and fine-line lithography will attain LSI for a price—power levels approaching the limit of currently available packaging technology.

The F100220 family of 8-bit digital-processing elements from Fairchild is a good case in point. The key element in the family is the F100220 address and data interface unit, which contains an 8-bit-wide ALU, an error-correction encoder and decoder, and three 9-bit I/O buses. The ninth bit provides parity, when used.



1. Considered MSI-complex, this 60-gate GaAs circuit developed by Rockwell acts as a 1:8 data demultiplexer at frequencies up to 1.1 GHz.



2. Using low-power Schottky technology, Texas Instruments has built a circuit that detects and corrects single-bit errors in 16-bit words, and detects and flags double-bit errors.

A total processor system would consist of cascaded F100220 sections (typically four to eight) supported by the other system elements and MSI logic. The other support circuits include the F100221 multiple-function network, which contains some of the often needed system "glue"; the F100222, a dual-access stack; the F100223 programmable interface unit, which contains the TTL interface logic along with the I/O control; and the soon-to-be-introduced F100224 microprogram sequencer. When eight of the ALU sections are cascaded and the F100179 lookahead-carry generator is used, a 64-bit add operation requires just 35 ns.

However, although the components form a high-performance system, each of the circuits dissipates about 4 W. In addition, to provide all the necessary interconnections, the circuits are housed in leadless 68-contact with built-in heat sinks.

Also available using Fairchild's Isoplanar process are some extremely fast memory products in both the company's 100-k logic family and the Motorola 10-k family of ECL products. Access times in the 10 to 20-ns range will keep just about any system operating at maximum efficiency. What's more, Fairchild has developed the F200 semiconductor array, which permits designers to turn around an IC from logic diagram to finished chip in about three months. Based on a cellular array of basic gate functions, the circuit permits the designer to pick higher-level functions from a library; a computer-aided-design program will generate the necessary interconnections for the desired cell function.

There are approximately 170 to 300 equivalent gate functions on the F200 array, depending on emitter and collector dotting. The chip itself measures about 173 × 130 mils. Power for the 100-k compatible array is high—about 4.5 W. However, relief is on the way in the form of the F201, and identical array that consumes only 40% of the power. A much more complex array, the F300, with about 2000 gate equivalents, is expected by early 1981. Internal gate propagation delays are expected to drop to about 400 ps. To facilitate I/O interfaces, the array will probably come in a leadless package with 150 or more contacts.

Motorola's Macrocell array provides designers with uncommitted functions and components arranged in an array. With the help of computer libraries of functional blocks, the individual cells can be connected to form the desired functions.

Using Motorola's latest ECL process, Mosaic I, the Macrocell offers a level of performance equaled only by pure custom designs. The Macrocell array packs 106 cells, each of which contains uncommitted transistors and resistors. The chip measures about 220 × 250 mils and actually contains the equivalent of about 1200 gates, depending on the library macros used to define the circuitry. There are currently about 85 "standard" library functions that can be selected through an interactive terminal.

Just how much performance all this involves will be unveiled shortly with the introduction of three digital functions—two ALUs and an 8 × 8 multiplier. With internal gate delays of just 700 ps, these circuits will be able to perform their operations in less than 10 ns.

Other Motorola memory products will go Mosaic, including RAMs slated for introduction later this year and early next, as well as larger-capacity units later on. Also, Motorola is rumored to be revamping its ECL 10-k logic family using the Mosaic process; the result should be a family that will cut all propagation delays by 50% over the existing 10-k equivalents. The initial devices in the family are expected to be totally pin-compatible with existing 10-k products with the additional benefit of having on-chip voltage regulation to keep the logic levels constant as the power-supply levels change.

Status of semiconductor technology

	Current			Future (1985-1990)	
	NMOS	Bulk CMOS	SOS-CMOS	SOS	GaAs
Relative process maturity (scale of 1-10)	9	8	4	2*	1*
Process complexity (no. of steps)	9 to 15	14 to 17	14 to 20	14 to 20	16
Logic complexity (no. of components, 2-input gate)	3	4	4	3 to 4	2
Packing density (gates/mm²)	100 to 200	40 to 90	100 to 200	200 to 500	300 to 1000
Propagation delay (ns) (typical value)	4 to 25 (15)	10 to 35 (20)	4 to 20 (10)	0.2 to 0.4 (0.3)	0.05 to 0.1 (0.07)
Speed-power product (pJ)	5 to 50	2 to 40	0.5 to 30	0.1 to 0.2	0.01 to 0.1

*As of 1980

Source: Lockheed MSC

The future of GaAs

Though some speak glowingly of the future for GaAs-logic devices, there are several hurdles to overcome—notably density limitations. Power dissipation, circuit structure and material all contribute. And currently there are no production-level lithography systems that can repeatedly yield the alignment accuracies necessary to pump out thousands of circuits a day. On top of all that, designers have not yet defined just what circuit functions would be practical to commercialize in GaAs, since the voltage levels would be different from any currently used "standard" voltages.

Nevertheless, work at Rockwell Electronics Research Center (Thousand Oaks, CA) has led to the fabrication of ICs using Schottky-diode FET logic (SDFL) in GaAs. SDFL is just one of about half a dozen structures currently being used to provide the first indications of the LSI capability of GaAs (see Table).

Current levels of integration using SDFL structures have resulted in circuits with complexities at the 100-gate level, according to Richard Eden, principal scientist in solid-state electronics at the center and an outspoken proponent of GaAs logic. What's more, he continues, circuits with complexities of 250 to 500 gates are now being characterized while circuits approaching 1000 gates are in design. By 1984, Eden feels, circuits with complexities approaching 10,000 gates will be feasible—on a chip measuring just 5 mm on a side (about 200 mils). In comparison, today's µPs, which have about 10,000 gates, require a chip that measures about 300 mils on a side, or about 2.25 times the area.

Of course, that comparison is slightly biased—the silicon-based technology uses 3-µm lithography rules while the GaAs circuits use 1-µm. If the silicon technology could be projected three years out, the area for an equivalent function would probably drop by about 50% or more, thus bringing the chip-size difference closer together. However, when lithography gets to the point of permitting silicon line widths in the 1-µm region, alignment accuracies must approach 0.25 µm. GaAs alignments are not as demanding, though, because of the device structure—with 1-µm line spacings, the various masks can stay within 0.75-µm alignment accuracies.

Rockwell has chosen the SDFL structure because of the simple gate structure permitted through the use of the Schottky diodes as the gate inputs. The extremely small diode size (about 1 × 2 µm) and high f_T's (about 300 GHz) make the final circuit much more compact than most of the other structures developed. Eden projects that propagation delays will be reduced to about 50 ps with 1-µm MESFET gate structures and further reductions to 20 ps will be possible with 0.25 to 0.5-µm gates. Ultimately, delays will shrink to 10 ps, Eden predicts, by combining 0.25-µm gate structures with low-temperature (about 77-K) operation.

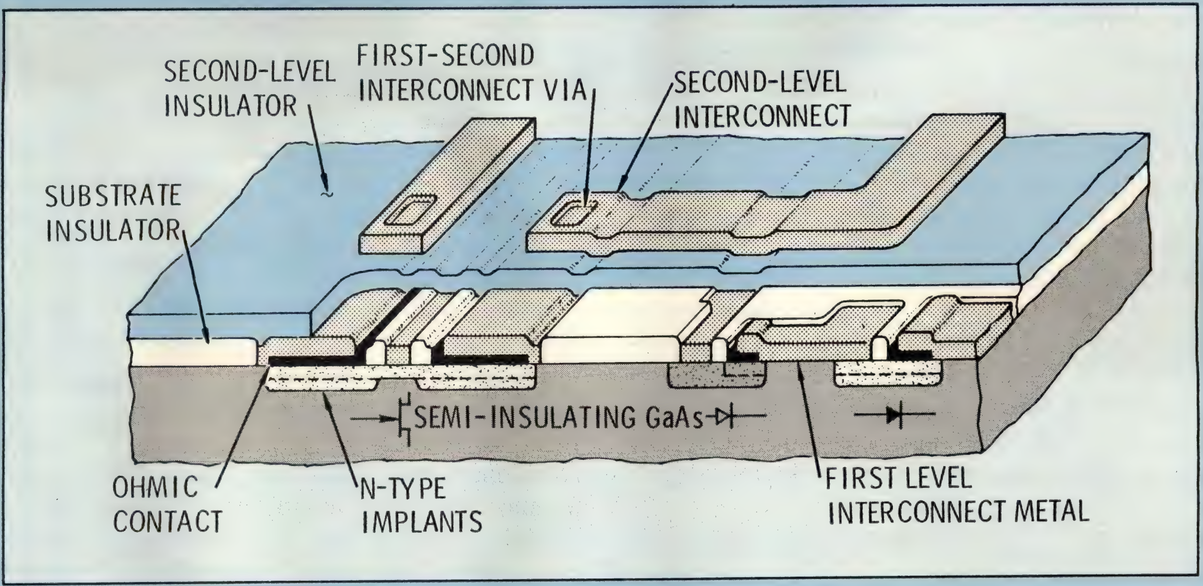
Rockwell planar GaAs IC demonstration circuits

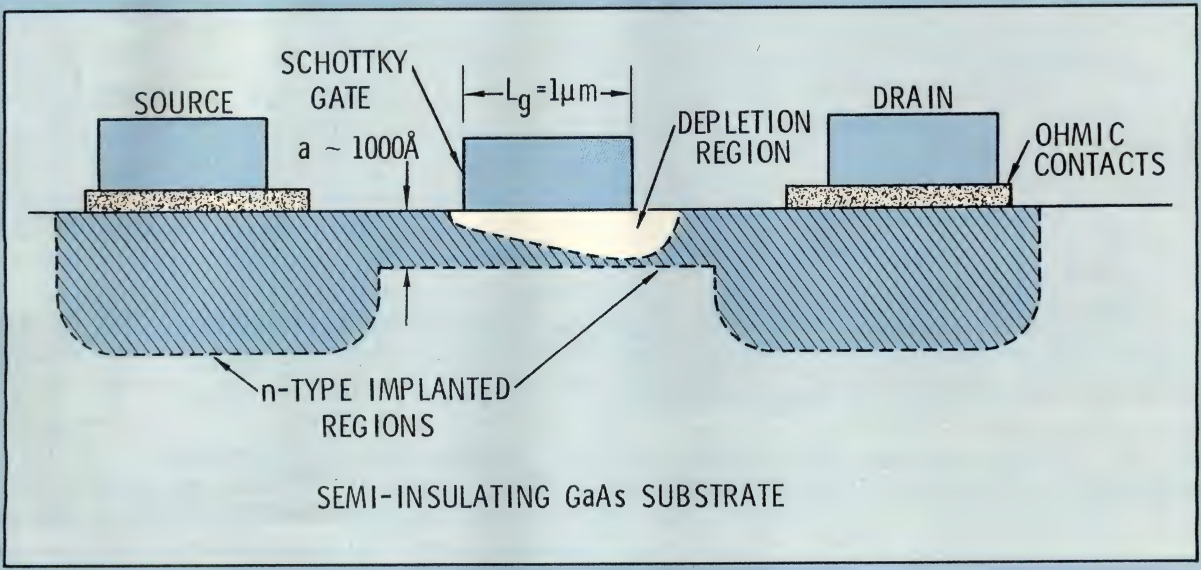
Fully working, successfully tested		
8-stage shift register/217-bit P/N code generator	96	gates
3 × 3 parallel multiplier	75	gates
4-bit fast ripple-carry adder using 2 and 3-level gates	43	(63 equiv)
÷ 10/11 or ÷ 20/22 var. mod. divider for freq. synthesizer	37	gates
8:1 data multiplexer with address generator	64	gates
1:8 data demultiplexer with address generator	60	gates
1-GHz analog sample/hold or track/hold circuit	25	components
Digital FM demodulator circuit	65	components
÷ 8 frequency prescaler (D-flip-flop ripple divider)	25	gates
÷ 8 synchronous counter implemented with D-FFs	33	gates
NOR-gate ring oscillators in 3,5,10 and 20-µm widths	9	gates
OR/NAND gate, 3-propagation-mode ring oscillators, 5 and 10 µm	7	gates
Fabrication/initial-testing stage		
5 × 5 parallel multiplier	260	gates
2 × 32 shift-register/dual 4.3 × 10^9-bit P/N code gen	550	gates
Layout/digitization stage		
8 × 8 parallel multiplier	1000	gates

Taking a different approach to GaAs logic, Lockheed Microelectronics uses enhancement-mode MESFETs and has been able to attain some low levels of integration thus far, but expects to increase the complexity in the next few years. D. Howard Phillips, head of the GaAs research team, sees the need for better materials as one of the prime targets for the next few years.

Compared to silicon technology, the GaAs materials technology is still in its infancy, Phillips explains, and few manufacturers of GaAs can really manufacture the material to the desired characteristics. Until recently, chromium-doped material had to be used to keep the impurities properly balanced. However, undoped materials with fewer impurities can now be pulled to provide the high performance without any additional impurities.

Meanwhile, a new form of FET logic that's a spinoff of the company's current-mode bipolar logic looks promising to TRW's Tom Mills, manager of the microwave products group. Initial test circuits have just been designed and are expected to be fabricated





in the next few months for evaluation. Expected performance, though, is in the 2 to 3-GHz range for functions such as a/d conversion circuits and various logic functions. Using more conventional device structures, though, designers at TRW have plans for experimental circuits at the 50 to 100-gate complexity level and eventual integration at the 1000-gate level.

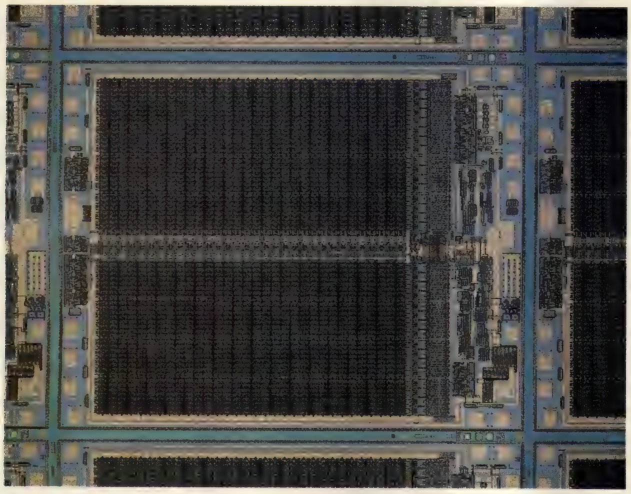
For the present, commercially available GaAs products number zero, although many experimental, military and aerospace circuits have been built. Defining which functions should be commercialized would be a big help, technology proponents agree.

Rockwell, for one, has demonstrated over a dozen functional circuits and has several more just being characterized or going into circuit layout—advanced designs all. But which products will be offered? Indications are that all companies are looking for a "universal appeal" function such as a divide-by-10/11 prescaler or multiplexer. Eventually, Rockwell expects to sample internally an 8 × 8-bit multiplier that should be able to perform a multiplication in about 6 ns. Whether or not it turns out to be commercially feasible, the device will not be ready for introduction until 1983.

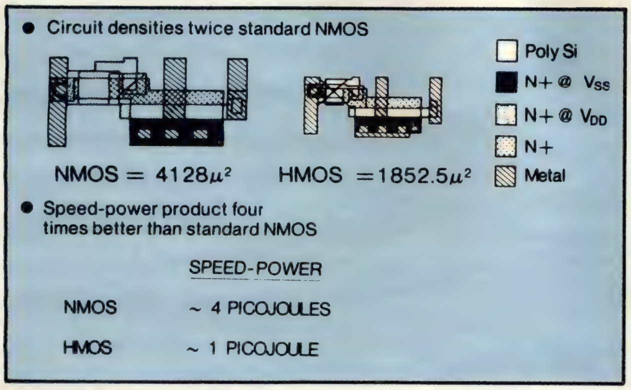
Other companies also are reaching into the gigahertz regions with ECL technology. For instance, Plessey in England has developed a family of counters and synthesizers that offer frequency division at frequencies up to 2 GHz (the SP8619). While high performance usually comes at the expense of power dissipation, Plessey has managed to curtail the power for some lower-frequency dividers: the SP8792 and 93, which are divide-by 40/41 and 80/81 counters, respectively, require just 70 mW maximum for count frequencies up to 250 MHz.

Taking ECL into the LSI domain, Advanced Micro Devices in Sunnyvale, CA, is getting close to seeing its first silicon for the Am29116, a microprogrammable 16-bit processor. The company's proprietary ECL process, combined with on-chip level shifters for TTL compatibility, will push the Am29116 to operate with microinstruction cycle times of 100 ns.

Even as ECL improves, so does TTL and all its variations—current-mode logic, integrated injection logic, as well as the low-power Schottky families and some advanced Schottky-TTL processes introduced last year by both Fairchild and Texas Instruments (Dallas).



3. Applying HMOS to memory arrays helps bring bipolar access times to NMOS devices. Typical of that enhanced performance is the Am9147 4-k static RAM, which accesses data in just 55 ns.



4. Twice the number of devices can be fabricated in a certain chip area as with standard NMOS, which Motorola accomplishes with a proprietary form of NMOS.

Some of the highest-performance functions in current-mode logic are offered by TRW LSI Components (Redondo Beach, CA), whose MPY family of multipliers can operate as speedily as 35 ns for an 8 × 8 multiplication on 8, 12, 16 or 24-bit words. A 2-μm production process helps get the high density and performance.

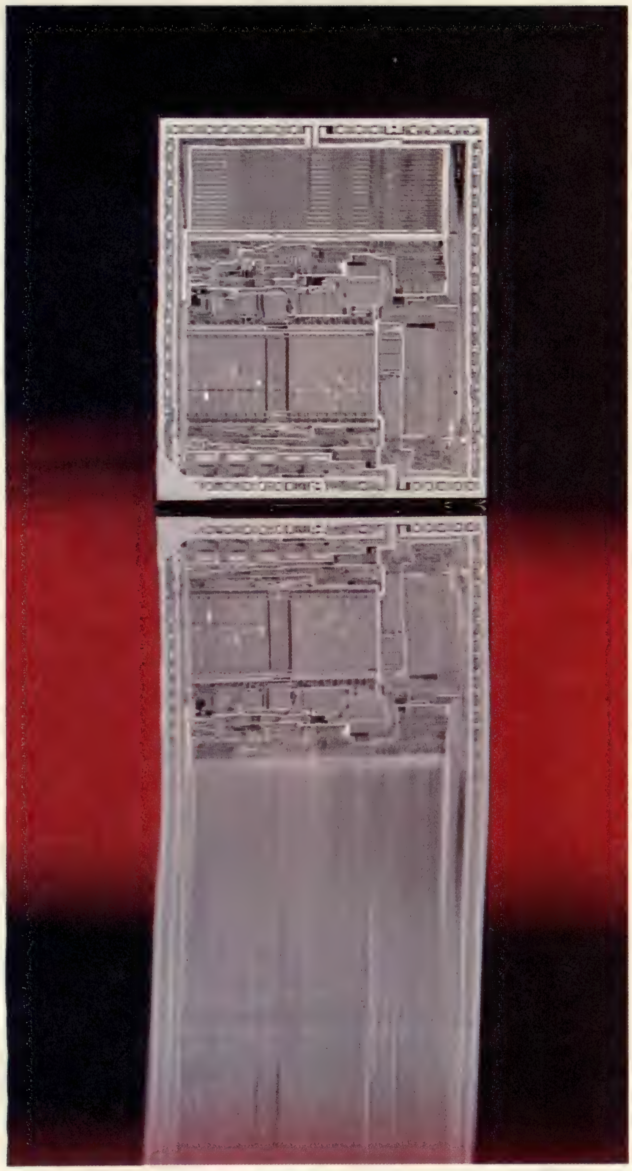
Joining the plain multipliers will be versions that include accumulators on the same chip, thus permitting a reduction of chip count and propagation delays in applications such as fast-Fourier-transform calculations where the multiply-accumulate functions are extensively used. Other circuits planned for introduction later this year include a digital correlator and a floating-point exponent-computing chip that will work with the 24-bit multiplier to provide a 32-bit floating-point multiplier system on just two chips, whose operating speeds total less than 250 ns.

Mask-programmable, too

Also available from TRW, but from the Government Electronics Division, are ECL gate arrays that can be mask-programmed for function as well as for either ECL 10-k or 100-k logic compatibility. Containing the equivalent of about 350 gates, the array layout consists of 64 master cells of primarily uncommitted components. Internal gate delays of 1 to 2 ns can be attained for loaded gates. One example of a circuit built from the array is a custom direct-frequency synthesizer that operates in the 700 to 800-MHz range and includes the switch, mixer, divide-by-4 counter and other functions on the chip.

Other processing advances include the one unveiled by Texas Instruments at last year's International Electron Devices Meeting: 1.1-μm lines on an I^2L experimental version of its old SBP0400 processor. By achieving cycle times in the tens of nanoseconds, the processor no longer becomes the limiting component in a system—the controller or memory becomes the slow-poke.

New "standard" families of TTL logic circuits using high-performance Schottky processing were introduced by both Texas Instruments and Fairchild in 1979. In fact, TI introduced two families—the advanced Schottky (AS) and the advanced low-power Schottky (ALS); Fairchild introduced FAST. Some of the parts are pin-compatible replacements to the older LS families, but with improved speed-power products, while future family members will be proprietary functions in high-density 20, 22 and 24-pin,



5. **The MC68000 16-bit microcoded architecture squeezes 68,000 transistors into a 68,000-mil^2 chip. In addition, it even permits simple modifications for future enhancements.**

300-mil-wide packages.

Both the Fairchild and TI families provide close to a 50% improvement in speed or power over conventional LS or Schottky-logic components. But while both National Semiconductor (Santa Clara, CA) and Motorola have agreed to alternate-source TI's ALS family, it looks as though Fairchild will be going it alone.

As part of its LS family, TI has introduced three major support functions for microprocessor, bit-slice or minicomputer memory systems. These include a dynamic-memory-refresh controller subsystem (the LS600 series), a memory mapper (the LS610 series) and an error-detection and correction circuit (the LS630 series). When combined in a system, these chips could end up yielding one of the highest-performance memory systems ever put together.

The memory-mapper chip takes four lines from a processor's address bus and maps those lines via a 16 × 12 RAM into 12 bits, thus yielding a 4096 time expansion of the processor's reduced (by four lines) address space. The EDC circuit operates on 16-bit words and can perform double-bit error detection and single-bit error correction (Fig. 2).

A complete memory-support subsystem is also provided by Advanced Micro Devices (Sunnyvale), which has defined three major products as well as the necessary buffer/interface components. The three major components are the Am2960/AmZ8160 error-detection and correction circuit (EDC), the AmZ2964 dynamic-memory controller (DMC) and, for Z8000 microprocessor systems only, the Am Z8163 refresh-timing and error-control circuit (RTEC).

For support, there are the Am2965/66 (AmZ8165/66) address-line drivers, with inverting or noninverting address outputs, respectively. Also forthcoming are the Am2961/62 (AmZ8161/62)—combination data-bus and EDC bus buffers—which feature inverting or noninverting buffers on the data-bus port.

On the I^{2}L front, several companies have gotten down to serious application. National Semiconductor offers a family of CRT controllers using I^{2}L to get the high bit rates, while TI uses the process to fabricate a full 16-bit μP capable of meeting the full military temperature range.

Even the basic I^{2}L transistor structure has been improved. One improvement adds Schottky diodes in the base to improve speed drastically with only a minimal effect on area. A good example of the performance possible can be seen in a test circuit using emitter-coupled injection logic and developed by researchers at the Institute fur Theoretisch Electrotechnik in Aachen, West Germany. As described at this year's International Solid State Circuits Conference, the circuit can achieve gate delays of 4.2 ns at just 200 μW/gate. This approaches the gate delays of ECL but with much lower power levels. Thus, the technology promises speed-power products for the next level of bipolar LSI.

Also working in the realm of I^{2}L is Signetics (Sunnyvale), which offers not only an I^{2}L array but also a higher-performance logic array using integrated Schottky logic (ISL). This ISL array, the 8A1200, contains about 1200 gate equivalents, consumes less than half a watt, yet offers the propagation delays of Schottky TTL.

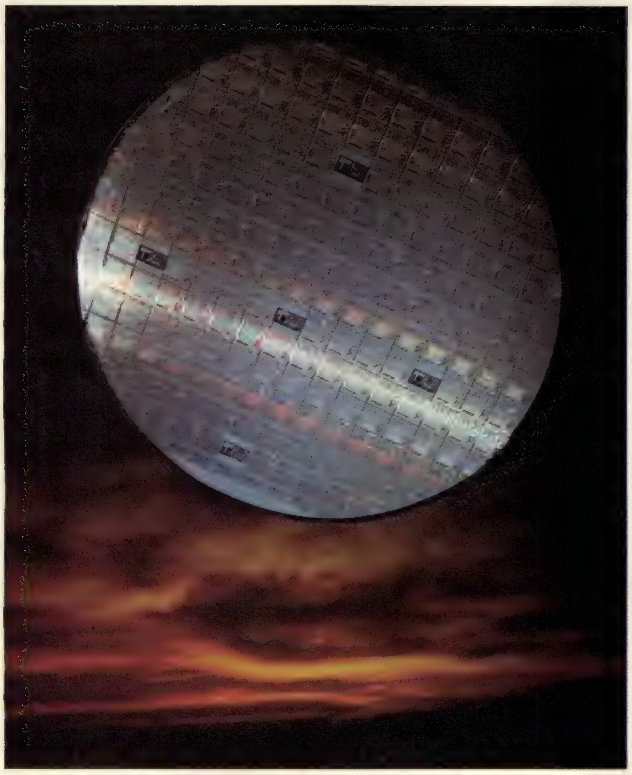
Fairchild is using its Isoplanar version of I^{2}L to plan a gate array with a complexity level of about 4000 gates and a gate delay of about 6 ns. Expected to be LS-family compatible, the array will be sampled in late 1981. Already on the way from

England, meanwhile, is the ULA5C000 array developed by Ferranti, which uses current-mode logic and offers internal gate delays of about 8 ns. Holding about 880 two-input gate equivalents, the array provides both linear and digital translation capabilities for its 48 interface cells.

In addition to all of the semicustom mask-programmable logic that is available from about 20 manufacturers, about half a dozen companies offer a form of field-programmable logic. Products based on this include programmable logic arrays, programmable gate arrays, programmable multiplexers, programmable array logic, field-programmable logic sequencers and field-programmable ROM patches. The field-programmable devices perform slightly slower than the semicustom products, with propagation delays of about 40 ns, maximum. But being field-programmable, the devices don't suffer from turnaround delays when changes in the pattern have to be made.

Meanwhile, bipolar performance is being approached by MOS, notably in the NMOS sector. Extremely complex 16-bit microprocessors and support circuits have been fabricated, along with memory circuits with bipolar speeds.

Density and performance improvements can be credited to extensive efforts to develop multiple-level polysilicon, scaled device models, charge pumps, and all the other circuit techniques needed to reduce power, transistor size, circuit capacitance, and many other performance-limiting factors. So, except for the need for large memories, the ability to put a function on a chip of silicon is no longer limited by the technology, but by the designer conceiving the circuit or subsystem function to be fabricated.



6. The Z8000 16-bit μP comes in two versions: a minimum version offers a 64-kbyte address space (the Z8002), and a maximum version offers an 8-Mbyte range in each of six work spaces.

One driving force behind high-performance digital technology, Intel (Santa Clara, CA), has developed several advanced processes in NMOS technology. Called HMOS, these processes rely heavily on device scaling, ion implantation, fine-line lithography and very thin oxide depositions. Combining all these factors makes possible such devices as 4096-bit static RAMs (Fig. 3) with access times of less than 50 ns, and μPs capable of operating at clock frequencies of 11 MHz.

HMOS is being used to upgrade the performance of Intel's previously introduced μPs and μCs. For example, Intel has redone the masks for its popular 8048 μC using 3-μm design rules, and has raised the clock frequency from the previously available high of 6 MHz to 11 MHz.

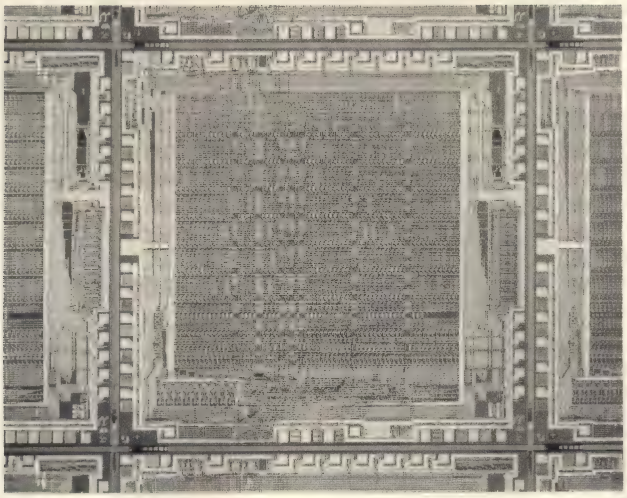
Actually, there will be two upgraded versions—the 8048H and 8048H-1—with the H offering a maximum clock of 8 MHz and the H-1 offering a maximum 11 MHz. And, along with the improved speeds comes a reduction in chip area—about 30%—which will increase the number of dice per wafer by about 40%. This improved yield should translate into both a higher overall production capacity as well as an eventual decrease in chip cost.

HMOS developments don't stop with the first generation at Intel. HMOS II is currently being phased-in. HMOS II couples the current HMOS techniques with advanced scaling techniques, which permits further reductions in cell size.

HMOS II appears in the company's leading-edge 2147 4-k × 1 static memory. With an access time of 55 ns, the 2147 was already the industry's fastest MOS memory. However, a pin-compatible HMOS II version, the 2147H, has a typical access time of just 35 ns—fast enough to rival all bipolar memories except ECL.

Motorola uses its version of HMOS in its latest microprocessor and memory products (Fig. 4). The MC68000 provides a full 32-bit architecture and can execute many of its instructions in less than a microsecond (Fig. 5). Packing about 68,000 transistors in a chip area of about 68,000 mil^2, the processor makes extensive use of microcode to define each of its user-accessible instructions, thus permitting future modifications and enhancements without requiring a major redesign of the basic chip logic.

Yet another version of HMOS is used in a three-member μP family from National Semiconductor.



7. **Using a computational technique known as the Chinese algorithm, a burst-error processor developed by AMD can detect and correct up to 12-bit burst errors in 20-Mbit/s serial data streams.**

The NS16008 and NS16016 can operate in either an 8080A-compatible instruction mode or in a native instruction mode, thus providing a transition from already available software to an advanced instruction set.

Architecturally, the 16008 looks like a pseudo-16-bit processor with internal 16-bit buses, an external 8-bit data bus and an addresing range of 64 kbytes. The 16016 offers a full 16-bit architecture and has 16-bit-wide external buses.

The most powerful of the three, the 16032, executes only the native instruction set, but offers a 32-bit internal data bus and an addressing range of 16 Mbytes without any support. The addressing range, though, for both the 16016 and 16032 can be expanded to 32 Mbytes by adding memory-management units.

Support will come from several dedicated circuits, which will perform such functions as memory management (including page-oriented virtual memory), advanced math operations such as floating-point multiply and divide, bus arbitration and DMA control. Some of these circuits, such as the math unit, are intended to operate as slave processors, monitoring the instruction stream and activating when the proper instruction is encountered. The other support circuits are designed as peripherals to the CPU, where the CPU must perform all control operations, and load and unload the registers.

Other companies using this slave concept include Intel and Zilog (Cupertino, CA); however, they call their respective circuits coprocessors and extended-processing units. Although Zilog has not specifically announced the first function it will implement as an EPU, a good guess would be either a high-level math circuit or a data-bus management controller.

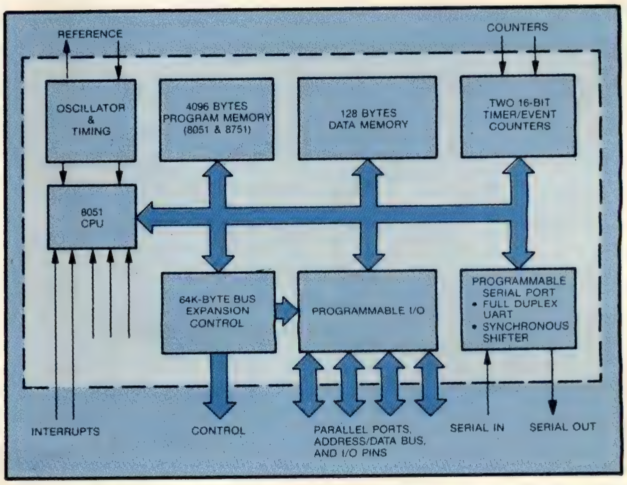
Even without the support circuits, however, Zilog's Z8000 family offers power and flexibility (Fig. 6). With two CPUs and a wide array of support circuits and boards to be developed jointly by Zilog and AMD, the Z8000 family will challenge every level of design to take advantage of all its capabilities. For example, the Z8001's 8-Mbyte address space, significant in its own right, can be expanded to 32 Mbytes with the help of the new Z8010 memory manager.

One special circuit being developed as part of the Z8000 family is AMD's burst-error processor, the AmZ8065 (Fig. 7). This circuit can, using a so-called "Chinese algorithm," correct up to 12-bit burst errors in a serial data stream. Data rates reaching to 20 Mbits/s will be possible because of efficient implementation of the correction algorithm.

Coprocessor support developed by Intel takes the form of an advanced math processor, the 8087, which adds IEEE-compatible floating-point math operations to the instruction repertoire of the 8086 or 8088 μPs. Described at the recent ISSCC meeting, the 8087 uses the company's HMOS to pack 30,000 bits into a four-state ROM, as well as 700 bits of RAM, a 68-bit arithmetic and logic unit, a fast shifter (0 to 63 places in one clock time), and a 68-bit-wide internal data path—all on a single, 300-mil/side chip.

In addition, Intel is bringing out an extremely powerful 8-bit μC chip. The 8051 is capable of performing Boolean operations as well as normal digital computations (Fig. 8). It also contains many powerful features—4096 bytes of ROM storage, 128 bytes of RAM, a fully programmable serial I/O port, two 16-bit programmable counter/timers and 32 programmable I/O lines.

Unique in its ability to implement Boolean functions directly through software, the 8051 represents a major advance in the simplification of the man/machine interface. Operating at clock frequen-



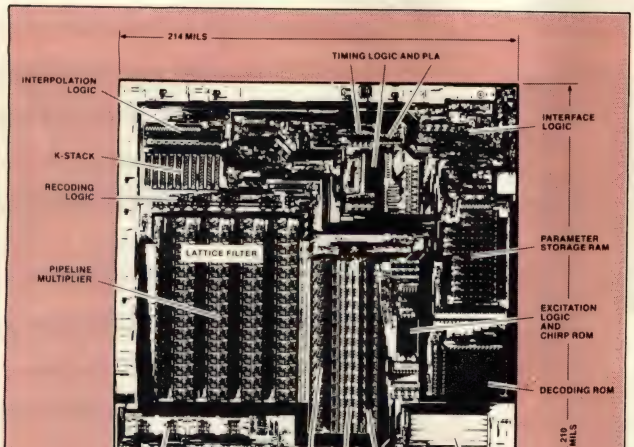
8. **Boolean and binary operations can be performed by Intel's 8051 μC, which contains 2048 bytes of ROM, 128 bytes of RAM, a full serial I/O port, two 16-bit counter/timers and 24 programmable-I/O lines.**

cies of 12 MHz, the 8051 includes multiply and divide instructions that execute in just 4 μs and can outperform the 8048 in almost every application. And, there will be not only a mask-programmable version but also a ROM-less version (the 8031), as well as a UV EPROM version (the 8751) for prototyping (for more on the 8051, see ELECTRONIC DESIGN, May 24, 1980 p. 57.)

Intel is not alone in the 8-bit, single-chip μC marketplace. Mostek (Carrollton, TX), Motorola (Austin, TX), General Instrument (Hicksville, NY) and Zilog also offer very powerful devices. However, Intel is one of a few companies able to place the UV EPROM on the same chip as the rest of the CPU functions. Motorola has managed to do it for both its 6801 single-chipper (the 68701), and for its 6805 (the 68705) and Fairchild has done it for the 3870 (the 38E70).

Mostek and Zilog circumvent the problem with a socket in a package, so that the EPROM rides piggyback on the microcomputer, leaving the user to plug a preprogrammed EPROM into the socket to program the μC. General Instrument, on the other hand, is examining ways to include some nonvolatile but electrically alterable memory on the chip—but not for the main program memory. Instead, the nonvolatile memory will be used to prevent data losses due to power failures or when power is just shut off. With research results looking promising, GI expects to evaluate some of its first samples soon.

The single-chip μC has found many homes—from consumer products to industrial controllers. However, even the microprocessor manufacturers see the μC as a powerful building block that permits the rapid development of intelligent peripheral controllers for the microprocessor. Zilog, Motorola, Intel and others are following this path to provide the necessary support and off-load the main processor.



9. PMOS does not limit the performance of the Texas Instruments TMS-5100 speech-synthesizer chip or its companion 128-kbit ROM (not shown). Both were originally developed for TI's Speak and Spell learning aid.

Motorola's MC68120, for example, is an intelligent peripheral controller that contains most of the features found in the company's 6801 μC, and then some. As described at the recent Electro/80, additions to the architecture include a dual-port structure for the on-chip RAM as well as an extra register intended for settling disputes in multiprocessor systems.

Intel takes a different approach for its 8089 I/O processor, by dedicating a peripheral I/O circuit from the ground up. This circuit contains a CPU and two independent 8-bit I/O channels that are supported by their own register files and instruction pointer. Both channels can be cascaded to form a 16-bit I/O channel when desired. The 8089 can also perform DMA transfers at up to 1.25 Mbytes/s.

Don't forget PMOS

With all the work being done to improve NMOS devices, it's easy to overlook the PMOS sector—and much of the same research applies here as well. Quite a few companies still have major production areas set aside for PMOS products.

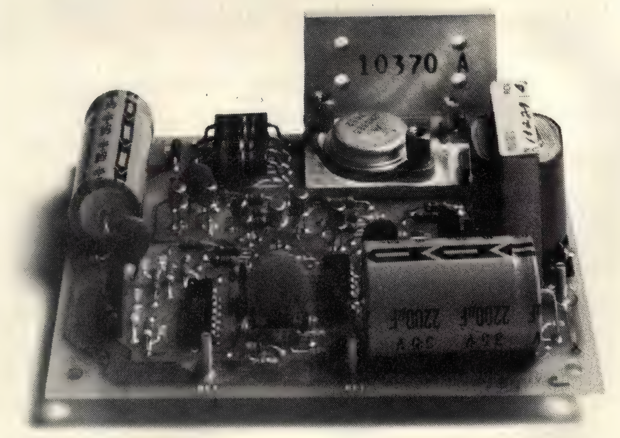
Although PMOS performance is lower than NMOS, PMOS is much simpler and final costs in most cases will be lower. And now, with the birth of the low-end μC—circuits like the TMS-1000 family from TI, or the PPS-4 family from Rockwell (Anaheim, CA)—PMOS has solidly entrenched itself for many years to come. New techniques have been developed to bring the operating power of PMOS very close to CMOS but, since fewer processing steps are needed, PMOS is less expensive.

While not all 4-bit μCs are PMOS-fabricated, a majority of them are, and new versions are still being introduced. TI's TMS-2100 μC family, for example, not only contains the CPU, RAM, ROM and I/O on the same chip but also a dual-channel, 8-bit a/d converter and a liquid-crystal-display controller. Combining powerful features with low cost will catapult this family into many consumer applications, where cost is a prime reason for selecting one chip over another.

Execution speed, although a prime spec for 8 and 16-bit machines, is not as critical a factor here since the processors will be performing dedicated functions. The only speed requirement will be: Is it fast enough to do the job?

PMOS developments are not limited to μCs—complete systems are still designed this way. TI, for example, developed the two major components for its Speak and Spell learning aid in PMOS. These two components, the speech synthesizer and the 128-kbit ROM, still have no equal in any other technology.

People are switching to Boschert



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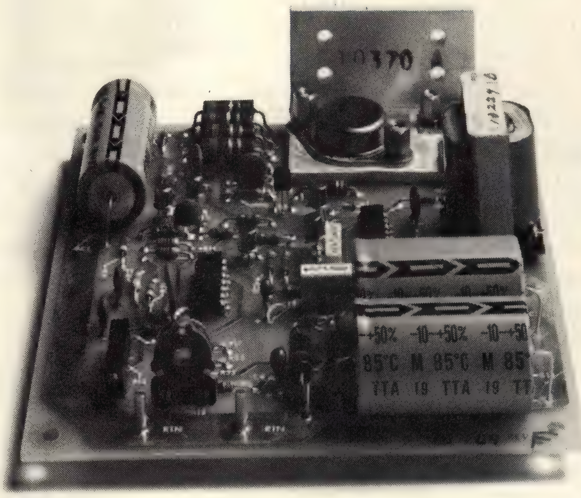

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With linear predictive coding, the synthesizer circuit (TMS-5100, Fig. 9) is controlled by a TMS-1000 μC that causes it to generate about 8000 signals per second. These signals act like air impulses created by the lungs. At the same time, the μC recalls a speech frame from the large ROMs and causes the digital codes to be translated back into analog form. Each frame in the memory consists of 12 numerical codes and represents a 1/40-of-a-second "freeze" of a spoken word, and contains information concerning the pitch and loudness (volume), as well as ten characteristics reflecting the shape of the speaker's vocal tract at that instant.

All the signals are combined by the synthesizer chip, which contains a ten-stage digital lattice filter that takes the vocal-tract characteristics and performs the operation equivalent to what the vocal tract does to air passing through it. The result is then passed through a d/a converter and finally fed to a speaker or amplifier.

High-density PMOS ROMs (TMS-6100s), two of which are use in the Speak and Spell, store the frames. In addition to holding 131,072 bits, each ROM contains a synchronous serial interface, an integral autoincrementing counter, an internal one-of-16 chip-select counter/enable, a 4-bit parallel load capability for address digits, and a 4-bit parallel-output option—all on-chip. Also, the ROMs have an indirect address capability and can provide a 100-kHz continuous data-transfer rate.

Meanwhile, National Semiconductor and several Japanese vendors, including Matsushita Electric, Hitachi and Fujitsu, have developed their own techniques for generating speech. Some, however, use NMOS technology, not PMOS, and some future products are expected to use CMOS to minimize the power consumption, especially in portable or hand-held applications.

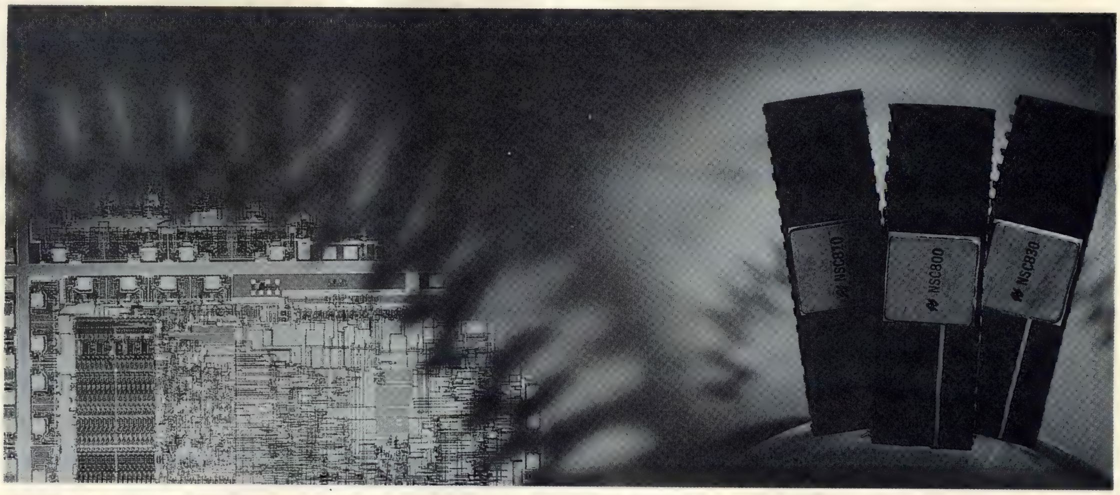
CMOS technology, long hailed as the technology of the future because of its extremely low power requirements and MOS packing density, has yet to fulfill that promise. The technology is still more expensive than NMOS or PMOS because of the additional production steps required, and because the final chip area ends up larger than comparable NMOS or PMOS designs.

Density improvements help

However, density has been improving ever since RCA (Somerville, NJ) introduced a structure called closed-loop CMOS. This eliminates the isolation wells around the devices, thus permitting almost a doubling of the density by permitting devices to be placed closer together. In addition, tighter lithography rules and better optical equipment permit circuit designers to obtain performance close to that of today's NMOS while retaining the advantages of CMOS.

Using its own process, called P²CMOS, National Semiconductor has developed both a family of high-performance general logic circuits and an 8-bit μP family (Fig. 10). Combining P-type wells, selective field oxidation, and self-aligned ion implants to optimize device topology reduces linear chip area between devices by about 50%. What's more, with a 30% device scaling, the final result is a chip with an area about half the size of guard-banded non-planar structures.

While P²CMOS requires about 20 to 25% more masking steps than NMOS, performance obtained with the process permits functions such as the NSC800, an 8-bit μP, and several LSI support circuits. Able to operate at clock frequencies of over 4 MHz, these circuits help keep the power low—at 4 MHz, for example, a system consisting of the NSC800 CPU and its two support chips, the NSC810 (RAM, I/O and timer) and the NSC830 (ROM and



10. Both 8085 and Z80 hardware features are combined with National's high-performance P²CMOS in the NSC800 μP and support family. At 4 MHz, the NSC800 and two support chips draw just 125 mW.

I/O) draws just 125 mW. A similar system built from NMOS components would typically require almost 20 times the power.

The NSC800 combines the best features of two other μPs—the basic architectures and instruction set of the Z80, but the external bus structure of the 8085. And like the Z80, the NSC800 has built-in dynamic RAM-refresh capability. Unlike the Z80's however, the NSC800's refresh has been extended from seven bits (good for 16-k RAMs) to eight bits (good for 64-k RAMs).

Many other companies are working on CMOS μPs and μCs with 4, 8, 12 and 16-bit data widths. The 4-bit area is populated by TI, National Semiconductor, Toshiba, NEC and Panasonic.

The 8-bit area is much smaller—Intersil (Cupertino, CA), Mitel (Ottawa, Canada), Motorola, National Semiconductor and RCA. Both Intersil and National are working on versions of the popular 8048 μs, while RCA is still trying to get its CDP1804 CMOS-on-sapphire (CMOS/SOS) μC into production and will then tackle the 8085.

Mitel, on the other hand has gone right after a μP—the Motorola 6802—which it will convert to CMOS and sample (it hopes) in the late third quarter. Motorola, having the technology in-house, has developed both NMOS and CMOS processors based on the original 6800 architecture. In CMOS, Motorola has crafted the MC146805; in NMOS, it has developed the MC6805. Basically the same, the processors provide pin-compatible interchangeability from the start of a design.

Power levels have been kept so low on the MC146805 that it can operate below 25 μA as well as at emergency power levels of less than 2 V. Indeed, designers at Motorola proved that a lemon could actually produce enough electricity to power the microcomputer for a day.

In the 12-bit CMOS area, the Intersil/Harris 6100 still reigns, and rumors have it that Harris is planning some extensions to the processor. Up in 16-bit, no U.S. manufacturer has yet to offer a CMOS processor commercially, although Mikros Systems (Albany, NY) has a CMOS/SOS version of its MK-16 processor in development.

However, at ISSCC, Fujitsu unveiled a 16-bit, single-chip 10,000-gate CMOS μP that dissipates just 130 mW when operated at 2.5 MHz. Fabricated using a silicon-gate, double-level metal process, the CPU offers an address range of 16 Mbytes and a machine cycle of 400 ns. To attain this level of performance, though, Fujitsu had to increase the chip size to about 400 mils on a side and house the device in a 64-pin dual-in-line package to provide the necessary I/O. Unfortunately, with today's current manufacturing capabilites, producing large quantities of chips that size would not be economically viable.

High-performance CMOS has also found its way into memory products. Hitachi, for example, has developed a CMOS equivalent to the Intel 2147—the HM6147P-3. Capable of being accessed in 55 ns, the Hitachi device consumes just 75 mW in the active state and a mere 4 mW in standby (the 2147 draws about 900 mW active, 150 in standby).

Other leading-edge CMOS products include the RCA, Harris and Intersil CMOS UV EPROMs, which offer power requirements of less than 100 mW active and less than 1 mW in standby. And, access times don't suffer—the CMOS devices offer less than 350 ns, except for the RCA units, which are specified at 1000 or 450 ns, depending on the model. Harris has also taken the CMOS technology into what was the exclusive realm of bipolar technology with the HM6641, a fuse-link CMOS PROM.

Just entering the sampling stage, the 512 × 8 PROM offers an access time of 150 ns—long for typical bipolar systems, but the intended applications are not too speed-dependent. Power dissipation is the shining star, though—just 50 mW when active and less than 1 mW in standby, as compared to over 800 mW for active bipolar units.

The promise of low-cost CMOS/SOS has yet to be fulfilled. Although more expensive than normal CMOS, CMOS/SOS offers many performance advantages—the insulating substrate reduces device capacitances in the circuit and thus permits higher operating frequencies at reduced power consumption.

Currently using CMOS/SOS for a 4-k memory, RCA is planning to use the SOS capability on its forthcoming CDP1804 single-chip μC.

HP has developed several different CMOS/SOS μPs specifically for use in some of its lower-cost minicomputer products. And, some of the CPUs are also used as peripheral controllers in equipment such as printers and terminals.

Rockwell has experimented with CMOS/SOS, and has developed three high-performance circuits for evaluation—a 12-bit analog-to-digital converter that operates in 2.5 μs, a frequency synthesizer capable of operating at 160 MHz while consuming less than 25 mW, and a Viterbi decoder that can pass a 127-bit pseudocode pattern when operating at 70 Mbit/s and consuming just 40 mW.

These circuits are fabricated using 3 to 4-μm channel lengths, which in turn yield average propagation delays of 1 to 2 ns and 600-fJ speed-power products. Future projections include channel-length reductions to 1 to 2 μm, speed power products dropping to 200 fJ, propagation delays cut to 200 ps, and a packing-density improvement to less than 1 square mil per transistor.□

CIRCLE NO. 31

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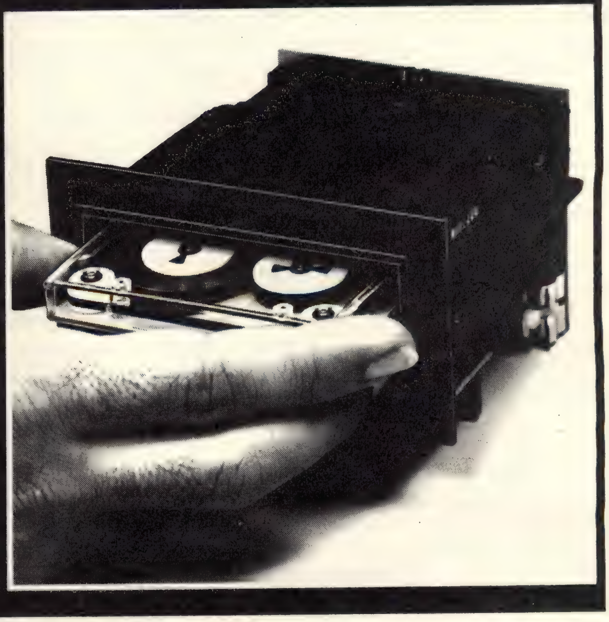

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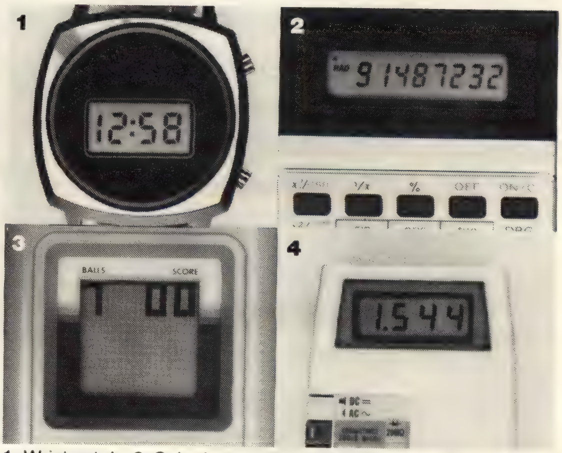

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CIRCLE NO. 35

Although higher-resolution ADCs and DACs are imminent, 8 and 10-bit converters keep on improving—with easier interfacing to μPs, simpler power-supply requirements and faster conversion.

Converters show off linear LSI processing

Whether bipolar or CMOS, the latest high-resolution, highly accurate single-chip data converters and precision op amps—the special products of analog LSI — will be smaller, faster and easier to use than ever before. For a/d and d/a converters, the integration of many parts on a single chip has ramifications beyond the savings in PC-board real estate. Integration entails more processing steps; yet the reduction in costs and design effort alone can be enormous.

With all its potential, the progress of monolithic integration has been slower than predicted. Monolithic 12 and 14-bit data converters attract attention; but the bulk of the manufacturing effort concentrates on adding conveniences, boosting speed and interface capabilities and lowering the power consumption of 8 and 10-bit converters. A new generation of integrated 8 and 10-bit DACs and 8-bit successive-approximation ADCs are coming on stream with easy μP interface, simple power supply requirements, and conversion times of 1 to 5 μs.

The majority of these 8-bit DACs and ADCs are the result of sophisticated linear-compatible bipolar processes which combine several devices—npn and pnp transistors, I^2L gates, buried zener (or, alternatively, bandgap) references, special diffused, zener-zapped or laser-trimmed thin-film resistors—all on the same chip.

CMOS converters have the advantage over bipolars in density, power consumption and compatibility with low-level logic circuitry. CMOS amplifiers do require offset compensation, and CMOS data converters require external references. However, the bilateral capability of CMOS switches allows CMOS DACs to be used in the "multiplying mode" for digital control of any analog reference signal, ac or dc. Though relatively slow, CMOS integrating ADCs have made possible a whole generation of digital panel meters and hand-held

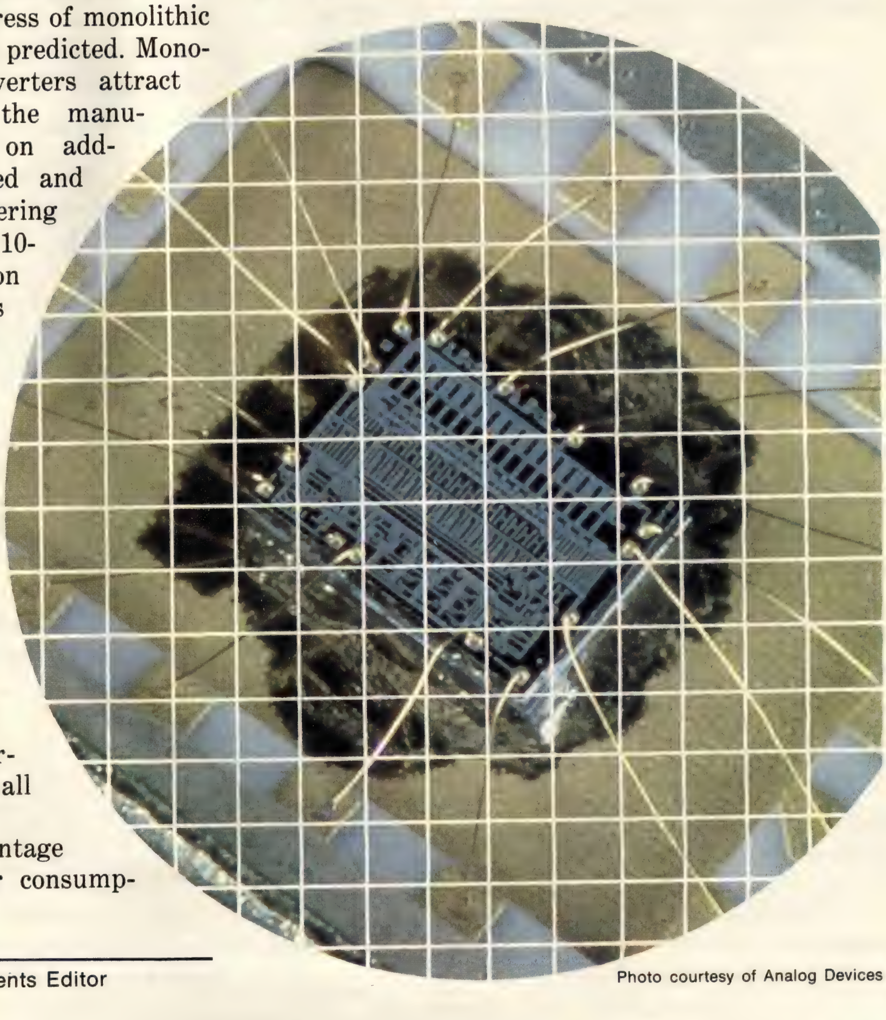


Photo courtesy of Analog Devices

Steve Ohr, Analog Circuits & Components Editor digital multimeters. The high packing density and logic-compatibility of CMOS ADCs will pave the way for data-acquisition components, with on-chip multiplexing circuits, microprocessor interfacing and memory.

Developments in parallel processing will pave the way for 10-bit video-speed converters by increasing the number of comparators without increasing the chip size or power consumption.

In op amps, bipolar technology is also passing old achievement thresholds. Power consumption, input bias currents and offset drifts have been cut to astonishingly low levels.

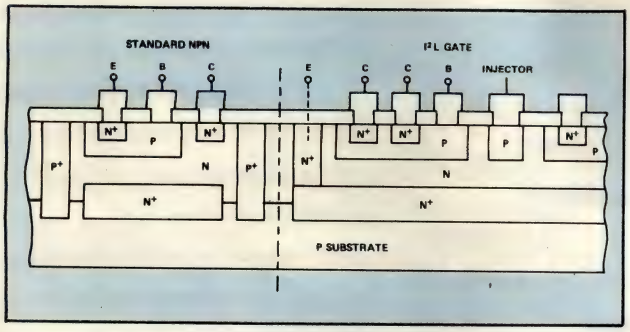
Linear-compatible bipolar

The special advantage of bipolar processing is its linear compatibility. Bipolar transistors make excellent high-gain, low offset amplifiers, and bipolar diodes make stable voltage references. Consequently, bipolar devices are best equipped to process the analog inputs and outputs of monolithic data converters.

But because bipolar devices tend to be large, they do not readily lend themselves to high-density, low-level, logic signal processing. Much of the work in monolithic integration focuses on achieving smaller data latches in monolithic DACs, smaller successive-approximation registers in ADCs and more accuracy from the bit-mapping resistors in both d/a and a/d converters.

One technique for meeting these goals, successfully exploited by Analog Devices (Wilmington, MA) and others, is Integrated Injection Logic (I^{2}L). The basic analog building block, the npn transistor, is inverted, so that its emitter acts as the collector of an I^{2}L gate.

Both the typical npn transistor emitter and the I^{2}L collector gate rest in a shallow p-type diffusion, which is the base contact of the device (see Fig. 1). However, the typical npn-transistor amplifier requires a wide separation between the deep p+ diffusion and the shallower area of the transistor to sustain high operating voltages. The I^{2}L gates do not require as much isolation between diffusions and take up less area on a chip, because they perform simple switching operations on logic-level signals, rather than amplification.



1. Mixing linear with logic: Shallow n+ diffusions in a p-type well form the emitters of *an npn transistor* amplifier or the collector of an I^{2}L gate. Lower voltages mean greater packing density for I^{2}L arrays.

All I^{2}L gates can be fabricated in one isolated p-type pocket. Fabricated with bipolar techniques and compatible with linear devices and process techniques, I^{2}L creates compact successive-approximation registers for ADCs and high-speed data latches for DACs.

One result of I^{2}L processing is Analog Devices' totally-integrated 8-bit DAC. First discussed at February's ISSCC (Electronic Design, Feb. 15, 1980, p. 49), the AD558 features I^{2}L data latches, an ECL control gate, pnp current sources, trimmed silicon-chromium R/2R ladders and a merged bandgap reference—all on the same piece of silicon. The result is an easy-to-use device with full microprocessor interface and with pin-programmable bipolar or unipolar voltage outputs. It will function on a single 5 to 15-V supply. Power consumption is approximately 10 mW from a 5-V supply (150 mW from 15-V). The output settling time for a ±½-LSB error is less than 1 μs in the 2.56-V range, and 2.5 μs in the 10-V range. Full-scale error for the device is typically ¼-LSB.

Bipolar d/a converters

The first μP-compatible 8-bit bipolar DAC came from Signetics (Sunnyvale, CA). Like the Analog Devices DAC, the Signetics NE5018 converter includes I^{2}L data latches, current switches, R/2R ladder networks and bandgap reference, on one chip. The offset of the on-chip buffer amplifier can be adjusted to provide unipolar operation over a range of 0 to 10 V, or bipolar operation over -5 to $+5$ V. Instead of a single supply, it requires dual 15-V supplies, though it draws less than 15 mA from each side.

Other bipolar 8-bit DACs, like those from Advanced Micro Devices (Sunnyvale, CA) and Precision Monolithics (Santa Clara, CA), require external references. The AMD 8-bit DAC provides full μP interface with the Am9080A, the Am2900 or other popular microprocessors. Though it provides 8-bit resolution, differential nonlinearity is specified as less than ±0.1%. The current output settles to within ±1-LSB within a fast 160 ns. Without a reference, however, the Am6080 can be used in the multiplying mode to control any analog input voltage at the reference input. The converter requires a dual power supply in the range from ±4.5 to ±18 V.

An industry-standard for fast 8-bit converters, PMI's DAC-08 requires a microprocessor interface and references, but settles to ±½-LSB within 85 ns.

While much of the activity in bipolar DACs centers on 8-bit parts, 10 and 12-bit DACs are gaining in accuracy and bit resolution. The Signetics NE5020 is a 10-bit version of the ground-breaking NE5018. It has all conveniences on-chip and settles to ±½-LSB to within 5 μs.

PMI recently announced a 10-bit-plus-sign monolithic DAC, the DAC210, that has a precision voltage regulator and output buffer amp built onto the chip (Fig. 2). Available in production quantities later this year, the DAC210 requires dual supplies of ±12 to ±18 V, to produce pin-programmable unipolar or bipolar voltage output. It settles to within ±½-LSB within 1.5 μs and provides full monotonicity from 0 to 70 C. Because the device responds to digital input currents as small as 2 μA, it is compatible with CMOS logic circuits.

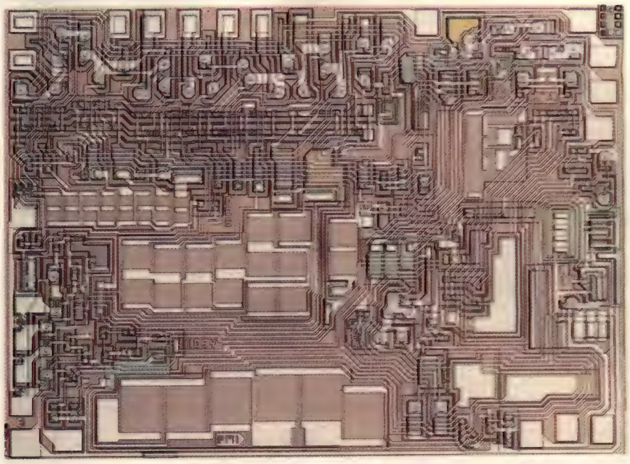
The 12-bit bipolar DACs include the Analog Devices laser-trimmed AD565. It is the DAC portion of the AD574, a two-chip, 12-bit successive-approximation ADC. AMD's trimless Am6012 provides full μP interface, with TTL, CMOS, NMOS or ECL inputs; 12-bit resolution with nonlinearity to within ±0.12%; and a settling time to ±½-LSB in less than 250 ns. Many DACs are following in the wake of the 565 and 6012, including the TP4068, a 300-ns 0.10% nonlinear DAC from Teledyne Philbrick (Dedham, MA).

Harris Semiconductor (Melbourne, FL), whose wafer processing provides dielectric isolation between the junctions of bipolar devices, is currently supplying the HI-562 12-bit DAC with a current output and a 300-ns settling time. In development is a monolithic 12-bit DAC with a buried-zener reference.

To trim or not to trim

Though bipolar DACs from Analog Devices, AMD and PMI lead the field in terms of bit-resolution and accuracy, this accuracy is contingent on matching the R/2R resistor ladders on-chip. Traditionally, the R/2R ladders perform the bulk of the bit summing and scaling operations in d/a conversion. The currents reflecting the most significant bit (MSB) and the least significant bit (LSB) must show a linear relationship to each other; therefore, the heads and tails of the R/2R ladder must track each other closely —a task that becomes more difficult as the bit resolution increases.

The resistor ladder may occupy more of the chip, and the ratios between the components on the ladder are hard to maintain. Laser-trimming becomes necessary to alleviate these problems, though it introduces manufacturing steps and elevates the cost of the part. Because the resistive film tends to seep into the surface of the silicon during high-temperature diffusion, resistors cannot be trimmed without damaging the silicon substrate underneath.


2. Bipolar processing can put precision voltage regulators and output buffer amps on the same chip with resistors and current switches to produce high-resolution DACs, like this one from PMI.

One way out of this dilemma is to connect resistor areas with a series of metal links which rest only on the surface of the silicon. Trimming then involves merely clipping the metal links. In a similar technique pioneered by PMI, these links are constructed as miniature fuses and trimmed by "zener-zapping;" that is, by selectively blowing the fuse links. With both of these techniques, the increments in trimming are defined by the metal links.

For continuous laser-trimming, the resistive material is made of chromium or aluminum thin-film which rests on the surface of the silicon. This approach is pursued with good results by Analog Devices with the AD558 8-bit DAC and the AD565 12-bit DAC.

An entirely different approach is taken by AMD with its Am6012 μP-compatible 12-bit DAC. The part combines elements of the traditional R/2R ladder with weighted current sources. Fewer resistors are required, and they can be made by diffusing aluminum onto the silicon at 1000 C. The resulting network provides high stability on silicon and shows good initial matching with traditional microlithography techniques. AMD claims an untrimmed accuracy of 12 bits and a differential nonlinearity of ±0.012% for the Am6012.

Because of the difficulty of matching the required characteristics of resistor network components on the silicon chip, many manufacturers of hybrid converters—such as Hybrid Systems (Bedford, MA), Micro Networks (Worcester, MA), Datel Intersil (Mansfield, MA), Burr-Brown (Tucson, AZ) and Beckman (Fullerton, CA)—and many manufacturers of monolithic parts still rely on multichip designs for high-resolution DACs. A typical two-chip hybrid design incorporates all elements of the DAC on a single piece of silicon, with the exception of the R/2R ladder, which is a separate precision thin-film or Bulk-Metal resistor network.

Bipolar a/d conversion

The very same bipolar processes that produce high-speed and accurate DACs have also given birth to a new generation of complete monolithic ADCs that use successive approximation. In addition to a DAC, the monolithic ADC must incorporate a comparator and successive-approximation register, internal references, scaling resistors and clock and control logic. The conversion time should be fast enough so the microprocessors need not wait for data after requesting a conversion.

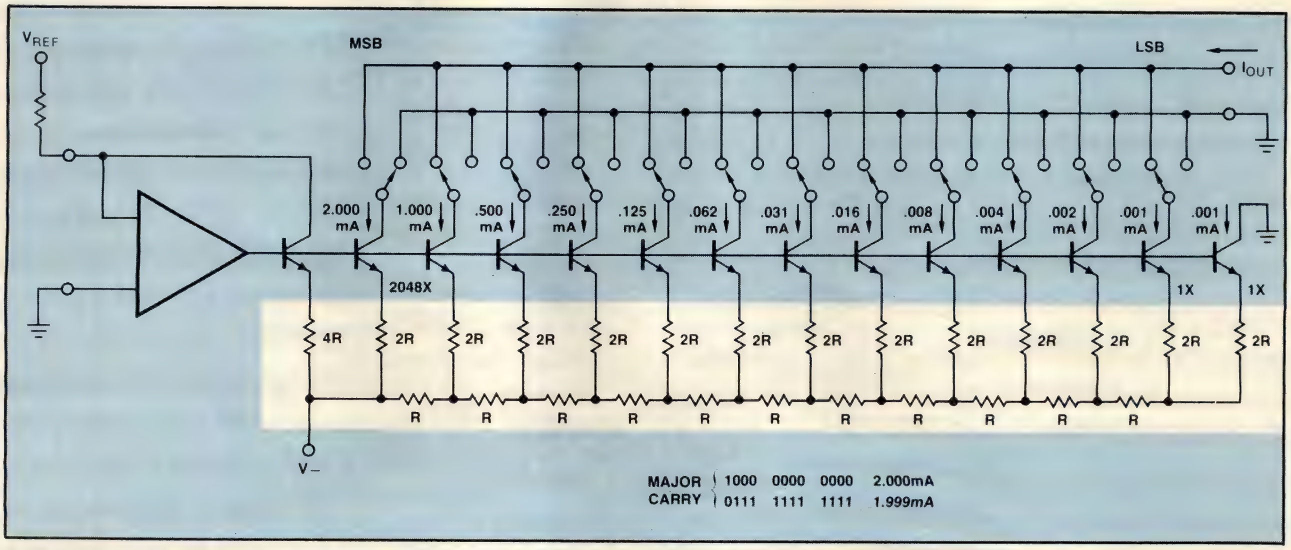
Once again, the field is led by Analog Devices with the AD570 8-bit ADC and the 10-bit AD571. The AD570 provides references and full μP-interface, and completes a conversion within 15-μs. The AD571 converts in 25 to 30 μs.

The TDC10013, a high-speed monolithic 8-bit converter from TRW LSI (Redondo Beach, CA), provides binary-coded TTL outputs, which are linear to within ±½-LSB, and converts within 400 ns. The device contains a precision DAC, a successive-approximation register (SAR), output data registers and controls, but requires an external clock and voltage reference. It is constructed with triple-diffused bipolar processing (see Fig. 4). The resistor ladders are deposited on-chip. Though tolerances for the resistor networks are necessarily broad, matching is close enough to achieve 8-bit conversion without trimming. TRW is currently developing another successive-approximation ADC, which also provides 10-bit accuracy without trimming. Announcements are expected later this year.

Waiting closely in the wings is a totally integrated monolithic 8-bit successive-approximation converter with a conversion speed of 900 ns. Soon to be announced by AMD, the device has DAC, SAR, high-speed comparator, stable bandgap voltage reference and resistor networks all on the same chip. It operates on dual ±5 V supplies, accepts unipolar input voltages from 0 to 10 V or 0 to 5 V or bipolar inputs from −5 to +5 V, and interfaces directly with most microprocessors. The 102 × 140-sq-mil chip employs a variation on ECL called Linear Differential Logic (LDL), specially trimmed R/2R ladders and dual-layer metallization. It is not an easy part to make.

Signetics is readying two successive-approximation parts. The 6-bit device, another product of I^{2}L bipolar processing, will function from a single power supply and will provide parallel and serial output data from a mini-DIP package. The 8-bit converter will have all conveniences on-chip (including clock, reference and output buffers) and will perform conversions within 17 μs.

While many of these parts have been discussed before at technical conferences and in technology updates in magazines, they have not yet appeared on the market. The delay, according to Signetics' product manager Phil Marcoux, may occur because the market lags behind the technology (e.g., the industry wants 8-bit parts while semiconductor manufacturers are trying for 12), but more likely, because complex parts (like monolithic 8-bit or 12-bit successive-approximation converters) are difficult to



3. Without weighted current sources or specially diffused resistors, traditional R/2R resistor networks perform bit-summing and determine the accuracy of a DAC. Resistors for high-resolution monolithic converters usually require large chip areas, close tracking and specialized trimming procedures.

make. The chips exist, but wafer yields are small, and the resulting parts are likely to be at very top of the learning curve in cost. Semiconductor manufacturers may feel it is not economically sensible to offer the largest parts for sale at that stage.

However, 12-bit resolution and accuracy are obtainable from multichip devices, such as the two-chip AD574 successive-approximation ADC from Analog Devices. One chip comprises a 12-bit DAC and 10-V reference (packaged and sold separately as the AD565). The other chip comprises a successive-approximation register, comparator, clock, control logic and three-state buffer. One reason for utilizing two chips is that the thin-film resistors and deep n+ diffusions needed for I^2L can be processed separately.

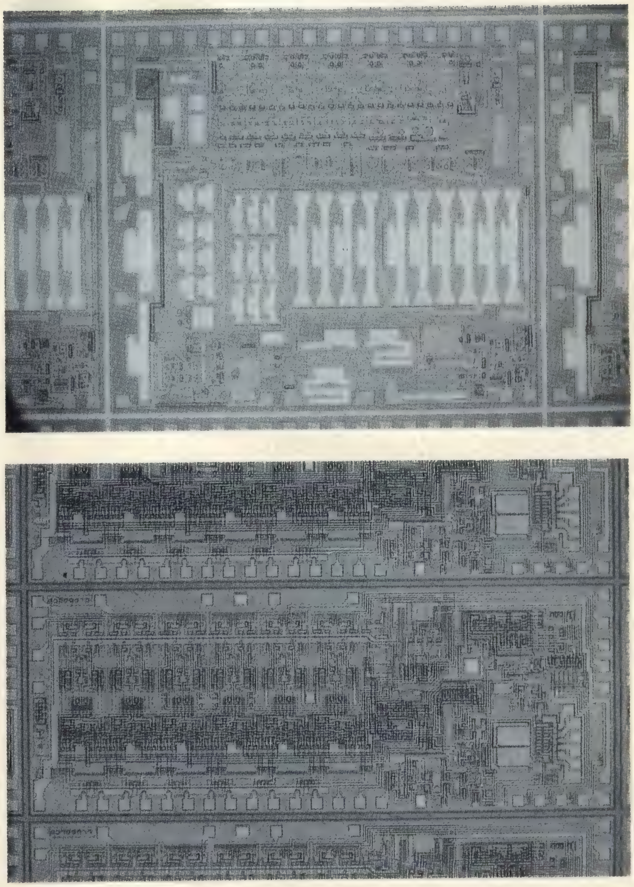
Since I^2L gates can be stacked, the TTL DAC inputs of the AD574 interface directly to the I^2L gate on top of the layer containing the SAR and clock. All the I^2L gates on a single injector operate within the voltage drop of one diode between the injector and the common emitter line. The ADC interfaces directly with 6800 or 6502 μPs without any intervening components. The two-chip design will likely become a monolithic part within the next year.

Parallel processing for video-speed conversions

For video-speed conversions, ADCs that use successive approximation—the comparison of bit to bit in sequence—are too slow, even when the devices are bipolar. Thus, ADCs rely on parallel processing for these conversions. Parallel processing requires a separate comparator for every voltage level the converter can resolve. For high resolution, hundreds of comparators may be needed. For 8-bit resolution, parallel processing involves $2^8 - 1$ comparators, or 255; 10-bit resolution demands 1024 comparators. Parallel processing, therefore, translates into large devices that absorb a lot of power (Fig. 5).

The best example of a flash converter is TRW LSI's TDC1007J. This 8-bit monolithic ADC appears in video applications, radar signal conversion and high-speed multiplexed data acquisition circuits. It digitizes signals at speeds up to 30-million samples per second. Without a sample-and-hold circuit at the front end, it accurately converts analog signal frequencies up to 7 MHz. (The 3-dB point of the comparator is actually 40 MHz).

The ADC consists of 255 comparators and an output buffer register which produces a TTL output within 20 ns of a full-scale step input. Outputs can be either straight binary coded or offset two's complement (true or inverted). Power consumption is the main bugaboo with high-speed converters: The TDC1007J dissipates more than 2 W in a 64-pin ceramic DIP.



4. High-resolution successive-approximation converters are frequently made in multichip form. Analog Devices' 12-bit ADC uses two chips: the AD565 DAC (top) and a separate I^2L SAR (bottom).

For DACs, which use successive approximation, yet another problem is presented by video-speed conversions. The binary-coded digital input components must be summed to the required output signal. The two most popular methods—superimposed weighted current sources and R/2R ladder networks—either compromise resolution or consume too much power.

TRW LSI has found a solution in the form of a summing network that combines both methods to derive each LSB and generates most of the MSB components with the R/2R ladder. However, the first and second MSB are generated by weighted current sources.

The combination technique, according to TRW LSI's Peter Rohr, requires one-fourth the current consumed by the R/2R ladder alone. The significant savings in power dissipation provides a space savings as well, because the current-supplying transistors can be smaller.

TRW's innovation appears in the TDC-1016J, a family of video-speed 8, 9 and 10-bit DACs. The high-speed converter accepts TTL or ECL digital inputs at 20 million samples per second. Neither a data register nor a sample-and-hold unit are needed. The device provides an analog voltage output, and consumes less than 0.6 W of power from ±5-V power supplies. Packaged in a 40-pin DIP, the TDC-1016J provides nonlinearities well within 0.05% (for the 10-bit part) and is useful for color video applications and CRT display generation.

While TRW LSI has emerged as the leader in video-speed conversion, Plessey (Santa Ana, CA) will shortly introduce several high-speed parts. The most significant of these is an ultra-fast DAC. First discussed at February's ISSCC, the Plessey part is a monolithic 8-bit DAC with a settling time of 5 ns to ±1/2 LSB. The DAC has complementary current outputs and can be driven in a multiplying mode with a 3-dB bandwidth of 40 MHz.

This device requires a high-speed process that gives good component matching. Plessey uses an ion-implanted process with a peak F_Ts of 5 GHz—what Plessey Director Dennis Chant calls "a 5-GHz process"—and resistor matching of better than 0.1%. The base-emitter offsets of the small transistor pairs are centered on zero, with a standard deviation of 0.2 mV. The process is, therefore, well-suited for high-speed data conversion.

The process uses a 2.6-μm epitaxial layer with implants for base and emitter. Base width is typically 0.15 μm and emitter depth is 0.3 μm. Auto-registered contacts and photoresist masking of implants raise both speeds and yields.

A bandgap reference—rather than a buried zener—pnp devices and thin-film resistors establish an on-chip precision voltage reference. A fast comparator on-chip speeds up the successive-approximation conversion. The propagation delay of the comparator from input to output is less than 1.8 ns, with less than 1.3 ns for output latching.

Also, keep an eye open for the American introduction of Siemens' AG (Munich, West Germany) SDA-5010 6-bit a/d converter with a 10-ns conversion time. The monolithic bipolar device has a 100-MHz scan frequency, provides ECL compatibility, ±¼-LSB linearity, operates from logic-level supply voltages, and dissipates a mere 450 mW in a 16-pin DIP package.

Doing it in CMOS

Although bipolar has the advantage in speed and process versatility, CMOS has the advantage of small device structure, low-power consumption and high packing density. Because CMOS switches are bilateral, CMOS DACs can handle multiplying functions. Both digital and analog functions can be placed together on the same chip, making CMOS a good medium for a/d and d/a converters. The CMOS parts are usually much less expensive than comparable bipolars.

High-resolution ADCs using integration techniques (rather than successive approximation) have been successful in digital multimeter applications and other digital display applications which do not require high speed. Typical converters in CMOS are showing 12-bit-plus-sign resolution (0.01% nonlinearity) with complete microprocessor compatibility. Because no trimming is required, cost is minimized and power consumption is generally in the vicinity of 20 mW at ±5 V.

A groundbreaker among CMOS converters is Intersil's (Cupertino, CA) ICL7106 3½-digit BCD converter. This monolithic part heralded an entire generation of low-cost hand-held DMMs. For data acquisition, Intersil's more sophisticated CMOS ADC, the ICL7109 is a 12-bit part with a conversion time of 20 to 50 ms.

Despite its many other advantages, a CMOS part cannot accommodate all of the circuit functions that a converter needs. At present, an accurate stable reference can not be built on a CMOS chip. Bipolar parts can utilize buried zener or bandgap references on chip, but the CMOS parts can not. As a consequence, an external precision reference is usually required along with the CMOS converter itself. Also, CMOS amplifiers have a tendency to drift, so CMOS application notes are built around a growing arsenal of techniques for autozeroing or otherwise maintaining the accuracy of CMOS converters. One technique is quad-slope conversion, patented and put to use by Analog Devices for their own digital display converters.

Quad-slope integration takes off from dual-slope integration. The converter is cycled through two additional phases intended to track and eventually subtract the drift product.

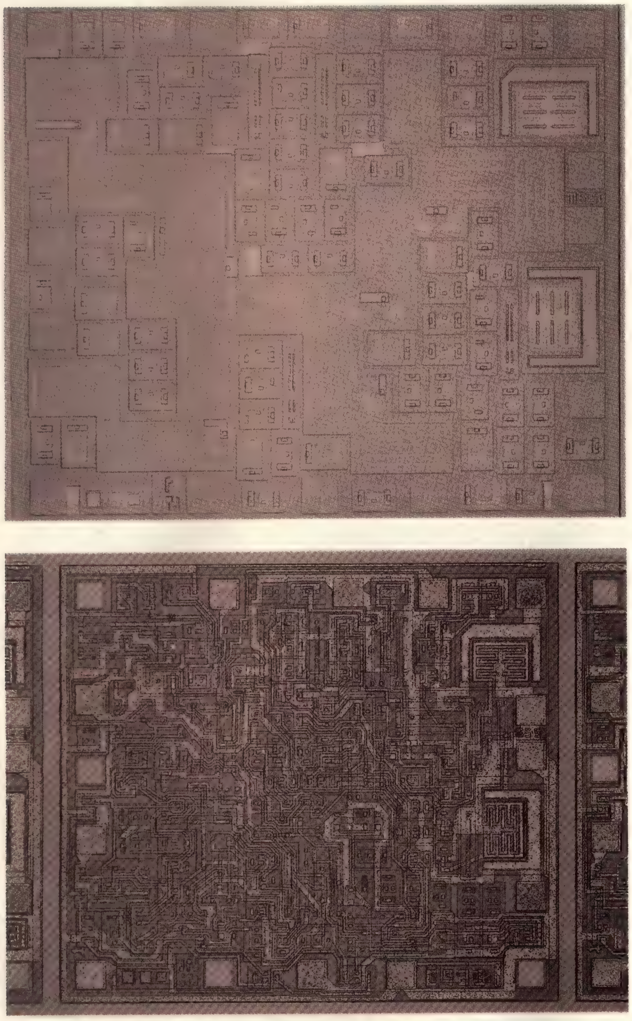
In ordinary dual-slope conversion, the comparator output shot is contingent on the relationship between the ramp rate of an input voltage on an external capacitor and the ramp rate of a reference voltage on the same capacitor. When a CMOS device drifts, it affects the ramp rate. The higher the input voltage, the faster the external capacitor should charge, but drift shifts the time at which charging takes place.

Under quad-slope integration, two ramp rates are measured: one for input voltage and one for the offset voltage. The latter is clamped as the former begins a zero crossing. Offset drift is held constant over time and temperature.

Analog Devices applies this technique in its AD 7550 converter. The device provides 13-bit resolution, functions from a single supply voltage and consumes less than 50 mW power, making it ideal for hand-held battery operated DMMs. Conversion time is approximately 400 ms. Also coming is a 5½-digit CMOS a/d converter for bench-type DMMs.

Integrating a/d conversion techniques have been put to good use in digital panel meters. However, CMOS a/d converters rely on successive approximation in data acquisition. Here, multiplexing or sample-and-hold circuits freeze the analog signal at the input until the entire conversion cycle is completed.

CMOS processing paves the way for analog and extensive signal processing on the same chip. Data acquisition components can carry multiplexing or sample-and-hold circuits, memories and even microprocessor units on-chip.



5. Processing transistors, diodes and switches on a standardized form (top) and then metallizing to the user's specs (bottom) provides rapid turn-around for Exar's semicustom linear ICs.

CMOS successive-approximation converters, like the ADC0800 series—the "naked eight"—of National Semiconductor (Santa Clara, CA) require external bit-mapping resistors, clock and references, but enjoy the advantages of low cost (less than $2.00 in quantity), low-power consumption (from a single 5-V supply) and direct interface with most popular microprocessors, such as the 8080, Z80 and 6800. New additions to the ADC0800 series (the ADC0808 and the ADC0816) have 8 and 16-channel input multiplexer circuits right on the chip. The conversion time is less than 100 μs to ±1.5-LSB. Tristate buffered outputs ease the connection to data buses.

Also coming on stream is NEC Microcomputer's (Wellesley, MA) μPD7001, an 8-bit CMOS ADC with four-channel analog input multiplexer and serial data output. The μPD7002 is a 12-bit converter with four-channel multiplexer, binary coded output and 2.5-ms conversion time.

As discussed at this year's ISSCC, National Semiconductor has a totally integrated monolithic successive-approximation CMOS converter. The 12-bit-plus-sign ADC includes laser-trimmed PROMs (which provide precision bit-slice data for two on-chip 6-bit DACs), a high-speed sampled data comparator, successive-approximation register, output buffer, timing and control logic. The laser-programmable memory devices (LPROMs) are programmed by scribing built-on thin-film fuses right on the chip.

Sampled data techniques that are possible only with CMOS prevent overloading of the comparator and improve its accuracy, response time, stability and noise. In operation, the ADC looks at analog voltages from the input and at voltages generated by a pair of on-chip DACs. Each 6-bit DAC generates a matrix of 64 analog voltages from a single positive reference supply. Outboard capacitors scale the multiple differential voltages for the comparator input, and successive-approximation signal routing provides a ±½ LSB comparator response within 50 μs.

The sign of the differential inputs is determined by the sampling rate, relative to an autozero time at the comparator. This procedure eliminates the need for 13-bit generation. The monolithic device consumes just 25 mW from the total power line; interfaces directly to popular microprocessors, such as the 8080, Z80 and 6800; and is virtually impossible to make with current bipolar processes.

Analog and digital processing on the same CMOS chip opens up other possibilities: Data acquisition components can be designed with sample-and-hold circuits on the front end and with on-chip memory. A device like this is under development by the Analog Device's CMOS unit in Limerick, Ireland. First described at this year's ISSCC, the monolithic CMOS part will multiplex eight channels, make 8-bit a/d conversions and place the information for retrieval in an on-chip 8 × 8 dual-port RAM.

Another device which takes full advantage of CMOS is an American Microsystems Inc. (Santa Clara, CA) microprocessor chip, with 8-bit a/d and d/a converters at each end. The AMI S2210 is a 4-bit μC. Its on-chip memory consists of a 2048-word 8-bit ROM (expandable to 8192 words with additional programmable memory) and a scratch-pad RAM for 64 4-bit data words. Each a/d and d/a converter comprises 8-bit resister string arrays (which require no trimming) and a high-speed clocked comparator. The chip is expected to be 48,400 sq mil and contain approximately 25,000 separate devices. CMOS will keep the power consumption down.

New op amp achievements

Not all the progress in linear LSI has been in a/d or d/a converters. New processing developments in bipolar and CMOS op amps have cut offsets, input bias currents and power supply requirements to a minimum.

Bipolar technology has previously given birth to high-gain op amps like National Semiconductor's LM10, which can operate on supply voltages as low as 1 V and supply currents less than 270 μA. The supersensitive LM11 requires input offset voltages of about 100 μV and input bias currents of 25 pA.

PMI recently introduced a precision op amp, the OP-20 that functions on a single power supply of 3 to 30 V, with supply current draw of approximately 30 μA. Input offset voltage is specified as 80 μV; bias current is typically 13 nA and 20 nA, max. Input offset voltage drift is less than 1.0 μV/°C. Both common mode rejection and power supply rejection approach 110 dB. Single-supply operation not only lowers power consumption, but also lets the input signal swing down to the negative rail. Recently introduced, the OP-420 is a quad amp version of the OP-20. It features single-supply operation from 5 to 20-V supplies, with a total current draw of less than 220 μA.

Bipolar processing provides dielectric isolation between the transistor and diode junction, resulting not only in low-noise op amps, but also in devices that are useful at ambient temperatures up to and beyond 200 C. Op amps from Harris Semiconductor, in fact, have been independently characterized for operation up to 300 C. The HA-2600 internally-compensated op amp, for example, provides a small input offset voltage at elevated temperatures: −0.25 mV at 25 C, +0.5 mV at 125 C, +1.0 mV at 200 C and only +2.0 mV at 300 C. Maximum input bias current is only 30 nA at 200 C, and the voltage gain is better than 50,000 V/V. These parts are useful for oil-well logging and other hi-temp applications.

Junction FET devices are implanted on bipolar chips by many manufacturers to create high-gain and high-input impedances. The FETs so implanted are typically p-channel devices, which require isolation from the negative rail.

A process recently announced by Texas Instruments (Dallas, TX) allows n-channel FETs to be constructed in an implanted p-well. The result is the TL090 series of N-FET op amps, the first junction FET op amps that can operate from a single supply voltage of 5 to 10 V and process analog input signals at or near the negative rail. Input offset voltages for the new series are 5 mV and input bias currents are far less than those of previous P-channel FET amplifiers. Input bias currents for the P-channel TL084 BiFETs are typically 400 pA; the new-N-channel equivalent has an input bias current of 50 pA. The first member of the N-FET series is the TL094 quad amp. Dual-channel and single-channel versions of N-FET amplifiers will be announced later this year.

Other manufacturers of bipolar-JFET amplifiers include National Semiconductor PMI, Motorola (Phoenix, AZ) with its Trim-FET amplifiers, Analog Devices with TriFET, and RCA (Somerville, NJ) with BiMOS. Bandwidth for these devices is typically in the 3 to 5 MHz range, noise is 25 to 30 nV/Hz and input bias currents are 50 to 200 pA. The FET input amplifiers usually require dual power supplies ranging from ±5 to ±15 V.

CMOS breakthroughs

Bipolar devices have always made the best amplifiers, but complementary MOS provides inherently low cost and low power consumption. Because CMOS amps are subject to drift, their appeal was limited until the introduction of commutating autozero compensation. The ICL7600 series from Intersil uses outboard capacitors to correct for the low-level input offsets in transducer or thermocouple junction amplification and other data acquisition situations.

In principle, the CAZ amp is two op amplifiers: At any given moment, one processes the analog input signal and the other serves a reference, applying a charge to the outboard capacitor that is equal to the offset. CMOS switches reverse the amplifier connections at the commutating frequency. The charge on the outboard capacitor with polarity reversed is then applied to the signal processing op amp, correcting for the offset. Initial offset for the CMOS amplifier is 1 to 5 μV, with drift less than 0.005 μV/°C over temperature, and less than 0.2 μV over the course of a year.□

DP Dialogue

Notes and observations from the IBM Data Processing Division that may prove of interest to the engineering community

Oshkosh Truck custom designs and builds vehicles like this airport crash-fire-rescue truck. Delivery can be as quick as 100 days because CADAM helps produce error-free engineering drawings fast.

CADAM® Means Quick Turnaround for Heavy Trucks

Most of the large all-wheel-drive vehicles made by Oshkosh Truck Corporation are custom engineered. Even those based on standard designs are substantially modified to meet individual customer needs.

But fast delivery of the company's vehicles for construction, crash-fire-rescue, in-transit concrete mixing and similar heavy-duty tasks is vitally important. As Ron Gehrke, manager of engineering administration points out: "Quick turnaround – sometimes in 100 to 190 days – is one of the things the customer is paying for. CADAM has drastically cut both the manhours and the elapsed time required to produce the engineering drawings."

The Computer-Graphics Augmented Design and Manufacturing (CADAM®) system runs on an IBM System/370 Model 135 at the company's Oshkosh, Wisconsin, headquarters. In the fabrication of sheet metal parts, Gehrke explains, CADAM has eliminated engineering drawings as a source of error.

Often, the metal stock that must be bent into complex curves is a half-inch thick. Today, to calculate the geometry of the flat equivalent of these parts and draft the patterns by which the stock will be cut, Oshkosh Truck uses CADAM.

"Since we installed CADAM, we have yet to see one drawing come back with errors," Gehrke says. "Because these parts are so complex, we were eating a lot of scrap costs even though we were double-checking. Frequently, we resorted to welding two simpler pieces – which is costly, but cheaper than making scrap."

On the average, he reports, there is a four to one saving of manhours on detail drawings. "The saving in elapsed time is even greater, because CADAM enables us to add late shifts. Many designers prefer the late hours, because they can get easier access to CADAM.

"We see the strongest gains when we are revising a drawing. The designer calls it up on the screen of an IBM 3251 Graphic Display Station and modifies it with a light pen. Once when a customer wanted the fuel tank moved back 12 inches, the designer changed the assembly drawing in five minutes. In general, on engineering changes our manhour gains are 12 to one."

Oshkosh Truck will sometimes "stretch" a vehicle by increasing the frame length, Gehrke notes. Previously, the draftsman changed the dimensions noted on the drawing, without changing the drawing itself. The resulting out-of-scale layout opened the possibility of errors; with CADAM, the line work is as easily stretched as the dimensions.

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ADRS Passes the Test at Roche Clinical Labs

Blood specimens are prepared for thyroid function test. Managers at RCL do their own planning and analysis, with the aid of IBM's A Departmental Reporting System (ADRS).

"Users are getting the answers the need – promptly," says Kim C. Frank o Roche Clinical Laboratories, Inc. "Wit ADRS, people throughout the compan are solving their own problems withou our help, and our programmers are free t concentrate on our primary busines systems."

Frank is operations/technical suppor manager of the Raritan, New Jersey, subsidiary of Hoffmann-La Roche Inc. A leading clinical laboratory, RCL accept blood and other specimens from physicians in many states and performs the tests they order. An IBM System/370 Model 148 collects the test results and transmits them via telephone links to IBM 3770 Communication Terminals in 24 regional offices.

Users from managers to secretaries at RCL have learned to work with A Departmental Reporting System (ADRS), an IBM program product that enables them to structure a wide variety of formatted reports and analyses. A data interface program lets them write ADRS programs that take advantage of existing computer files.

"With a small programming staff, we can't always respond to users' needs fast enough," Frank notes. "Now managers, professional people and secretaries invoke ADRS directly through 3277 Display Stations."

Among the personnel using ADRS is James P. Halligan. As director of distribution services, he is in charge of the field organization that collects the samples from local offices and then transports the finished reports from the regional facilities to the local offices. He uses ADRS to analyze route structures for a fleet of 225 vehicles.

Good Management Tool

"It's a tremendous management tool," he states. "We've improved gas utilization, done travel-time studies, prepared budgets, and tracked costs and revenues. The system stores anything I want – lists of drivers' names and addresses, vehicles, routes, and collection stations. And airline schedule data. We can shape the information as people need it. We invest less time and get better information."

In the purchasing and material control department, people use ADRS to track the consumption of supplies, analyze the materials costs of specific tests, and maintain purchasing and vendor files. Still other active users are found in the payroll, finance, security and maintenance departments.

"Some of these applications," Frank says, "would have taken months if developed conventionally, by system analysts and programmers."

Accelerating Vehicle Design at Clark Equipment

"It has brought in enthusiasm and taken the drudgery out of design." Jack Squier of Clark Equipment Company is describing the Computer-Graphics Augmented Design and Manufacturing (CADAM®) system. "Under the old method, when you got an idea, you stopped thinking for 4½ hours while you drew a picture."

Squier is manager of new product development for Clark's Industrial Truck Division, headquartered in Battle Creek, Michigan, which makes lift trucks and related vehicles. The division wants to accelerate the design on new model families. "CADAM has cut the cycle by at least a third," he states. "We can make a layout in one day that would have taken five or six.

"CADAM enables us to build better engineering prototypes. It eliminates most drawing and arithmetic errors, and gives us more flexibility in trying alternatives and modifying a design."

To illustrate, Squier cites the case of an assembly drawing of a truck which had to be lengthened by one inch. "It would have taken 15 weeks to lengthen all the tubing, wires and frame members," he points out. "With CADAM, the designer made the changes with a few strokes of the light pen and touches to the keyboard."

Another interesting design problem is a wheel that moves up and down as it is steered, in order to keep the truck horizontal. To verify that there were no interferences, they needed to define the external envelope of its motion, and this required plotting its geometry at half-inch increments. This was completed in three hours at the IBM 3251 Graphic Display Station by a man with two weeks of CADAM training, Squier states. "It would have taken 2½ weeks at the drafting board.

"We can do more accurate layouts, showing more details. It's easy to duplicate and erase a drawing, creating multiple copies of a basic layout for different purposes. CADAM helps us assure that parts can be assembled."

Adds Jim Bauer, vice president of engineering for the division: "CADAM is so productive we can't afford *not* to extend it to other industrial truck engineering locations in Kentucky and Germany."

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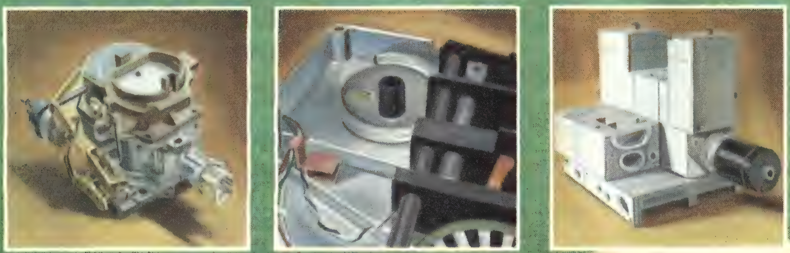

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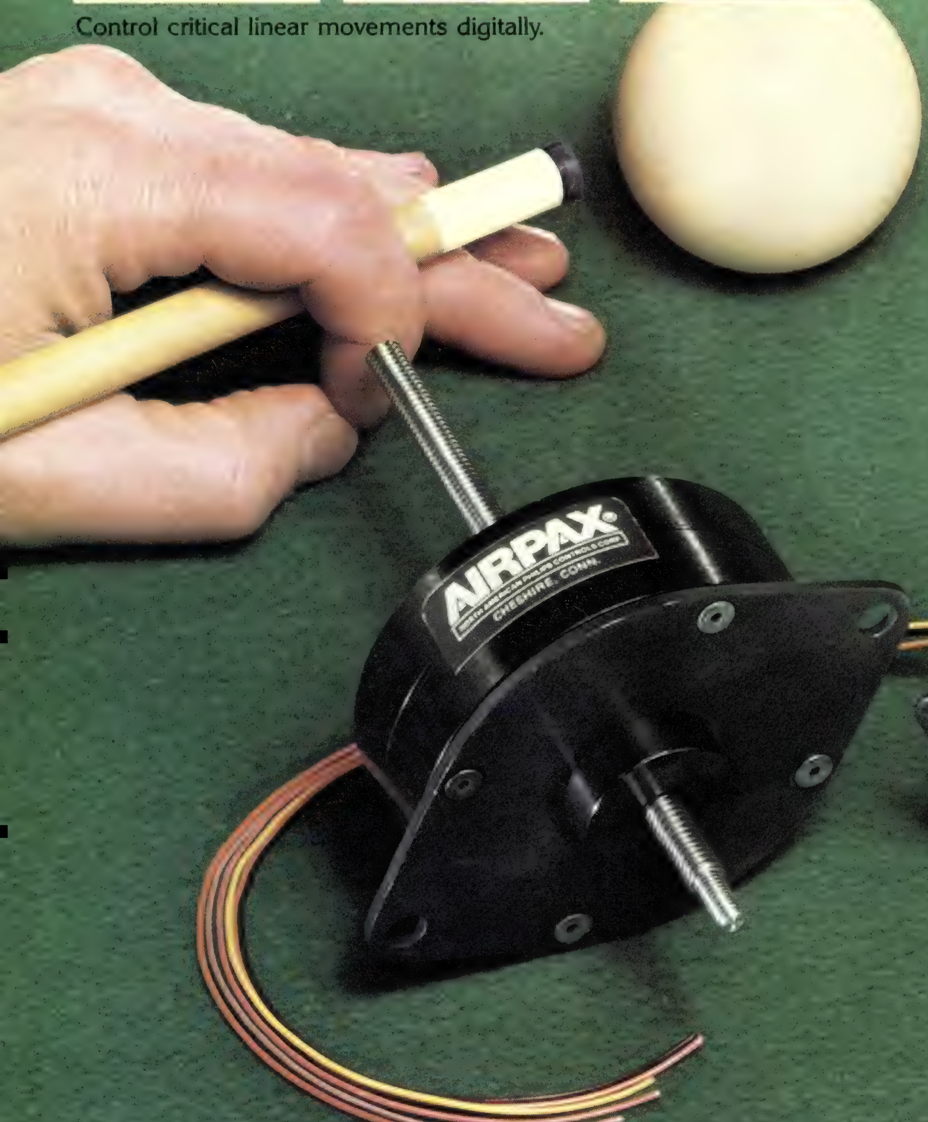
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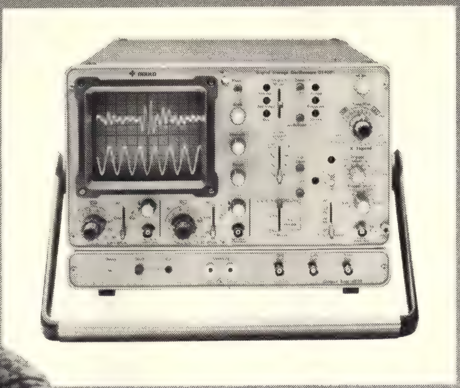

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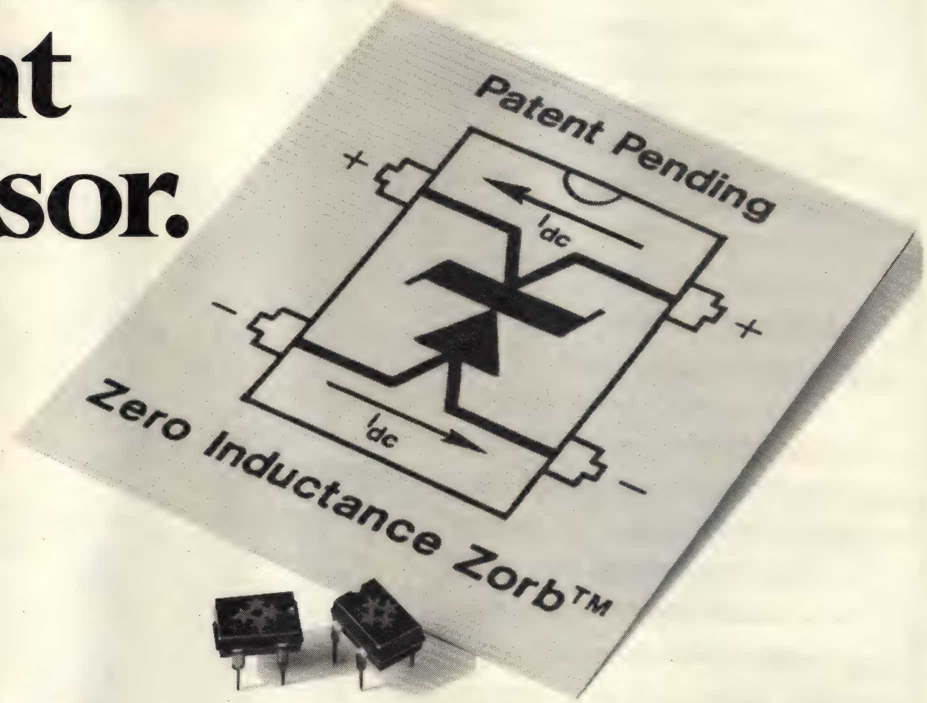

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For telecomm chips, the route to better performance, reliability, size, power and cost lies in processing, material and circuitry; for data-comm chips, the key is basically architecture.

ICs ride the tidal wave of data comm, telecomm

The demand for more information traffic is tapping virtually all aspects of IC technology. While data-comm chips rely primarily on architecture, tele-comm chips rely on processing, materials and circuitry, for improvements in performance, reliability, size, power and cost. Designers in data comm and telecomm often use microprocessor and memory chips for programmable functions. But there ends the similiarity between most data-comm and telecomm ICs.

Data-comm, or line-protocol control chips, organize, control and supervise data for transmission over serial channels. Hence, most data-comm chips are entirely digitial. Data-comm chips are almost always cast in dense digital MOS circuitry. Chip designs differ in architecture, programmability and the number and depth of the protocol(s) that are handled.

Most telecomm chips contain both analog and digital circuitry for the specialized functions peculiar to transmission over voice-grade phone lines. For fabricating telecomm-ICs, new processes and circuit arrangements are under continuous investigation in the critical areas of breakdown voltages, power consumption and dissipation, dynamic range, noise immunity, die size (and its corollary, cost), linearity and bandwidth. Telecomm chips receiving the most attention today are:

- Subscriber-line interface circuits (SLIC)
- LSI codecs and their associated filters
- PCM repeaters
- Crosspoint arrays.

Perhaps the most technically demanding of the telecomm chips from the viewpoint of circuit design and process technology is the subscriber-line interface circuit. Certainly, it has been the longest time in coming. The technologies applied to SLIC encompass junction-isolated bipolar, BIDFET, dielectric isolation and MOSFET processing.

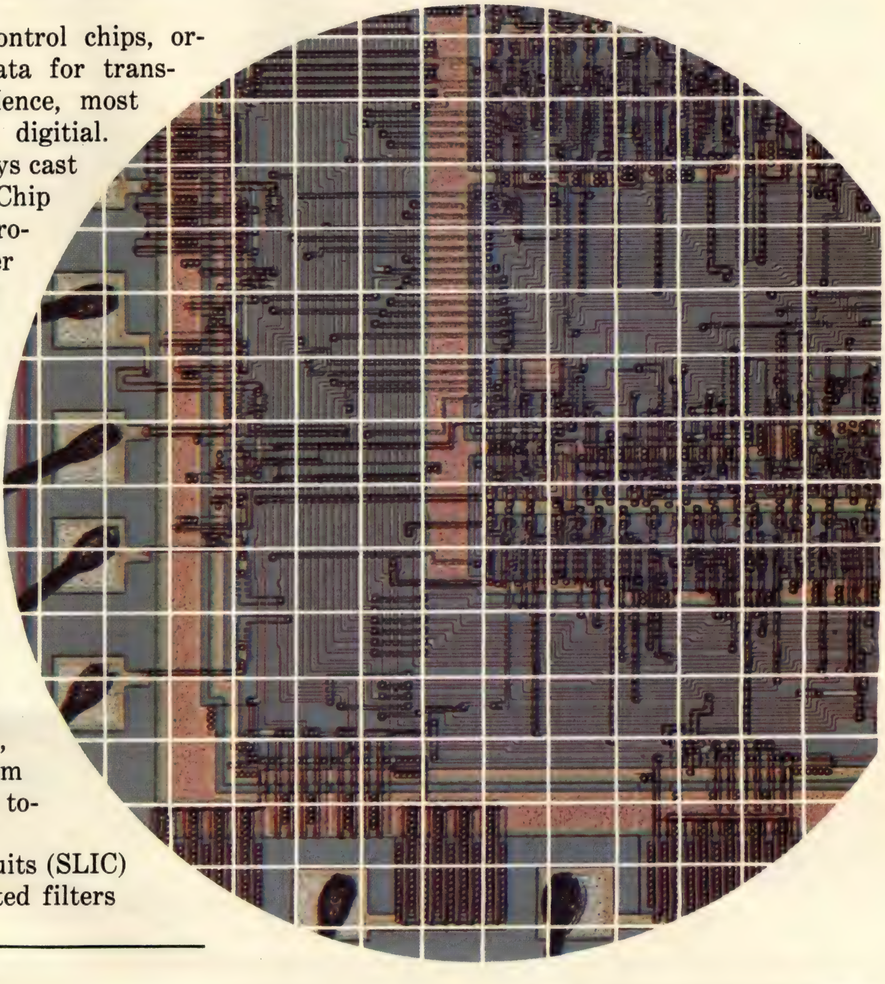


Photo courtesy of Standard Microsystems

Sid Adlerstein, Communications Editor

Among the major functions the SLIC must perform are: two-wire to four-wire conversion, battery feed, switch-hook detection, supression of trans-hybrid loss and longitudinal-signal balancing.

Opinions differ as to whether the SLIC chips should, or even can, include ringing voltage generation, secondary protection from high-voltage, high-current stresses (a result of lightning or power-line crosses), and test functions. (For a description of these so-called BORSCHT functions, see Electronic Design, April 12, 1979, p. 86).

Glen Haas, Telecommunications Strategy Manager at Texas Instruments (Dallas TX), observes that many projected SLIC chips contain only parts of the total package needed, and that trans-hybrid-loss and longitudinal balance have long been stumbling blocks. He cautions equipment designers to evaluate the cost completely before committing themselves to any particular chip on the basis of its range of functions.

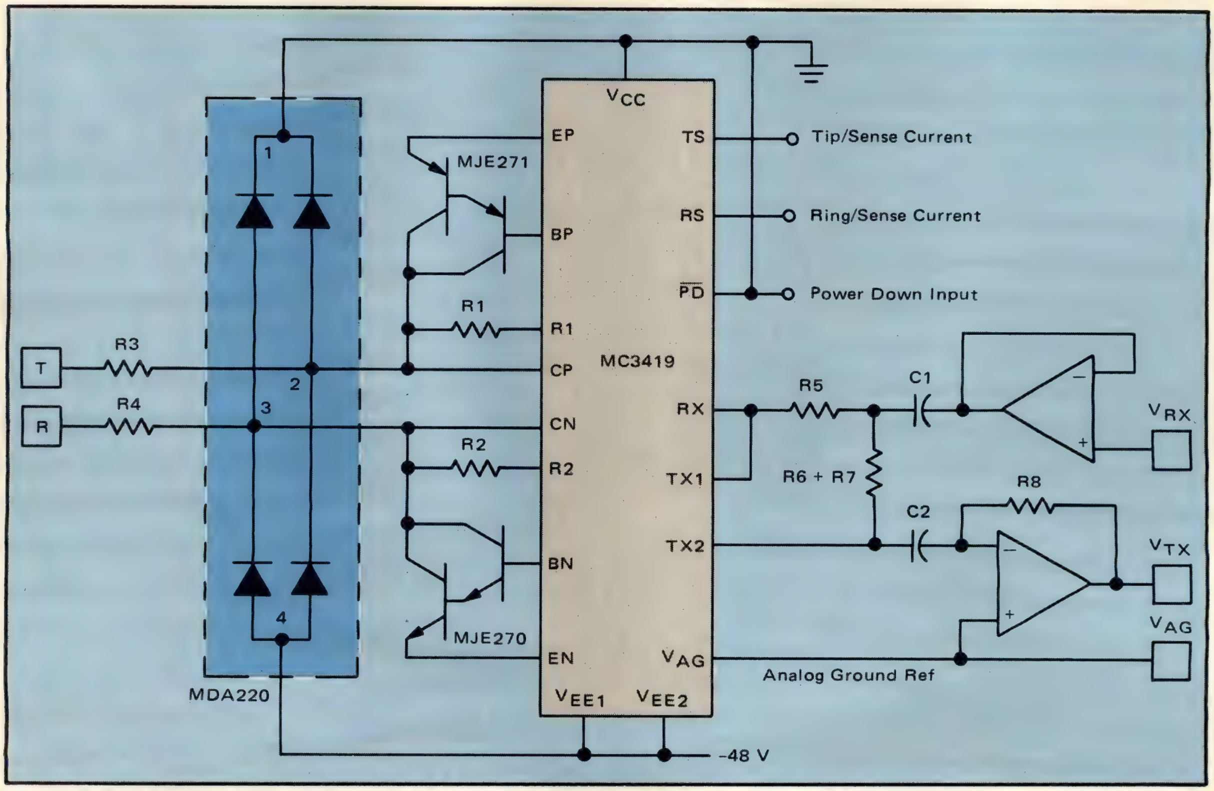
BIDFET takes a total view of SLIC

Investigation at TI applies BIDFET technology to address the functional needs of the SLIC, all at once, instead of part by part. BIDFET processing combines bipolar, double-diffused MOS and CMOS circuitry on the same chip. Haas projects that one chip might furnish the high-voltage, high-current capability required at the telephone-line interface along with the low overall power and the closely matched switched-capacitor components for balancing trans-hybrid loss and longitudinal signals. In spite of BIDFET's promise, TI has considerable respect for the problems in making an IC SLIC. So far, the company has not indicated *when*, or even if, such a part will be forthcoming.

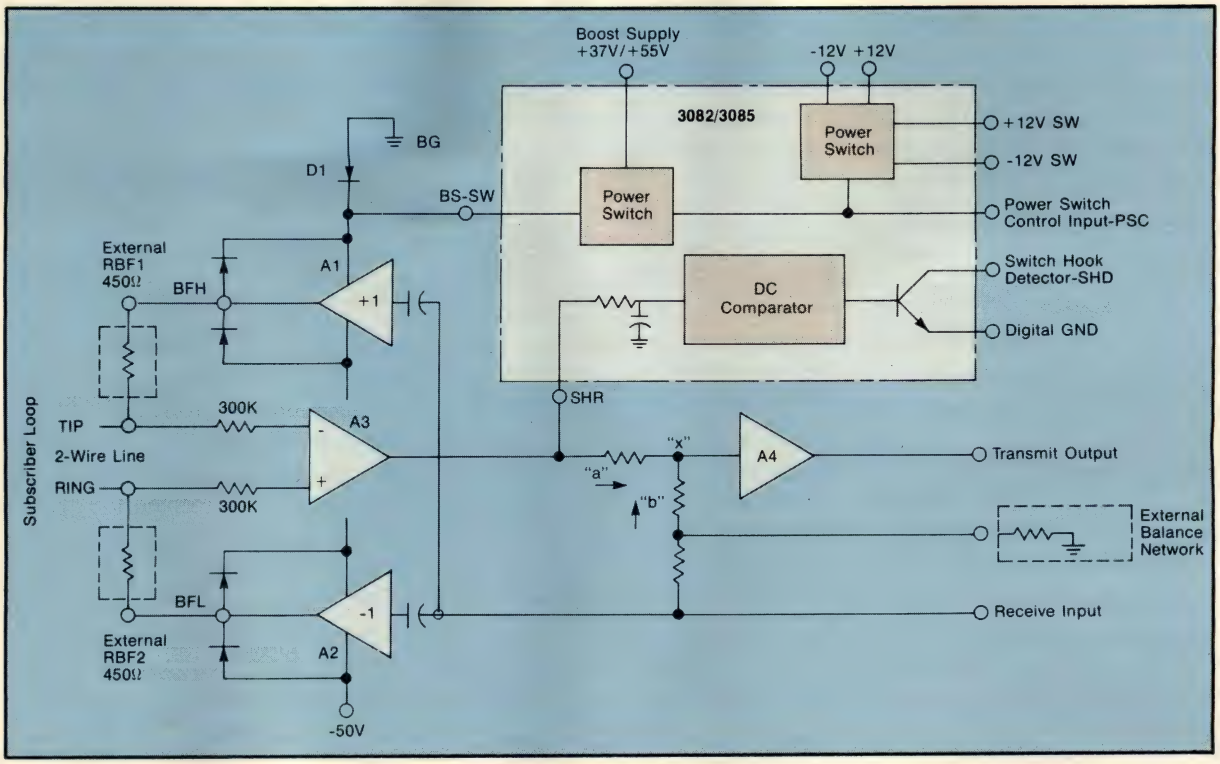
Driven by another technology, Motorola has another viewpoint. The long-awaited MC 3419 (Fig. 1), using buried-antimony bipolar circuitry, is scheduled for introduction later this year.

According to Bill Carns, New Product Planning Manager at Motorola's bipolar production facility (Mesa, AZ), the laser-trimmed SLIC chips will contain circuitry for two-wire to four-wire conversion and for feeding power to the handset. On-chip testing and fault detection, on-hook power drain of no more than 5 mW and off-hook status outputs are to be additional features of Motorola's first generation SLIC. Future generations will offer on-chip control of the ringing signals, which can go to 140-V peak, and secondary protection from transients due to lightning strikes and power-line crosses.

One problem in designing IC versions of SLICs has been the lack of empirical data on how all-electronic (transformerless) solutions behave in actual telecomm circuits in the field. Thus, ITT Microsystems



1. The diode bridge and 30-Ω resistors in the Tip and Ring leads protect Motorola's bipolar laser-trimmed SLIC chip (MC3419) from transients created by lightning and power-line crosses. The Darlingtons control longitudinal balance. Load balancing is performed by the RX and TX circuitry.



2. An LSI chip will soon incorporate many of the active circuits in ITT's hybrid all-electronic SLIC set, the 3081/2. Reliability and cost should be improved by substituting the Value Engineered Line Circuit chip into the hybrid.

(Deerfield Beach, FL) has an advantage, since its hydrid, all-electronic SLIC sets, the 3081/2 and 3084/5 (Fig. 2), have logged lots of operational data.

Armed with the results of this in-service check, ITT Microsystems has completed a Value-Engineered Line (VES) Circuit, that combines both LSI and thick-film technology. An IC replaces parts on the hybrid substrate. On the substrate, the precision resistors can be laser trimmed, and the high-power capability of the circuit remains intact. Samples of the VES microcircuit are scheduled for the first quarter of 1981. Large-quantity production should follow in the next quarter. The MSI could be manufactured in ITT's West German facility.

The IC development and, indeed, the entire hybrid SLIC are components of ITT's complete line interface circuit (CLIC) program. The CLIC effort will create a hybrid microcircuit that performs five major functions:

- Battery feed to the two-wire lead
- Two-wire to four-wire conversion
- Transmit and receive filtering
- Codec
- Switch-hook detection.

The CLIC can interface between a telephone handset at the subscriber end of a local analog loop and a digital switch in a Class-5 central office. The switch then connects to the PCM highways of long-haul digital transmission.

In an example of international cooperation to develop an IC version of the SLIC, the bipolar dielectric-isolation (DI) processing of Harris (Melbourne, FL) takes on the circuits patented by France's Telecommunications Radioelectriques et Telephoniques (TRT). High breakdown voltages are one result of the process. Bipolar elements made with DI can withstand strains in excess of the 140-V peak that the (68 to 105-V rms) ringing signal can reach. Hence, the ringing-signal control and the two-wire to four-wire electronics can connect directly in one IC, without fear of breakdown. A balanced linear output amplifier that connects directly to the TRT line hybrid should go a long way toward solving the trans-hybrid loss problem, without requiring closely controlled resistors.

DI enhances frequency response

One advantage of replacing the usual magnetic multiwire transformer (hybrid) with electronics, is enhanced frequency response. Usually, small transformers severely attenuate low frequencies. However, the high-frequency response may become important, if data are to be transmitted directly in digital form. Harris knows that the amplifiers in its hybrid can easily pass 9.6 kbits/s; they are expected to handle 50 kbits/s without trouble.

Longitudinal balance also calls for closely matched resistances and requires high-power dissipation.

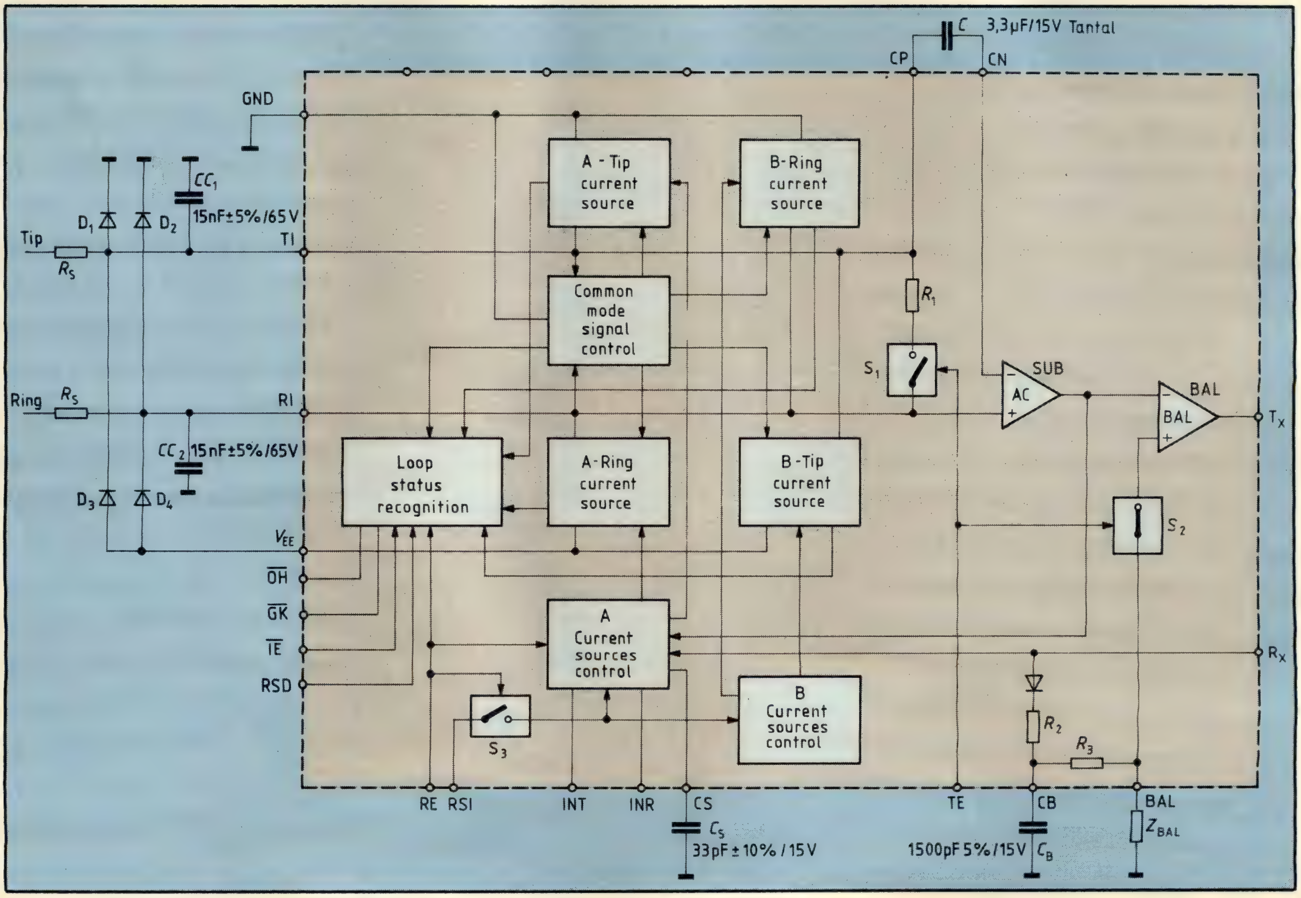
Most SLIC designers use the transmission-line solution: matching the line impedance. However, TRT uses a circuit-designer's approach to common-mode rejection. This solution shorts the longitudinal current and cancels any power build up. TRT's method avoids the expense and inefficiency of adding external precision power resistors.

Feeding the battery voltage through the chip becomes relatively simple with the aid of the high breakdown voltages of DI. The main telco battery simply connects resistively through the hybrid to the subscriber line. Unfortunately, this method wastes power in the current-limiting resistor. An active circuit is more efficient. The usual active circuit proposed for battery feed is a charge-pump, or floating-feed, type. The TRT patent gives Harris yet another efficient option that is supposed to be simpler than a floating feed, but the details are still closely guarded.

The Harris IC will operate under µP control. The system processor could add features like variable-frequency ringing. Tests programmed through the µP might revise the present telecomm testing dogma, predicts Charles Riehm, Communications Products Manager at Harris. Now only 200-V steps satisfy test requirements.

While the DI process supplies the Harris chip with protection from power-supply and ringing-voltage damage, even more protection is needed. Secondary protection anticipates high currents and voltages from the lightning strikes and power-line crosses that telephone lines fall prey to. Primary protection from such catastrophies is afforded by telco-installed gas-discharge tubes and carbon blocks. Harris does not now plan to package secondary protective devices within its SLIC. However, the company will define and characterize the means for secondary protection that are appropriate for a particular circuit. Further, Harris will recommend the proper parts to use.

Harris expects the high-performance SLIC chip to be priced competitively with passive circuits. The basic chip, without any added testing functions and without controller or secondary protection will cost about $10. Volume production is slated for late 1981,



3. Bipolar technology and laser-trimmed, on-chip resistors allow Siemens' G150 subscriber-loop interface circuit to operate from normal telephone-battery power: −48 (+6, −10) and +5 V. The chip feeds the *line* with a constant 23 mA, performs two-wire to four-wire conversion, injects the ringing signal, monitors the line for on or off-hook conditions, detects Ring and Tip status, disables the feeding control and suppresses longitudinal current imbalances. Secondary protection is relegated to external passive components.

Double-polysilicon CMOS for PCM codec and filter ICs

The manufacturing process for PCM codecs and filters affects how well these parts will meet such design objectives as low power, noise immunity and cost (die size). The double-poly CMOS process was originally developed to improve the density of such digital devices as CMOS memories, logic and μPs. Double-poly processing, as the name implies, places two layers of polycrystalline silicon on the field oxide over the p and n devices. Conventional n-channel and CMOS Si-gate MOS processes use only a single layer of polysilicon.

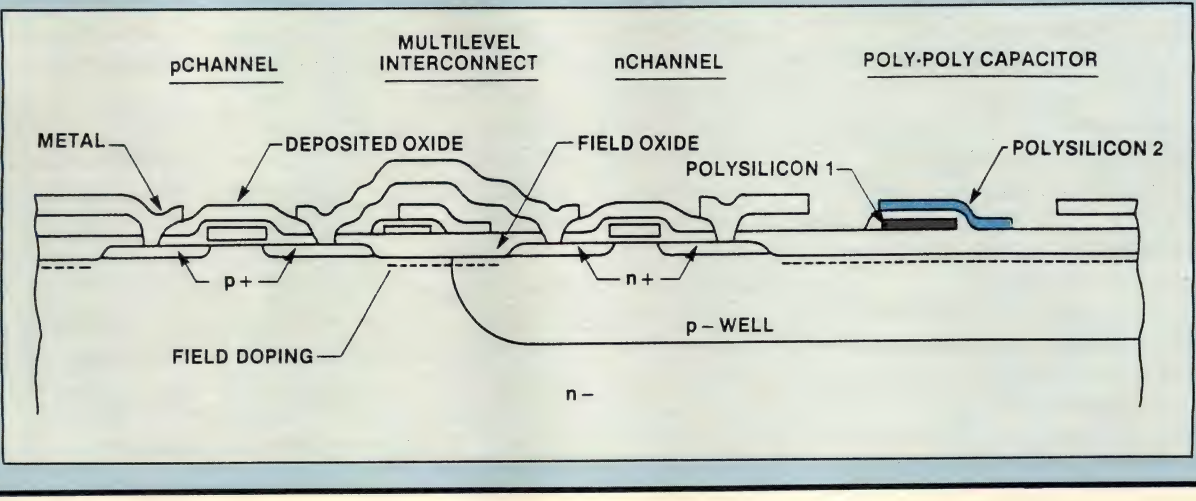
As the cross-section shows, two levels of moderately low-resistance interconnect are available. Circuit density and speed and noise shielding are all better than with conventional single-layer processes. The cost of the additional steps in the double-poly process is more than offset by the lower cost of the smaller die.

Fortunately the advantages of double-poly CMOS are not confined to digital circuitry. Significant benefits can be gained by applying the technology to analog or mixed analog and digital circuits. One of the most important is a high-quality capacitor built using polysilicon for both plates, with oxide as the dielectric. Poly-to-poly capacitors exhibit temperature coefficients as good as NPO ceramic capacitors and have negligible voltage coefficients. Furthermore, capacitor ratios can be held more precisely and parasitic capacitances kept lower than with poly-to-silicon, metal-to-silicon or other types of IC capacitors.

Double-poly capacitors are ideal circuit elements for the design of capacitive, a/d converters. Capacitive converters relieve some of the voltage-coefficient and ratio-matching problems of purely resistive a/d converters. When applied to active, voiceband, ladder filters, the switched capacitor technique gives long time-constant integrators by simulating very large-value resistors. Thus, pole-zero location depends only on capacitor ratios and the accuracy of the sampling clock frequency. The resulting filters are both stable and cost-effective.

Double-poly capacitors can be built in any MOS process. However, CMOS contributes several features important for telecomm circuits. In addition to low-power dissipation in its static logic, CMOS creates high-performance operational amplifiers. With both p and n-channel devices, the op amps get the benefit of lower noise figures and higher power-supply rejection ratios. Furthermore, CMOS offers a band-gap reference that is less dependent on processing than the threshold-differencing type offered by NMOS. CMOS analog switches operate in a balanced manner. Double-poly CMOS is a proven flexible process.

(Much of the above information was supplied by National Semiconductor Corp., Santa Clara, CA.)



though samples are expected soon. Harris hopes to have a CMOS one-chip codec-plus-filters to accompany the SLIC. Even a CMOS echo-canceller chip is possible.

Another European SLIC, the G 150, is to be made with junction-isolated (JI) bipolar technology by Siemens of West Germany (Fig. 3). Though not as immune to breakdown as a DI chip, the JI bipolar unit can work with power supplies up to the required 58 V. JI bipolar technology has never been famous for producing compact chips and this one is no exception—it is larger than 43,000 mils^2.

When the loop handset goes off hook, the SLIC —under control of the received voice signal—drives a constant 23 mA through to the handset microphone. Laser trimming adjusts the chip's thin-film, nickel-chromium, temperature-stable resistors to within 0.1% for balancing the trans-hybrid loss to

±0.1 dB. Other features packed into the chip include a complex resistor network for longitudinal-balance control, ring-signal injection, line monitoring, detection of faults to ground, ring/tip detection, disable-feeding control and loopback.

The chip's typical power dissipation of 750 mW is well below the 2 W that Siemens considers acceptable. Since most handsets are on hook most of the time, the average power is to a great extent determined by the chip's 20-mW standby power drain. Siemens recommends a four-diode bridge and two resistors for secondary protection up to 1 kV. Functional samples are expected at year's end; full production will begin in mid-1981.

Ion-implanation cooks up BORSCHT functions

Ion-implanted bipolar technology, along with thin-film resistors, is the technology that will provide the notorious BORSCHT functions according to chip designers at Precision Monolithics (Santa Clara, CA). Other techniques are not likely to produce the closely matched resistors PMI engineers feel are the best way to control longitudinal balance and trans-hybrid loss. Though external components will probably be needed for secondary protection and high-power feed, PMI feels that the bipolar circuitry will at least be able to withstand the −48-V station battery.

Another conservative approach to SLIC design is on the drawing board at Mitel in Ottawa, Canada. The unit will most likely combine an IC and discrete components made with some form of bipolar processing, into a single-in-line hybrid. The bipolar processing offers the needed high voltage and current capability. But power MOSFETs might also make a contribution, says Mod Hammad, Marketing Director, at Mitel in San Diego, CA. Hammad indicates that the company already has a SLIC operating in the PBX, but this environment does not compare to that of a central office. Mitel does have a design that Hammad feels will meet the central-office requirements. However, if the commitment were made today to produce the unit, volume production of a central-office quality SLIC would be at least six months away.

Manufacturers strive toward single-chip SLIC

In spite of all the SLIC development now in progress, a full IC version—a true single-chip SLIC—may be years away. After studying the SLIC requirements and matching them to possible high-voltage processing technologies, Fred Kamp, Telecomm Manager at Siliconix (Santa Clara, CA) estimates that at least three years of development and considerable investment will be needed to produce a complete SLIC chip. New technology is needed if the chip is to interface directly to the analog line.

The first stage of a complete chip, both for central-office and PBX use, should contain high-voltage analog switches that would replace the relays now in use. Kamp would place the two-wire to four-wire hybrid after the switches. With the relays replaced, the line hybrid is within reach of today's technology: ITT and Northern Telecomm have electronic hybrids in phones now, TI and others will announce similar devices soon, and Mitel has joined the list with its unit for PBXs. Also, Siliconix is considering the development of a two-wire to four-wire converter for handsets.

Back at the central office, the requirements are harder to meet with today's technology. The main problems are isolating the converter circuitry from the high ringing voltage, the battery feed, lightning and power-line crosses. Kamp feels that an analog switch, capable of standing-off 400 V, would do.

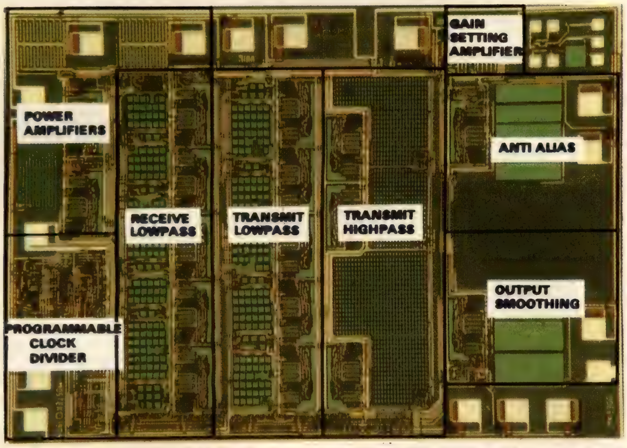
Such a circuit was described by Peter Shackle, High-Voltage Design Supervisor at Bell Labs (Murray Hill, NJ) at the ISSCC this year (see ELECTRONIC DESIGN, Feb. 15, 1980). Indeed, Bell's gated-diode switch (GDS) can block up to ±500 V, withstand 1-A surges and switch the loop dc that passes from the 48-V station battery to the handset.

A GDS consists of three interconnected semiconductor elements: a JFET, an npn transistor and a pin diode, all on a polysilicon substrate. The bidirectional blocking feature comes from connecting two GDS cells back-to-back with a common gate. A third cell is used to break conduction, once started.

Kamp says that Siliconix can make a circuit now with equivalent performance to the GDS. However, there is one major hurdle to overcome—size. Siliconix found that one single-pole single-throw GDS cell spreads over more than 6000 mils^2 of die area. At this rate, just two three-cell switch elements would take up all the area of a good-sized chip.

Siliconix is looking into technology for combining high-voltage and current capability with density. Perhaps an SOS process or true DI would fill the bill. Kamp thinks that improved processing could shrink GDS elements to a quarter of their present size. Then several double-pole double-throw switches and the line hybrid could be shoehorned onto one chip. In this way, a true IC SLIC could be made, including secondary-protection diodes or resistors, active or passive battery feed, longitudinal balancing resistors and the line hybrid. For example, processing that develops good isolation could place high-voltage analog switches on one section of the chip and dense low-voltage logic for the hybrid in another section. Perhaps, speculates Kamp, a good approach would be to create islands for the separate functions.

Improved processing techniques and information gained from previous generations of the telecomm



4. As extended by Mostek, NMOS technology provides a low-power, low-noise PCM filter chip. Compact analog and digital functions, executed in NMOS circuitry, make the MK5912 by far the smallest of the single-chip PCM filter ICs.

ICs are also upgrading per-channel codec filter chips. For one thing, codecs and filters are being combined onto one chip. Though highly confident that the single-chip versions will yield well once in production, most companies have not yet admitted their impending introductions.

Filter joins codec on CMOS chip

An exception to the silence is General Instrument (Hicksville, NY). GI's single-chip filter and codec will be produced in silicon-gate CMOS. This technology offers dense, fast logic and low power for the chip's analog and digitial circuits. The codec section will use the delta/sigma modulation approach that GI developed in its previous work on separate codec and filter chips with England's Telecommunications Authority, the British Post Office. As before, the filtering is to be digital. Thus, the chip will be partitioned more towards digital logic than towards analog circuitry. GI expects to have prototypes for sampling in the final quarter of 1981.

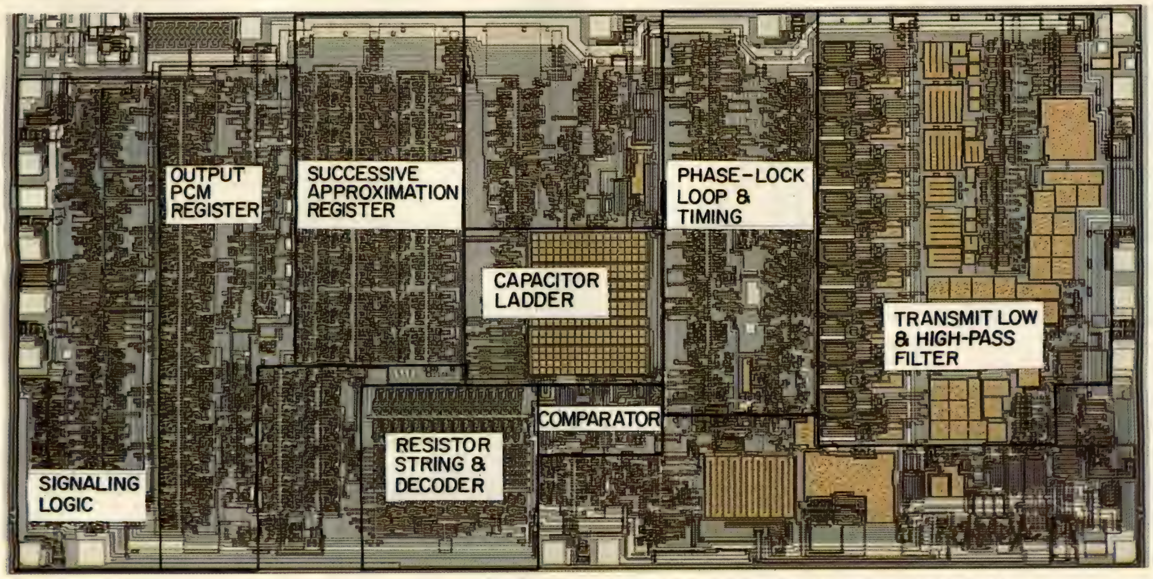
The fast pace of telecomm-IC introductions prompts Mostek's Dave Seeler to warn equipment designers about waiting with their designs, for "ultimate" chips. Instead, he advises prudent equipment designers to use the chips that are available now and meet the necessary requirements. Then, as newer chips become available, they can be fit into existing designs, to lower costs even further.

In the MK5912, Mostek (Carrollton, TX) proved that NMOS processing could produce a PCM filter that combined low power drain with small size and low noise. Using variations of its RAM process, Mostek fabricated precisely ratioed capacitors between a polysilicon layer and substrate, without resorting to overlapping poly layers (Fig. 4).

Even this advanced switched-capacitor processor is being further refined with an eye to yet lower cost. The newest chip is being sampled and is slated for quantity production late in the third quarter of this year.

The dense NMOS processing puts transmit and receive filters onto about 9000 mils^2 of silicon, about one-third the size of other IC filters for PCM. Mostek foresees that the same NMOS processing will scale down the codec to the point where a chip of economic size could accommodate both the codec and its associated filters. Under 30,000 mils^2 seems certain.

Mostek is so pleased with the technology used in the PCM filter that the company is investigating its use for other signal-processing applications, such as adaptive filtering and speech processing. Adaptive filtering is like bread and butter to telecomm equipment designers, being the basis of applications such


OUTPUT PCM REGISTER
SUCCESSIVE APPROXIMATION REGISTER
PHASE-LOCK LOOP & TIMING
CAPACITOR LADDER
TRANSMIT LOW & HIGH-PASS FILTER
COMPARATOR
RESISTOR STRING & DECODER
SIGNALING LOGIC

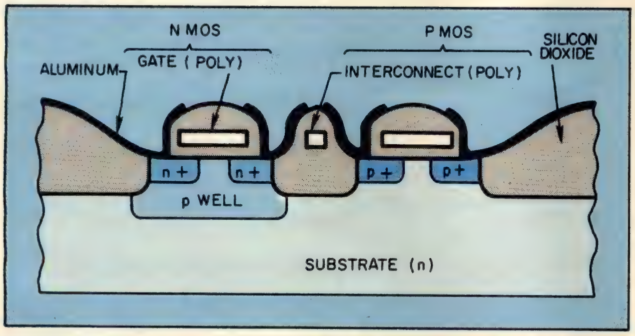
5. The architecture of AMI's 3501 transmitter-plus-filter CMOS chip.could probably be applied to make a one-chip codec-plus filter. All the elements for the one-chip IC come together in CMOS.

as line equalizers and echo cancellers.

The compatible NMOS technology of Intel's codec and filter make the 2910, 2912 set a prime candidate for a combination chip. Power drain and noise will probably show overall improvements when the single-chip version sees daylight.

Per-channel codecs split up to come together

American Microsystems (Santa Clara, CA) has already integrated its filters with the codec. But, for now, the CMOS implementation is a two-chip affair, with the codec and its filter on one chip and the decoder and its filter on another. Among a dozen or so per-channel IC codecs, only AMI and Fujitsu (MB 6001 coder plus filter, MB 6002 decoder plus filter) build separate transmit and receive sections. With filters and converters already integrated, this architecture seems certain to develop into one IC.

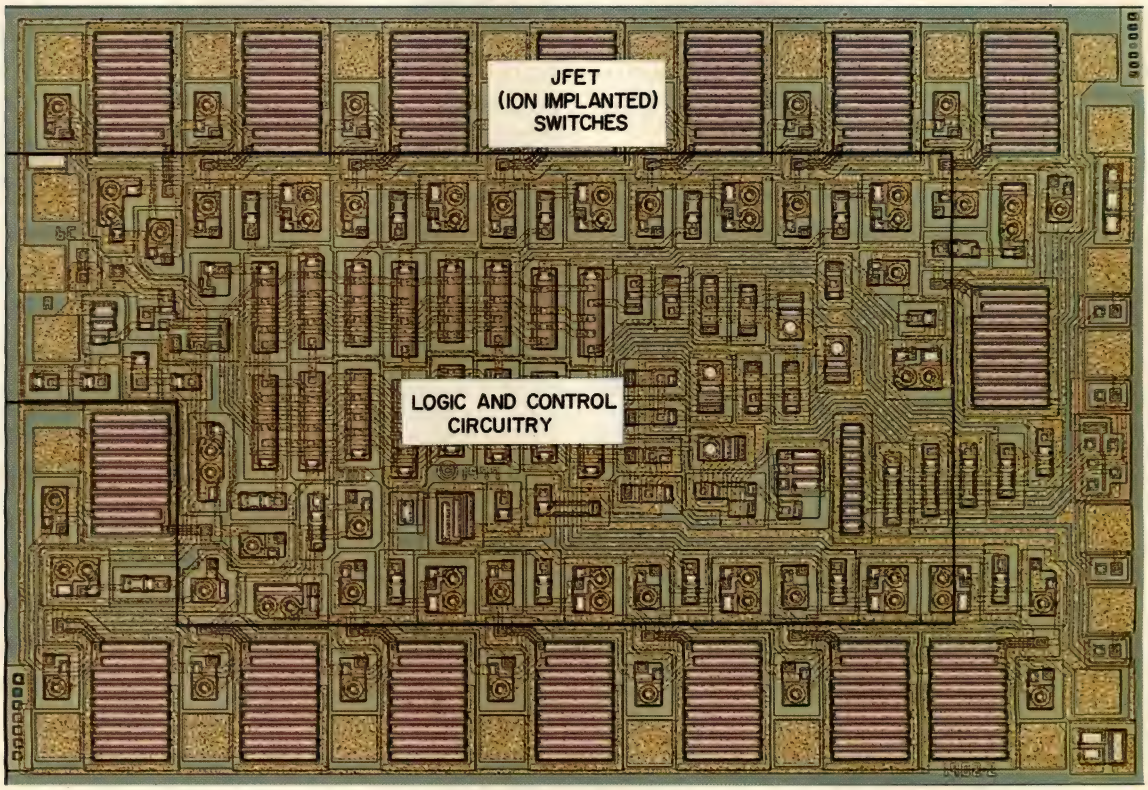


6. In contrast to standard CMOS, silicon dioxide isolates p and n-channel FETs in Mitel's Iso CMOS making fast, dense chips with 10-Mbit/s logic and DTMF filters compressed to 110 × 140 μm.

Telecomm ICs are certainly moving in the direction of increasing integration. Bill Nicholson, Communications Engineering Manager at AMI reflects that combining analog and digital functions on the same chip has been a watershed in telecomm ICs. Nicholson sees the design of telecomm ICs in large part to be a matter of apportioning to the analog and digital sections those functions that give the best relationship in performance, reliability, power consumption and cost.

A forceful demonstration of the mixing is in AMI's 3501 and 3502 codec set (Fig. 5). Though mainly analog functions are performed, the chip devotes two-thirds of its silicon to digital logic. Every telecomm chip being developed at AMI, but one, uses a mixture of analog and digital circuitry. Nicholson sees the trend towards systems on a chip, but he says that these telecomm chips will continue to mix both analog circuits and digital logic.

The trend at Siliconix is towards individually packaged coders, decoders and separate filters for each all in metal-gate CMOS. Slated for mid-year introduction, the filter family consists of three units: DF351 (transmit), 353 (receive) and the hybrid 352 (receive plus a bipolar output-amplifier chip). All



7. Ion-implanted JFET switches surround bipolar logic circuits in PMI's MUX 86, a 16-channel multiplexer particularly useful for shared-channel codec systems.

three filters operate from ±5-V supplies. The bipolar amplifier, in the 352, can deliver up to 16.5 dBm. No way exists to drive that power level into 600-Ω loads, from ±5-V supplies. However, the Siliconix bipolar output amp can run from ±15-V supplies and deliver the required output level into the single-ended transformers that are now in telco equipment.

In addition, because the new filters use continuous as opposed to switched-capacitor sections for anti-aliasing (transmit) and for smoothing (receive), they are expected to provide less ripple and noise and more bandwidth. Once the idle-channel noise problem is better contained, Kamp expects telecomm equipment manufacturers to get better crosstalk data. Some switched-capacitor IC filters are so noisy, says Kamp, that crosstalk signals are completely masked.

Iso CMOS processing gives Mitel the essential ingredients for a single chip that combines the circuitry for a codec and its associated filters. The Iso CMOS process is a polysilicon-gate CMOS technology (Fig. 6) that is related to the Iso Planar process developed some years back at Fairchild. Three major advantages of the Iso CMOS process are:

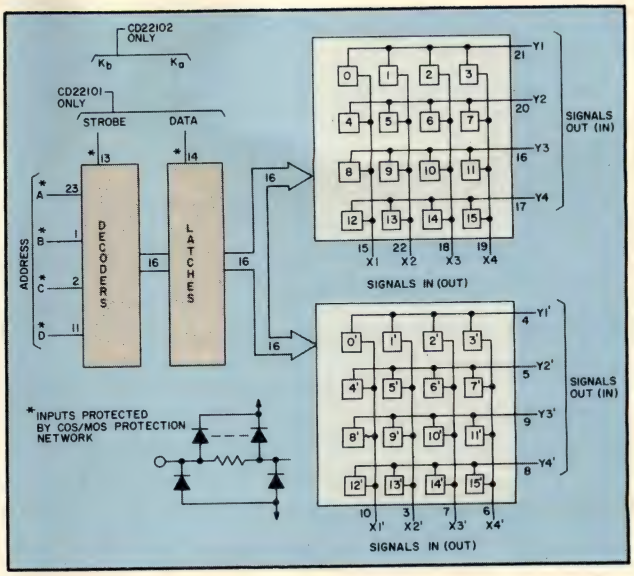
- Low power drain
- High-speed silicon-gate technology
- Density.

Low-power drain is a well-known feature of CMOS circuitry. This is especially true when the circuits are standing-by or under a low duty cycle. As the operating rate increases, CMOS logic tends to approach NMOS in power consumption.

Speed, in Iso CMOS circuits, is enhanced by isolation wells, created in the process, that eliminate much of the parasitic capacitance normally found between nodes. Pragmatically, Iso CMOS is as fast as SOS, though SOS is theoretically capable of higher speeds. In SOS, speed is aided by the insulating substrate. Parasitic capacitances simply cannot be formed to an insulator. However, very few SOS circuits actually operate at speeds greater than the 10-Mbits/s of Iso CMOS.

Iso CMOS can pack circuits even more densely than NMOS, using the same 5-μm geometry. Currently, Mitel manufactures some custom Iso CMOS chips with 2 to 3-μm design rules. Next year the company will use the finer lines in standard devices.

A recent $20-million grant from the Canadian government will start Mitel on a VLSI program. The resulting Iso CMOs technology should increase packing density by about four times. At that level of integration, VLSI telecomm products would stand in danger of being overpowered, were it not for the inherently low power drain of CMOS.



8. On-chip diode and resistor networks protect high-input impedance CMOS circuitry from the damage of static charges. RCA's CD22101 and 22102 are 4 × 4 × 2 crosspoint switches with built-in control memory.

Iso CMOS processing should result in an all-in-one IC early next year. The codec-plus-filter chip will be one of the advanced ICs to be used in Mitel's forthcoming digital central-office switch, the SX 2000.

As an offshoot of the combined codec/filter chip, Mitel also plans to introduce an Iso CMOS chip that contains the filters only. Noise and power improvements over other switched-capacitor filters are anticipated when the chip is introduced towards the end of this year.

In both the all-in-one and the filter-only chips, Mitel is developing special low-noise op amps. Usually, lower noise in op amps follows from larger geometries.

Although all of Mitel's new telecomm ICs are slated for Iso CMOS processing, many of the company's mature devices are made by the older metal-gate CMOS process. Metal-gate CMOS is the byword at Motorola for codec and filter chips because of the low power drain and produceability of the process.

The first generation two-chip codec and filter set (MC14404,6,7 codecs and MC14414 filter) draws 110 mW in operation and less than 1 mW in the power-down mode. This translates to approximately 5-mW average in typical central-office use. Motorola's codec, filter and time-slot assigner (MC14416,8) chips operate from a single 12-V power supply. All the chips can operate with continuously variable clock frequencies from 0 to 3.088 Mbits/s. Hence, this codec family can be used in equipment other than PCM switches. The single-supply operation results directly from the internal self-biasing capability of the CMOS circuitry.

Because the 14414 filter does not include the high-pass section required in switching applications, the chip is useful as an analog filter for channel-banks. The break frequency is programmable by changing the clock frequency, because there is no high-pass filtering to interfere.

For PCM filtering, Motorola now offers the MC 14413 that adds a high-pass section to the two low-pass sections of the 14414. The response of this chip does not program well with the clock as a result of interaction with the high-pass section.

JFET encourages multiplexer performance

From PMI come ICs for shared-channel codecs. Shared-channel systems place stringent requirements on the analog multiplexer. These units must deliver low on-resistence, low crosstalk levels, and constant channel resistance in the face of analog voltage changes. Also, shared-channel MUXs must inject only minimum charge in both the MUX and DEMUX modes. PMI merges ion-implanted JFETs with bipolar circuitry to achieve high-performance in such members of its codec MUX family as the MUX86 (Fig. 7).

Communication systems based in digital signal processing will require accurate, high-speed linear a/d and d/a converters. Resolutions of 12 to 16 bits will have to be guaranteed, along with corresponding monotonicity and differential nonlinearity. Engineers at PMI look to high-stability thin-film resistor and ratioed bipolar structures to meet the demands of these circuits.

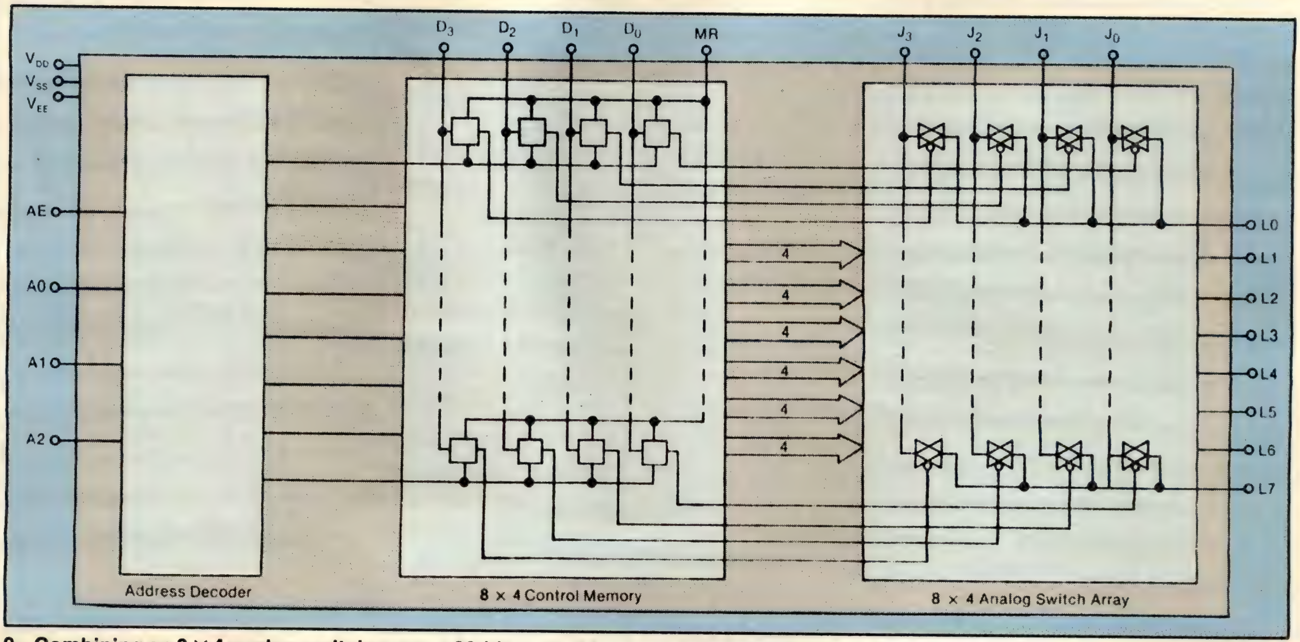
Currently, PMI uses its high-speed bipolar processing in its RPT-81 PCM repeater chip. The gain bandwidth product required in this chip is so high that PMI had to develop a new process that stretched the previous speed limit. The preamplifier gain bandwidth product exceeds 45 MHz and the line-driver rise time is lower than 30 ns.

Bipolar processing is also popular for another type PCM repeater IC. RCA (Somerville, NJ) builds its TA10261 chip in pure bipolar technology. Though externally the chip seems to be a simple amplifier, internally it must extract the signal from noise, resynchronize the clock, provide 30-ns transitions and 100-ns pulse widths and furnish front-to-back isolation. The chip should operate for at least 20 years. Today, RCA engineers could probably cast the chip in CMOS.

Bipolar circuits solve the problems associated with PCM repeater chips for Exar Integrated Systems (Sunnyvale, CA). The bipolar circuits must process 100-mV inputs into clean, high-speed output pulses across a 660-Ω load. In addition, PCM repeater chips provide automatic line build-out capability (ALBO) —a type of AGC that automatically attenuates and shapes signals to adjust for variations in cable characteristics. Controlled by feedback as in AGC, the preamp output passes between two peak levels.

Alan Grebene, Vice President of Exar, considers MOS circuitry to be a good choice for high-density functions. However, a PCM repeater, he notes, is more of a precision circuit. Thus, even with uncrowded bipolar processing, the XR-C262 is a modest sized chip—well below 10,000 mils^2.

Bipolar-compatible I^2L processing will put dense digital signal-processing circuitry on Exar's new PSK encoder IC. The I^2L digital section of the chip



9. Combining an 8 × 4 analog-switch array, a 32-bit control memory and digital address decoding on the same chip, Mitel's 8804A crosspoint switch provides high front-to-back resistance ratios, low power consumption and digital logic. The switch is fabricated with metal-gate CMOS.

will accommodate counters, decoders and ROM, while the bipolar analog section will provide the linear waveshaping circuits for amplitude modulation and squarewave conversion. The PSK IC is scheduled for introduction this fall.

Metal-gate CMOS is the process used to build crosspoint arrays by three major producers of analog switching ICs, Motorola, RCA and Mitel. Motorola's 145100 and 142100 are 4 × 4 × 1 devices. RCA's 22100 is a 4 × 4 × 1; its 22101 adds a second layer to become 4 × 4 × 2 (Fig. 8). Mitel's MT 8804, an 8 × 4 × 1 array, keeps addresses in its memory (Fig. 9). CMOS circuitry gives all these chips stable on-resistances of less than 100 Ω and off-resistances of more than 10 MΩ.

Special specifications and quirks abound in the telecomm systems of different nations. Each nation, for example, uses different duty cycle pulses in dialing. Recognizing this problem, TI has made its ICs mask-programmable. TI's Glen Haas advises telecomm equipment engineers who want to design internationally viable products to look for programmability of hardware functions at the IC-mask level and to use the software programmability of μPs at the system level.

Architectures, rather than processing technology, set apart the chips that manage data-comm protocols. Chips handle functions that were formerly performed by CPU software or first-generation IC hardware. Some chips cover limited ground deeply; others combine such disparate functions as:

- Asynchronous transmission
- Synchronous transmission
- Bit-oriented processing
- Character-controller processing
- Error checking and control
- Communications over global facilities, local nets or simple point-to-point links.

Almost all dedicated data-comm chips are produced in metal-gate MOS technology. These chips are not yet candidates for leading-edge processing techniques because the logic is too random; half of the chip area is taken up by interconnections. Processing that would lead to smaller, more densely packed devices simply would not have much of an effect.

Microprocessor and memory chips are a different story. LSI memories, and even μPs, are built up from very well-defined blocks that fit together tightly. According to Brian Cayton, Applications Manager at Standard Microsystems of Hauppauge, NY, shaving even half a μm from the design rules in a memory or a μP can lead to dramatic improvement. In the more random data-comm chips, the change would go almost unnoticed.

Data-comm chips replace CPU software with hardware, completing the cycle started when software replaced the costly hardware of earlier days. One example of former software functions implemented in LSI is SMC's COM8004. Software offered a good alternative when the functions handled by the 8004 required 40 to 50 TTL packages. The LSI chip adds 32-bit CRC capability to standard, synchronous protocol-control ICs, like SMC's COM5025. Could a CPU take on this task? Very easily, answers Cayton; but, in today's demanding, high-speed, synchronous systems, processors often have all they can do to keep apace of their principal number-crunching and file-managing tasks. Chips that unload the burden of overseeing data-comm functions are more than welcome to system designers.

The COM8004 performs a 32-bit CRC on serial input data and delivers serial output. Other types of CRC hardware, such as the 2653 from Signetics (Sunnyvale, CA), check only 16-bit blocks. With larger block length and faster data rates, catching data-transmission errors becomes critical. The new chip will detect all but one error in several million bits, while the standard 16-bit check misses an average of one error in 65 kbits.

Hardware to software and back again

Concurring with the view that protocol-control chips tend to replace designs formerly executed in SSI/MIS hardware or firmware, Alex Goldberger, Data-comm Applications Manager at Signetics, adds another vector: on-chip intelligence. In bit-oriented protocols, control information occurs at preset positions. But in the Bisync protocol, for example, special characters must be recognised and stripped from or added to the block. Each character-controlled protocol has its own distinct characters. Thus, handling data transmission under synchronous protocols requires intelligence in the controllers. The more types of synchronous protocols a chip handles, the more intelligence it needs. Also if the chip is to be more than cosmetic, it must handle protocols in depth. That implies even more processing power on the chip itself.

Experts from coast to coast agree that developing useful synchronous protocol control chips costs about $250,000. This high initial cost usually makes single-application chips impractical. Hence, designers can expect that future data-comm chips will handle many protocols. An acceptable means for selecting the active protocol, from a chip capable of controlling many protocols, is via control signals from the CPU. This method adds very little to the load of the processor.

Going with the multifunction trend, Signetics is developing a chip for controlling synchronous data transmission that will process the various synchronous protocols now being handled by the 2661 and 2652. The new LSI will provide up to 16-bit CRC checking, like the 2653, and will automatically ask for a retransmission on error. According to Goldberger, the chip should handle most popular synchronous protocols with a minimum load on the CPU. The operating protocol will be selectable by the CPU via control signals and control words that the CPU transfers into waiting registers on the control chip. The chip will also contain intermittent-transmission FIFO registers.

Even in protocols thought to be standard, users still make changes to suit their systems. Hence, protocol-control chips must anticipate programming variations. Another stimulus for flexibility in data-comm ICs is that processors must often communicate with network equipment that uses a variation of the standard protocol or one that is completely different. A chip can accommodate only so much logic. So, Don Phillips, Peripheral Components Manager at Intel (Santa Clara, CA) observes that chip designers trade-off the number of protocols accommodated against the depth of the handling.

Two channels equal one compact data-comm chip

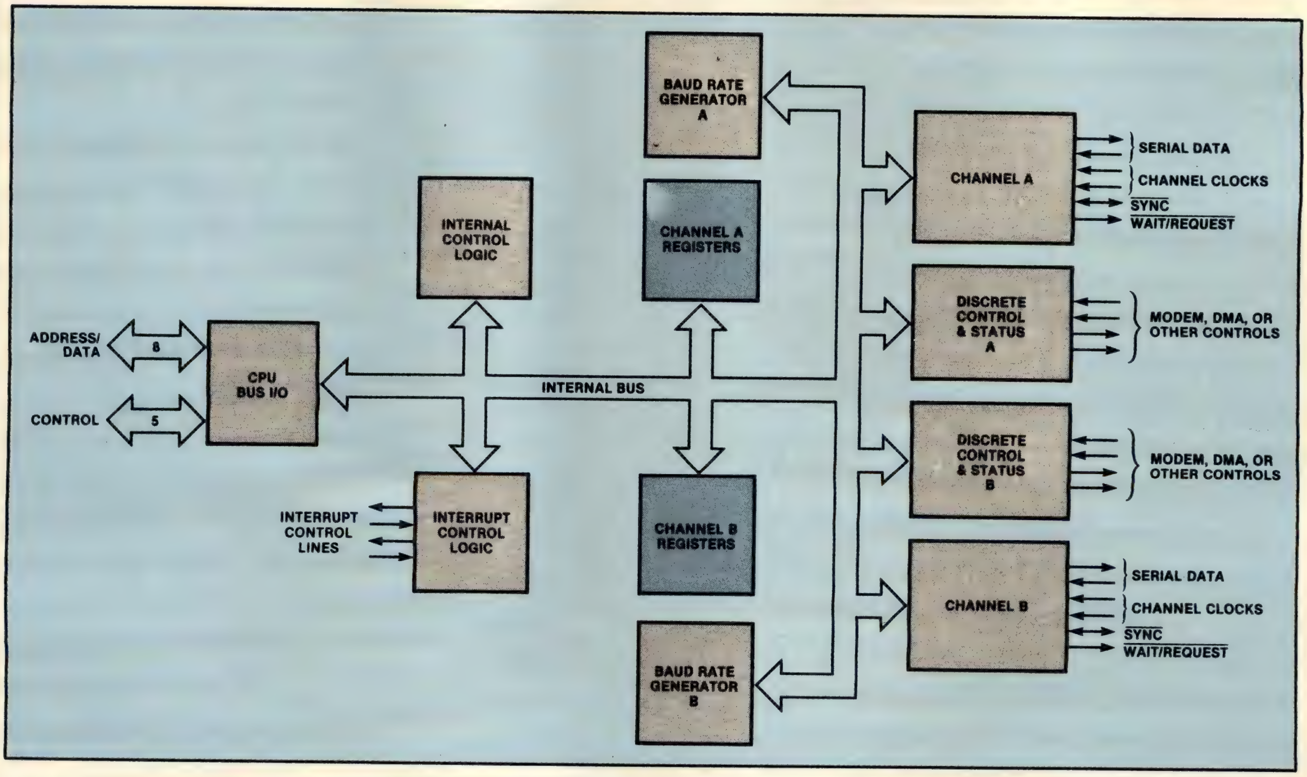
One of the most versatile of the data-comm chips is Zilog's (Cupertino, CA) SIO (second-sourced by Mostek). The layout of this chip is unique—two separate channels are on the same die. With computer aid, Ross Freeman, the SIO's designer, divided the chip into two independent memory-like arrays. Then the computer generated the second channel in a mirror image of the first. One of the densest of all nonmicroprogrammed, random-logic data comm chips, the SIO die is less than 200-mils on a side.

The density translates into capability. The chip contains all the input prioritization for both channels plus several popular lengths of CRC. Hence, the SIO can operate without a companion interrupt-controller chip.

The two-channel chip also provides vectoring to identify the memory location at which an interrupt-service routine begins. This feature works only with processors having vector capability, like the Z80. For example, if Channel B detects a parity error, it issues an interrupt to the CPU. The CPU then returns an acknowledgement of the interrupt request. Next, the SIO sends a uniquely coded 8-bit value for the B-channel priority. This value directs the CPU to the service routine.

Software in the SIO allows the chip to be polled by processors that have no vector capability. About 30% of the SIOs made to date work with processors that have no vector capability, according to Ken McKenzie, Marketing Manager of Ziolog's Components division.

The two-channel architecture of the SIO, with both



10. Popular synchronous and asynchronous protocols mate to the 16-bit architecture of Ziolog's Z-bus in the company's SCC. The two channels of the SCC are separately configurable under control of software-based commands from the central processor.

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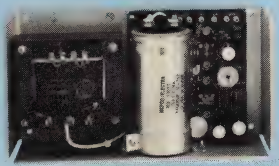
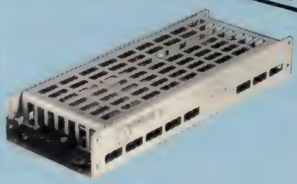
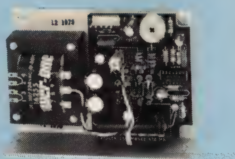
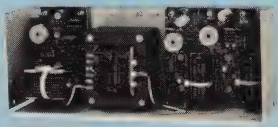
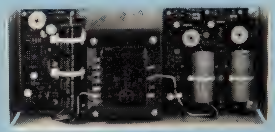
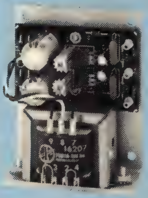
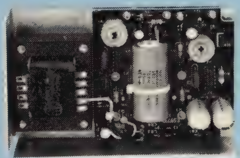
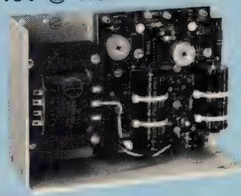
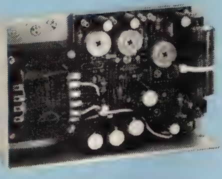
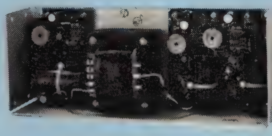
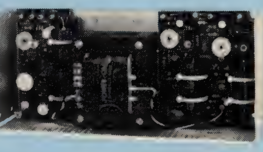
SINGLE OUTPUT & LOGIC POWER SUPPLIES • 56 "off the shelf" models • 2V to 250V, 0.1A to 40A • ±.05% regulation • 115/230 VAC input	**5V @ 3A, w/OVP** HB5-3/OVP $24.95 single qty.	**5V @ 12A, w/OVP**  HD5-12/OVP $79.95 single qty.	**5V @ 40A, w/OVP** **NEW**  SK5-40/OVP Switching Model $250.00 single qty.
FLOPPY-DISK SERIES • 8 "off the shelf" models • Powers most popular drives • Single/dual drive applications • 2-year warranty	**5V @ 0.7A, w/OVP** **12V @ 1.1A/1.7A PK** **NEW**  CP340 For one 5.25" Media Drive $44.95 single qty.	**5V @ 1A, w/OVP** **−5V @ 0.5A, w/OVP** **24V @ 1.5A/1.7A PK**  CP205 For one 8.0" Media Drive $69.95 single qty.	**5V @ 2.5A, w/OVP** **−5V @ 0.5A, w/OVP** **24V @ 3A/3.4A PK**  CP206 For two 8.0" Media Drives $91.95 single qty.
DUAL OUTPUT MODELS • 15 "off the shelf" models • ±5V to ±24V, 0.25A to 6A • I.C. regulated • Full rated to +50°C	**12V/15V @ 0.25A** **NEW**  HAD12-.25/HAD15-.25 $32.95 single qty.	**5V @ 2A, w/OVP** **9−15V @ 0.5A**  HAA512 $44.95 single qty.	**±12V @ 1.7A or** **±15V @ 1.5A**  HBB15-1.5 $49.95 single qty.
TRIPLE OUTPUT MODELS • 10 "off the shelf" models • 5V plus ± 9V to ± 15V outputs • Models from 16W to 150W • Industry standard size	**5V @ 2A, w/OVP** **± 9V to ± 15V @ 0.4A**  HTAA-16W $49.95 single qty.	**5V @ 3A, w/OVP** **±12V @ 1A or** **±15V @ 0.8A**  HBAA-40W $69.95 single qty.	**5V @ 6A, w/OVP** **±12V @ 1.7A or** **±15V @ 1.5A**  HCBB-75W $91.95 single qty.

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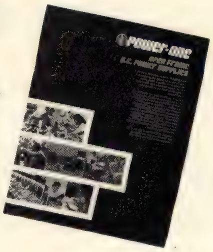

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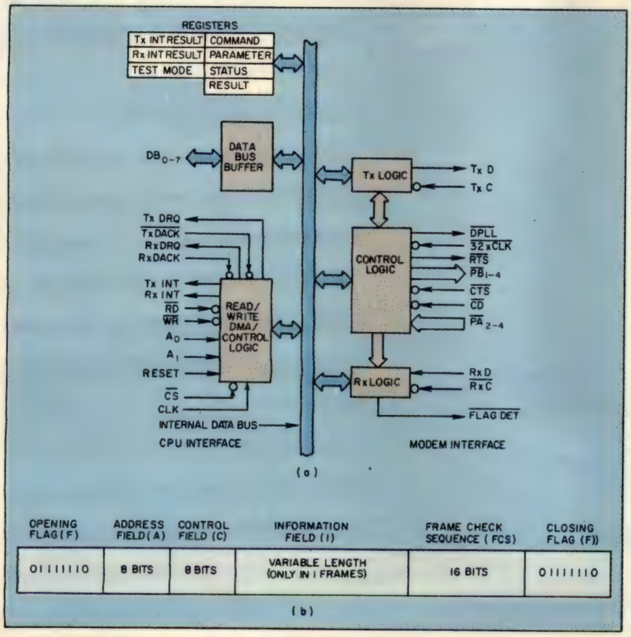
channels logically independent, can provide useful parts in spite of flaws in a die. When a fault stops one channel from working properly, the other channel is unaffected. Zilog packages single-channel fallout chips in the same 40-pin DIP as the full-capability unit. A designer can then build up data-comm equipment using only the one working channel, at a lower cost. In the future, if a second channel is required, the DIP can be replaced with a two-channel unit. The single-channel and dual-channel chips are software compatible.

Zilog offers another fallout chip, a two-channel DART, having only the asynchronous capability of the SIO. It sells for about $10.

For the Z8000 processor, the fourth quarter of this year should see an upgraded version of the SIO. Denser processing will add functions to, and raise the speed of, this Serial Communications Controller (Fig. 10) while the chip remains essentially the same size as the predecessor SIO. The two independent channels for synchronous and asynchronous operation will gain: on-chip, user-programmable, baud-rate generation; separate phase-locked loops to derive the clock directly from the data signal; and NRZI plus FM encoding/decoding capability.

Data comm for the long haul

Viewing data-comm chips from the application perspective, Intel's Phillips divides the uses into global telecommunications, local networks and point-to-point, low-speed systems.



11. HDLC/SDLC controllers must recognize and process three types of frames: information, for data transfer; supervisory, for control; and nonsequenced, for initialization and secondary-station control. The information that aids frame processing in Intel's 8273 (a) is stored in appropriate registers. All frames conform to the format shown (b).

Global systems interconnect remote locations through modems over long lines, with data rates fairly standardized at 65-kbits/s. Controllers for global transmission must go deeply into Level-2 of the protocol to replace the intricate and lengthy software that controls messages and their routing, or flow. Intel's 8273 (Fig. 11) reduces intervention from the CPU by focusing on bit-oriented synchronous data transmission under the related SDLC and HDLC protocols. Though the chip does not handle all HDLC and SDLC Level-2 functions, it goes far beyond Level 1 by including such features as: framing, address recognition, zero-bit insertion and high-level commands. Thus, data-comm channel control becomes transparent to CPUs at the frame level.

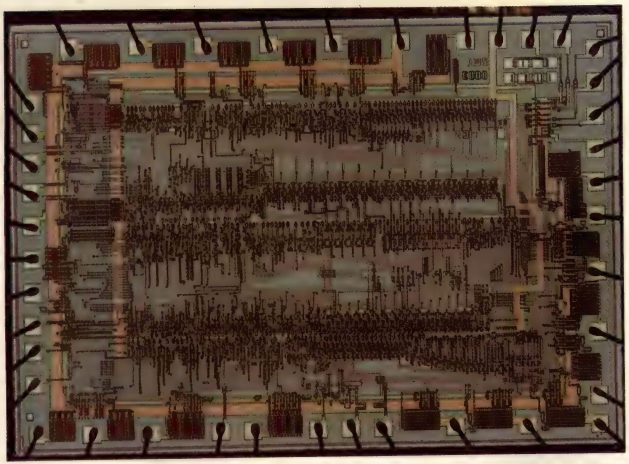
However, the 8273 neither sequences nor retransmits missing frames. Within its intended protocols, the chip does accept and execute commands from the CPU and can be configured into modes as the CPU requires. Other HDLC/SDLC control ICs (like SMC's 5025 and Signetics' 2652) operate similarly.

Probably the most extensive control of Level 2 is planned for the proposed LSI controller for packet-switched communications under the CCITT X.25 protocol, the 2511 from Western Digital (Newport Beach, CA). The ambitious packet-switching controller is slated for introduction in 1981.

One problem IC designers face in trying to commit protocols to silicon is that the so-called standards are often ambiguous. Systems designers come up with different interpretations of the same protocol. In the field, several implementations of one standard grow up simultaneously, says Phillips.

Rather than rely on only the published standards, which are often years in coming, many semiconductor manufacturers encourage their designers to participate in establishing the standards. Charles Von Urff, Telecommunications Division Vice President and General Manager at Western Digital, told attendees at the data-comm LSI session at Interface 80, that his company sends five people to the ANSI committees to learn the functions equipment manufacturers need from LSIs. Indeed, the LSI makers often move so incisively that the standards are usurped by *de facto* hardware.

Local networks connect what Intel calls "Development Systems" to shared resources, such as files and line printers. In the rapidly developing field of word processing networks, ten or so terminals often share one printer and the mass storage of hard disks. Such local data-comm networks are best accessed via protocol-control chips that offer both high-speed synchronous and low-speed asynchronous capability, says Phillips. Equipment working into local networks



12. Design rules in SMC's SMART chip need no compression at all. Much of the silicon area is either unused or taken up by interconnects to handle the 20-bit, Manchester-coded words of the MIL-STD-1553 protocol.

can use chips, like the 2651, 2661, SIO, 8251 and 1671, that handle many protocols.

Old UARTs never die

Asynchronous transmission, though the least efficient in terms of channel-capacity use, is still surprisingly popular in point-to-point datacomm. In particular, CRT terminals are still being designed for connection to mainframes over asynchronous lines. Here, Phillips, McKenzie and Cayton agree in their surprise over the continuing popularity of asynchronous transmission, even though synchronous control chips promise more efficient line use. Perhaps equipment designers are impressed with the low cost of UARTs and reluctant to try their hands at data-comm engineering. Cayton sees equipment engineers asking for ever faster asynchronous parts; although some of the new transmission schemes like X.25 and T1 demand separate synchronous clock and data signals.

The protocol for military avionic data-comm equipment differs markedly from most others in use today. Data are transmitted synchronously in 20-bit Manchester-coded words under the MIL-STD-1553 protocol. SMC offers its SMART chip, dedicated to this protocol (Fig. 12). Unlike most R/T chips, this IC's acronym does not start with the letter U, because the device is not universal.

In response to the continuing strength of asynchronous transmission, SMC will offer four updated UARTs. Two will be 5-V versions of older parts, and two will offer increased distortion margin. Distortion margin is the ability of an asynchronous system to extract errorless data in the presence of jitter and noise from the separate clocks of the transmitter and receiver. Two methods for increasing distortion margin are faster clocking and sampling with both leading and trailing edges of the signal.

Certainly much more needs to be done to bring the power of LSI to data-comm equipment. Al Weissberger, who used to design data-comm ICs and now designs systems as Principal Engineer in the Advanced Engineering Department at Memorex (Cupertino, CA) has proposed that LSI designers turn away from general-purpose programmable chips and direct their attention to such pressing data-comm needs as:

- Intelligent receiver/transmitters
- Link and terminal protocol converters
- Level-1 protocol converters
- First-in, first-out (FIFO) chips
- Multiport RAM controllers
- Low-cost modems.

Receiver/transmitter chips could offload CPUs by including I/O driver firmware, normally left to the processor. Weissberger says that enough room is available for two 16-bit counters, for receive and transmit; either a DMA or FIFO, shared-memory interface; modem controls; and logic for arbitrating among shared resources. Some functions could be made completely automatic (requiring no CPU intervention), such as character assembly and disassembly line formatting and error control. Weissberger would like even more: automatic baud-rate detection, data compression and encryption, for example.

A link and terminal protocol converter could perform one-to-one link-level conversions on transmission format, line framing, code set, data rate and polling selection. The chip should have room for the logic to form character blocks, check errors and control the flow. By programming the metal masks, designers could implement almost any set of conversions.

Level-1 protocol converter chips could lead equipment designers out of the "RS-232C or RS-449" quagmire (see ELECTRONIC DESIGN, April 26, 1980, p. 46). Another conversion between physical interfaces that Weissberger considers useful would be RS-232C to X.21/X.24, the CCITT's recommended standard for X.25 packet networks and X.21 circuit-switched networks.

A FIFO buffer-memory chip would smooth data flow between devices operating at different speeds. The first IC steps have already been taken in FIFOs. However, Weissberger wants higher capacity chips that accommodate 64 and 128 bytes.

Multiport RAM controllers could arbitrate the access of multiple μPs to a shared RAM. Low-cost modems could take advantage of processing to place high-performance analog and digital circuitry on the same chip.□

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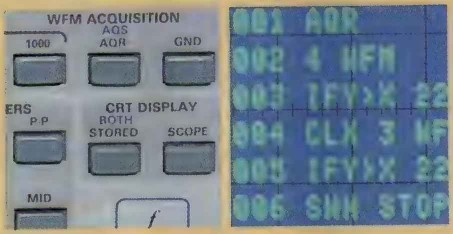

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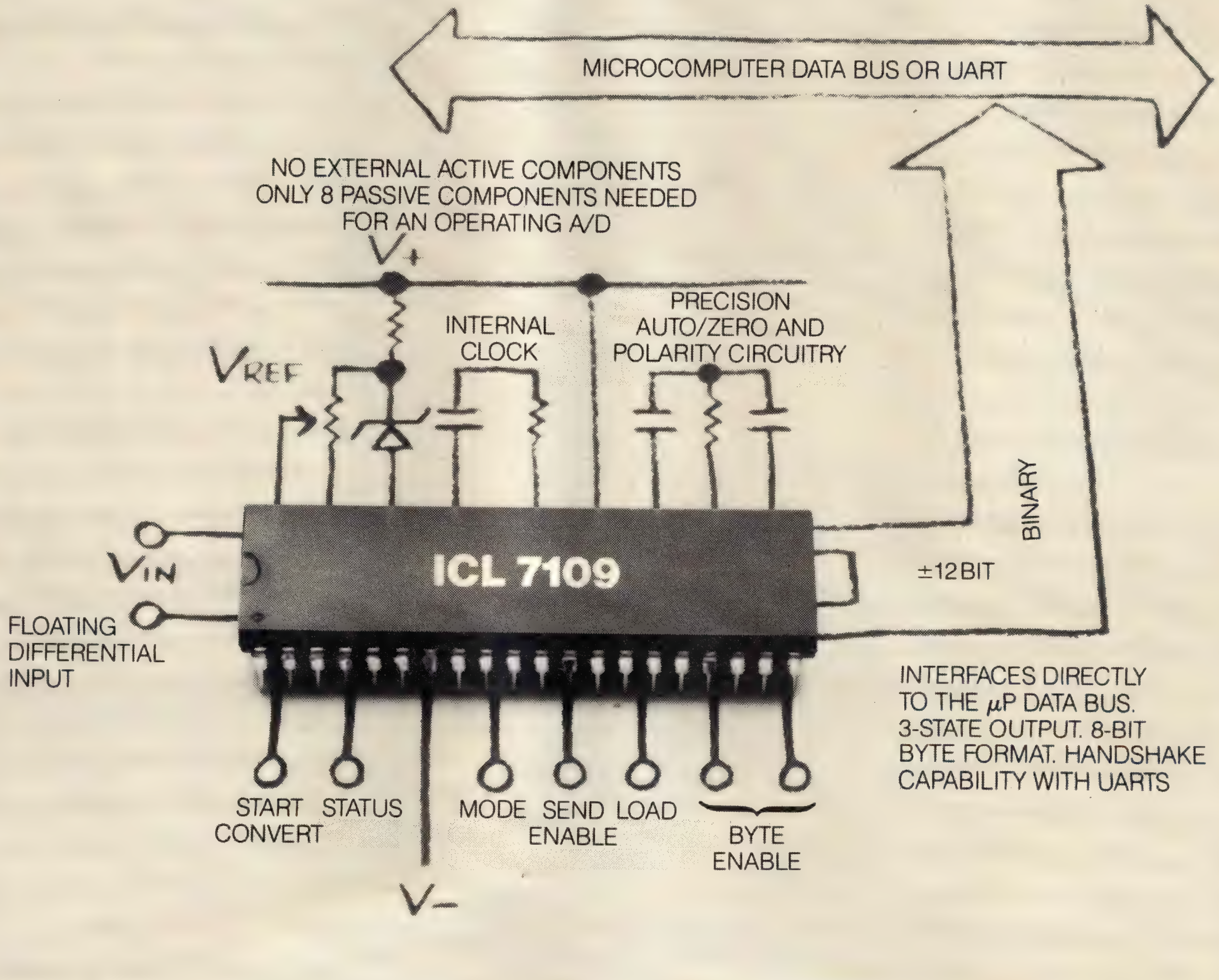
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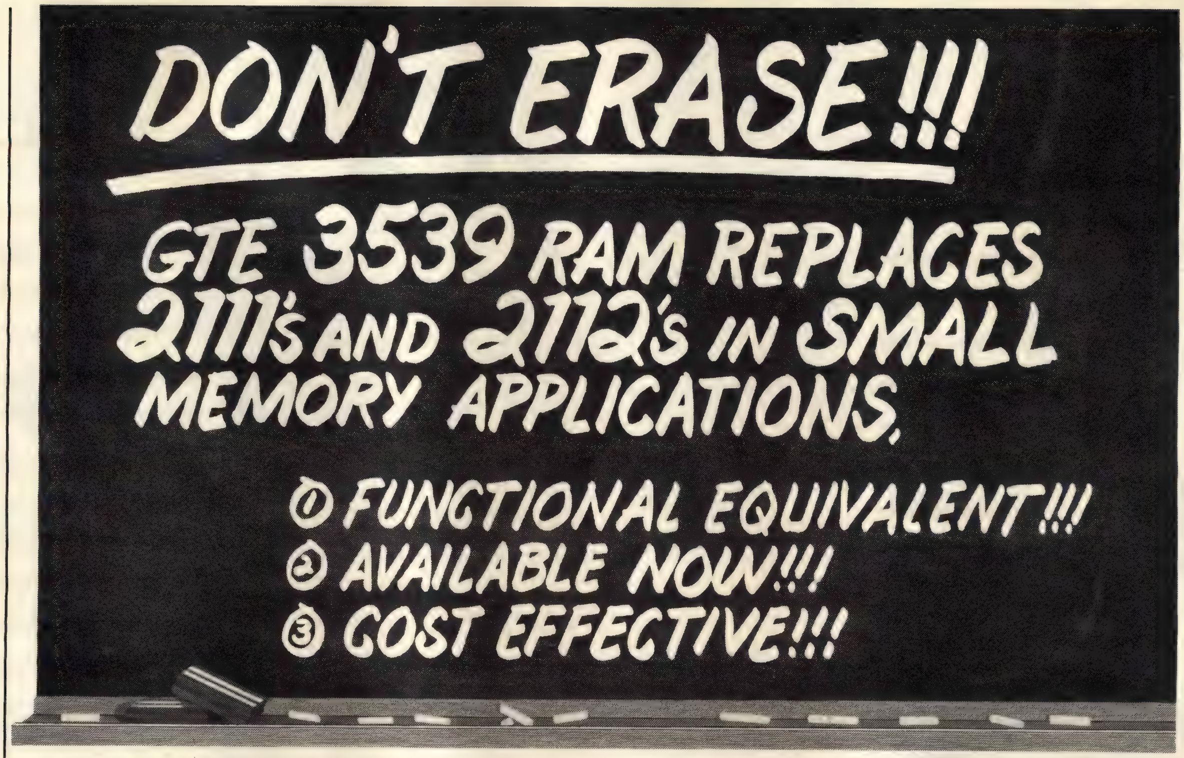
CIRCLE NO. 41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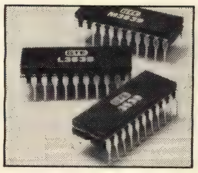

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CIRCLE NO. 42

With power-handling capability and breakdown voltages on the rise, in both bipolar and MOS transistors, competition between the two technologies is heating up. Designers can choose from the best of both.

MOS power vs bipolar—the designer wins

After a period of relative calm on the power-transistor front, developments over the past few months herald innovative devices on—or just over—the horizon. These new devices result from intensive efforts by manufacturers to improve their processing and packaging techniques while cutting production costs.

Some of the upcoming products depend upon better processing methods—as power MOS transistors illustrate—but bipolar makers are dusting off old ideas to develop new devices:

- The use of a proven technique—the cascode switch—to produce an experimental device, the cascode-switch bipolar transistor
- The use of the planar technique, rather than the traditional mesa technique, to develop a new class of high-breakdown voltage bipolar devices
- The appearance of new power packages, but none yet ready to dislodge the old reliables —TO220AB and TO-3
- The application and modification of vertical DMOS technology to extend the breakdown voltages of power MOS devices.

Feeling the hot breath of MOS manufacturers uncomfortably on their necks, bipolar makers have sought more performance out of proven and stable technologies, as demonstrated by the innovative cascode switch from General Semiconductor Industries (Tempe, AZ). The four-terminal hybrid transistor can switch a 20-A inductive load at nanosecond speeds, and snubbers are not needed. Before this, bipolars were not fast enough for switching regulator power supply applications at 100 kHz and above.

Gene Heftman, Field Editor

The device, having an area of 250 × 250 mil^2, is composed of two transistors and a zener diode. The output transistor is a modified bipolar designed for high-speed square-wave switching. Its driver is a very low-voltage (BV_{CEO} of 15 to 20 V), high-current,

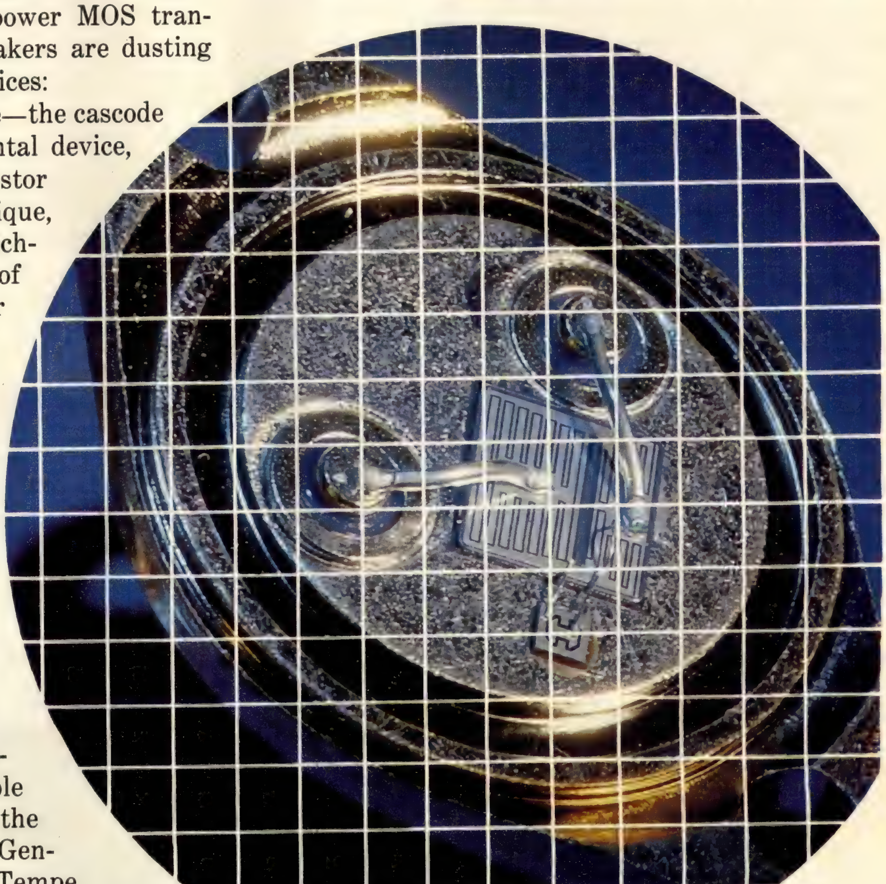


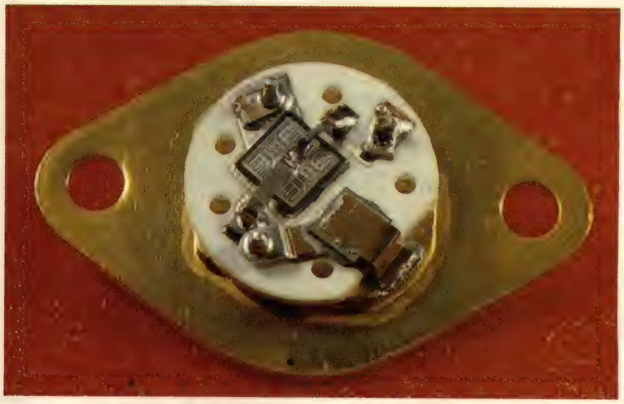
Photo courtesy of Motorola

high-speed switch that is much smaller than the output transistor. To make the output transistor operate reliably at turn off, both the driver and the output must be tightly coupled in the same package. The first units will be housed in the familiar TO-3 package (Fig. 10).

While formal announcement is still a few months off, the turnaround time from development to production for the experimental device could be short, since the primary semiconductor devices of the cascode switch take advantage of standard bipolar processes and mask tolerances.

The trend toward multiple devices housed in a single package is well underway at Unitrode (Lexington, MA), which puts its switching-regulator output circuits in TO-3 and TO-66 cans. Sitting inside the PIC800 series of hybrid power ICs are a power transistor and a matching commutating diode (Fig. 1). Both devices are mounted on a beryllium-oxide substrate which provides both good thermal conductivity and electrical isolation of the components from the case. In addition, the substrate gives a low capacitance between substrate and case, reducing the effects of RFI. Passivation is accomplished with a layer of soft glass followed by one of hard glass, but this is not yet the ideal solution. Even in the mature world of bipolar transistors, much work remains in the passivation area.

Attesting to the limitations of current passivation materials, Arnold Applebaum, President of Solid State Devices (La Mirada, CA), notes that soft glass often fails to provide a good hermetic seal, although it fires at lower temperatures than hard glass. While hard glass does seal better, it is brittle and cracks easily. Thus, all passivation with glass—sometimes called glassivation—is marginal.



1. The essential elements of a switching-regulator power supply reside under one roof, in this Unitrode power-output hybrid circuit. With matched transistors and diodes, the devices not only handle high power (30 A, 40 V) but also simplify power-supply design.

Manufacturers are experimenting with nitrides and certain silicon compounds to solve the problem. Particularly in plastic packages, semiconductor devices that are not passivated can pick up package contaminents and exhibit drift over time and temperature. Moreover, glass coverings lead to a cleaner manufacturing process, eliminate extra etching steps and generally provide a more reliable device.

One type of transistor that must use glassivation to reduce leakage currents and ensure stable high-temperature operation is the horizontal-deflection transistor. For high-voltage TV circuits, Motorola's (Phoenix, AZ) MJ12004 and 12005 devices withstand collector-to-emitter voltages up to 1500 V. Both Motorola devices are high power types; the MJ12004

2. With a growing ability to handle large wafers, bipolar manufacturers hold a significant lead over MOS-makers in high-power applications. The new Motorola Darlington carries 40-A continuous and has a 400-V sustaining voltage.

handles 5 A and the 12005 handles 8 A, with power dissipation that reaches 100 W.

In applications that require transistors to handle more than 15 A at voltage levels exceeding 400 V, the bipolar device still holds a commanding lead over the MOSFET. Because heat can easily destroy a transistor at these high-power levels, devices must be ruggedly constructed.

High power—bipolar territory

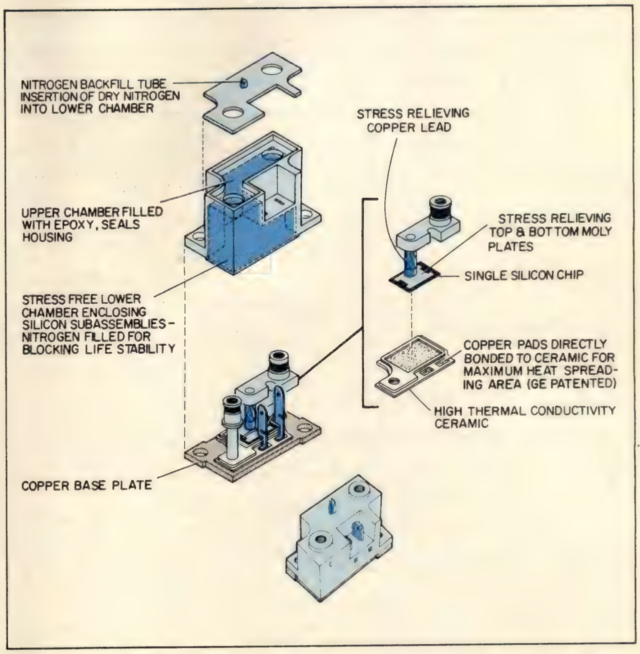
To handle the load, most companies do not rely on solder techniques to attach the semiconductor chip to the header. Instead, the die is metallurgically bonded to a molybdenum pedestal, providing much greater resistance to thermal fatigue. With this mounting technique, TRW Power Semiconductor's (Lawndale, CA) SVT7573 family of switching transistors can handle currents of 20 A continuous, withstand voltages of 600 V and switch in hundreds of nanoseconds.

Another way of preventing thermal failure, used by Unitrode in its UMT1006 through 1012 family of power transistors, is barrier processing. Although it requires an extra diffusion step, the process prevents current from going to the center of the junction when the transistor turns on. Current is easier to get out when the device turns off, so switch-off times improve. There is less current crowding, current density decreases, and the device exhibits better second-breakdown capability.

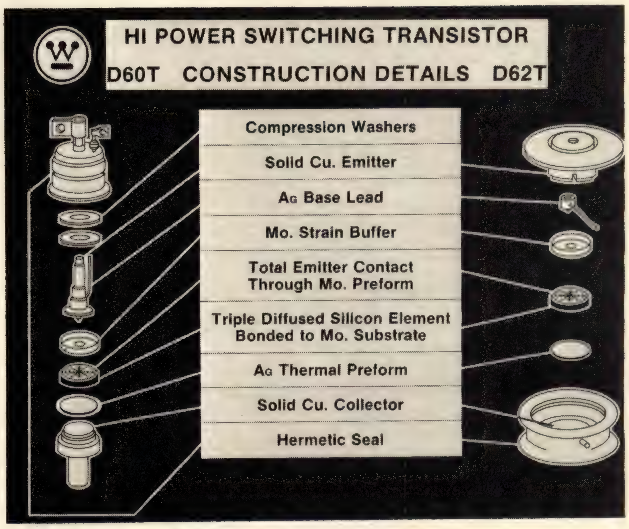
For higher breakdown voltages in bipolar devices, Texas Instruments (Dallas, TX) uses the well-understood and highly reliable planar technique, instead of the traditional mesa technique, to manufacture a line of high-voltage devices. Previously, planar processing was considered too costly, and the structures too complex. As recently announced, the TIP701 transistors boast collector-to-base breakdown specifications ranging from 800 to 950 V. Beveled-mesa devices, meanwhile, are pushing into the 1500-V breakdown region.

Darlington's fill the bill in circuits that draw large currents and must provide more gain than a single transistor can deliver. Many Darlingtons, such as RCA's (Somerville, NJ) 2N6284 and 6287 20-A units, are simply monolithic circuits that function as a single high-gain power transistor. Typically, an RCA device contains two resistors and a diode, in addition to the power transistors.

One key to the construction of more powerful Darlingtons is wafer fabrication. Wafer sizes have moved up over the last few years—4 and 5-in. slices are common now—but the cost of the process could be improved. Semimakers want to build high-power parts, but build them economically. The benefits from improved wafer fabrication are demonstrated by Motorola's MJ10022 and 23 Switchmode Darlingtons (Fig. 2). The devices handle continuous currents of 40 A; collector-to-emitter breakdown voltages range from 350 to 400 V. An internal base-emitter diode across the input transistor gives an inductive-load storage time of just 1.9 μs and an inductive crossover time of 0.6 μs.


NITROGEN BACKFILL TUBE
INSERTION OF DRY NITROGEN INTO LOWER CHAMBER
STRESS RELIEVING COPPER LEAD
UPPER CHAMBER FILLED WITH EPOXY, SEALS HOUSING
STRESS RELIEVING TOP & BOTTOM MOLY PLATES
SINGLE SILICON CHIP
STRESS FREE LOWER CHAMBER ENCLOSING SILICON SUBASSEMBLIES - NITROGEN FILLED FOR BLOCKING LIFE STABILITY
COPPER PADS DIRECTLY BONDED TO CERAMIC FOR MAXIMUM HEAT SPREADING AREA (GE PATENTED)
HIGH THERMAL CONDUCTIVITY CERAMIC
COPPER BASE PLATE

3. The TO-3 can is not the last word in power packaging, as shown by this innovative Darlington housing from General Electric's Semiconductor Div. Nitrogen gas, inserted into the chip's containment area, eliminates stress and reduces the effects of epoxy contaminents.


HI POWER SWITCHING TRANSISTOR
D60T CONSTRUCTION DETAILS D62T
Compression Washers
Solid Cu. Emitter
Ag Base Lead
Mo. Strain Buffer
Total Emitter Contact Through Mo. Preform
Triple Diffused Silicon Element Bonded to Mo. Substrate
Ag Thermal Preform
Solid Cu. Collector
Hermetic Seal

4. Westinghouse Semiconductor's compression bonded encapsulation (CBE) relies on pressure—not solder—to secure the chip to the header in the high-power dissipation D60T and D62T transistors.

No single chip can withstand the hundreds of amps at hundreds of volts of breakdown required in the highest power applications. So PowerTech (Fair

Lawn, NJ) builds uniquely metallized power transistors and puts them in solid copper Powerblock modules. A single power package, configured to a designer's custom specification and containing perhaps ten individual modules can handle up to 1000 A at breakdown voltages exceeding 400 V.

Tell a device by its package

While new power packages seem to be more in evidence, no serious challanger has emerged to the plastic TO220AB or the metal TO-3 for large-volume applications. However, the General Electric Semiconductor Products Group (Auburn, NY), Westinghouse Semiconductor (Youngwood, PA) and Solid State Devices have each developed housings that could unseat the frontrunners.

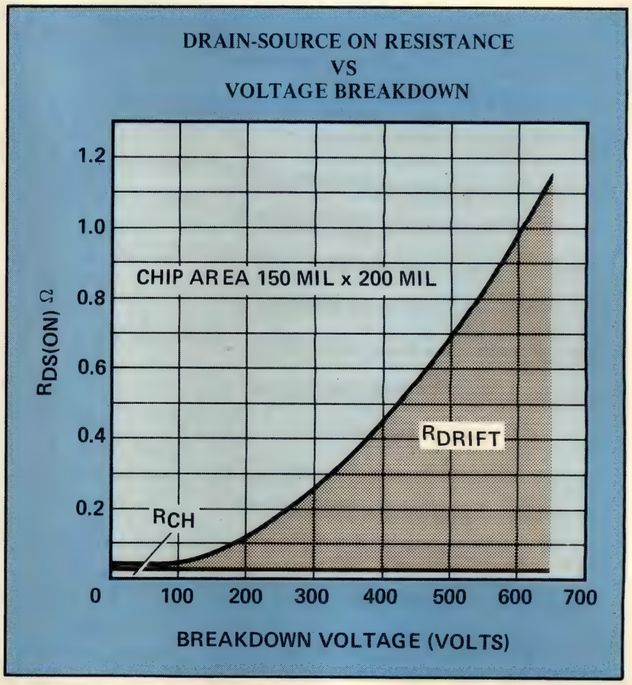
If designers could have their wish for an ideal package, two of its likely features would be electrical isolation, and terminals that point up, rather than down, through the heat-sink surface.

At least one company, General Electric's Semiconductor Group, is responding to that wish. Its recent line of power Darlington's, the D66 and D67, feature collector isolation from the heat sink and quick-connect electrical terminals facing away from the mounting surface (Fig. 3). More interesting is the evacuation and backfilling of the package with nitrogen gas. The package is subdivided into two chambers—the upper chamber is filled with epoxy, sealing the nitrogen in the lower. The effect is to create a stress-free lower chamber, allowing the silicon chip to operate in an atmosphere devoid of stress-forming encapsulants and poisonous gasses. Gasses are usually created during the epoxy curing process.

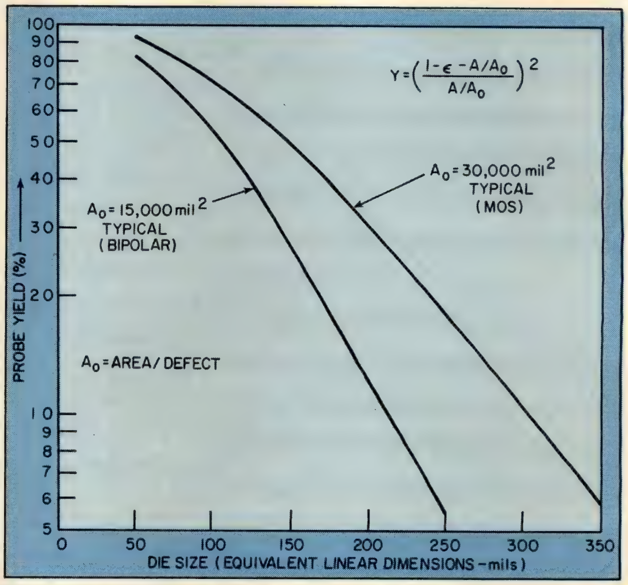
Another feature of GE's package is the use of molybdenum top and bottom plates, together with a braided coppper lead, to improve the device's thermal cycling capability. These techniques allow the Darlingtons to carry high collector currents—50 A continuous, 75 A peak for the D66, and 100-A continuous, 150-A peak in the D67.

When high current—more than 100 A—and high voltage—more than 400 V—meet in the same circuit, very special packaging measures must be taken to ensure the survival of the power device. For this application, some transistors make use of a chip-mounting technology called compression-bonded encapsulation (CBE) to bond the transistor to the case. Rather than solder, CBE is pressure mounting, which is far less susceptible to thermal fatigue failure. The technique can be used in many package styles—stud, disk, integral heat sink or flat base.

The Westinghouse D60T, for example, comes in a stud-mounted package and is rated to dissipate 590 W at a case temperature of 75 C. The company's D62T, with the same size chip and also in a stud-



5. In MOS processing, on-state resistance increases with breakdown voltage. The relationship is exponential: $R_{DS(ON)}$ increases by a power of 2.3 to 2.7 times the breakdown voltage, depending on the process.



6. MOS dice must be larger than bipolar dice to handle the equivalent amount of power; therefore, MOS yields are lower than bipolar yields and MOS devices cost more. A graph from Integrated Circuit Engineering Corp. (Scottsdale, AZ) illustrates the production problem.

VDMOS and VMOS: Basic names in MOS technology

To judge by the names manufacturers assign to chip geometries, MOS transistors fall into a half-a-dozen categories. In fact, most devices available in any quantity can be grouped into simpler classifications.

The two basic MOS structures are vertical double-diffused (VDMOS) and V-groove double-diffused (VMOS). In both, current flows vertically, between the front and back surfaces of the device. Both are designed to maximize the perimeter of the source per unit area for large current handling capability, and to minimize the on-resistance per unit area for a given breakdown voltage.

Other names for vertical devices are DMOS, TMOS, ZMOS and, in the case of International Rectifier, HEXFET. Two terms associated with both VDMOS and VMOS describe the way in which the source and gate regions are accessed. Interdigitated access is the older method. In this geometry (see top figure) source and gate access lines are adjacent to each other, but do not overlap.

In dual-level access (see bottom figure), source and gate access lines are on different levels, separated by an insulating layer. The dual-level method provides a greater source perimeter, hence, greater current density. However, in dual-access structures, the overlap of source metallization and the gate region increases the possibility of device failure resulting from defects in the intermediate dielectric layer.

The most notable difference between VDMOS and VMOS technology is in breakdown voltage. Most of the high-voltage breakdown (400 to 500-V) chips are VDMOS. Recently Siliconix announced a 400-V VMOS unit, but breakdown ratings for VMOS devices are almost always in the 40 to 120-V range.

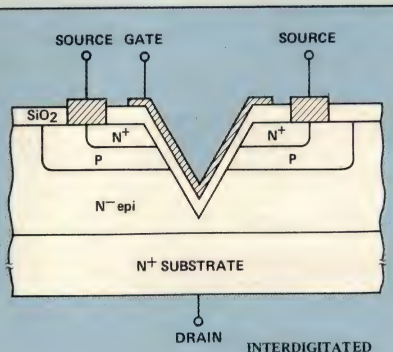
VMOS transistors can be either V-groove or (at companies such as Siliconix and Intersil), U-groove. VMOS processing with V-groove uses the silicon area efficiently, but the sharp bottom of the V-groove is a drawback. At the point of the V, a strong field concentration develops between gate and drain and the gate oxide layer tends to be quite thin. The result is limited high-voltage capability, because of gate oxide breakdown, even though the gate does not experience the full drain-to-source voltage.

The V-groove problem can be solved by turning the V into a U. U-groove and V-groove gate geometries are similar, except that, in U-groove, the etching process that forms the groove stops while the groove is still relatively wide (etched field termination).

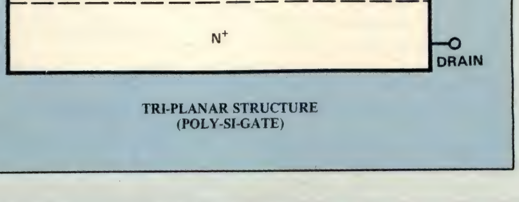
The gate area can be covered with a polycrystalline silicon doped with phosphorous (silicon-gate process) to improve manufacturing yields, as well as breakdown voltages. Although polysilicon is an effective ion migration barrier, it is a poor conductor, and can slow the device's turn-on. Therefore, a layer of high-conductivity aluminum is deposited over the polysilicon to improve switching time. Silicon-gate processing has replaced the older metal-gate processing because, among other advantages, the technique results in much lower leakage currents.

In general, the ability of any MOS structure to withstand high reverse voltage is governed by the body-to-drain junction. Two techniques help to obtain the high breakdown voltages of VDMOS devices. (They could also be used in VMOS devices since the structures are similar.) The first method, called field plates, distributes the depletion region around the body-drain junction. The second, field limiting rings, used by Supertex in its 500-V devices, uses floating rings of body diffusion to distribute the voltage between the source and drain regions.

Regardless of the variations in the geometry and processing of their devices, MOS manufacturers all aim to achieve the lowest possible value of on-state resistance ($R_{DS(ON)}$). This parameter, the figure of merit for any power MOS transistor, determines how effectively it operates as a switch. Unfortunately, on-resistance is proportional to die area—the larger the die, the lower the resistance, the better the switch. But large die give poor yields, a fact that keeps MOS prices higher than bipolar, and—for now—makes it difficult for MOS to become a factor in many applications for which is is otherwise well suited.



INTERDIGITATED STRUCTURE



TRI-PLANAR STRUCTURE
(POLY-SI-GATE)

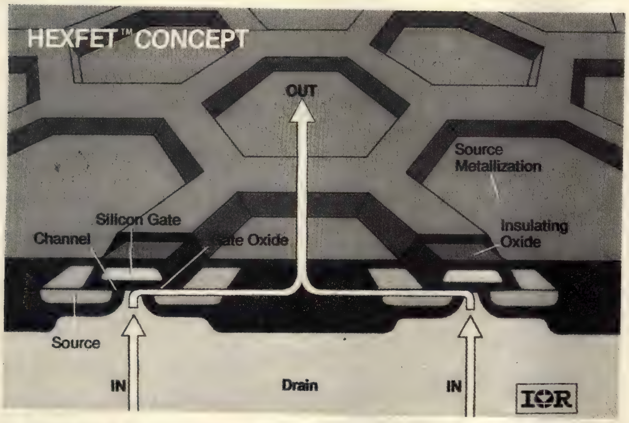
mounted package, can handle 1100 W at 75 C case temperature. The difference is in the case—the 62T is housed in a disk package, which can be cooled on both sides, permitting a significant increase in power dissipation (Fig. 4).

Solid State Devices offers so-called mini-stud packaging. The mini-stud transistor is a 5-A npn that can dissipate 12-W while occupying a mere 6.6×10^{-3} in.^{3} of board space. Packaged in an inverted TO-111 case, the chip is bonded to a beryllium-oxide wafer. The wafer, in turn, attaches to a 4-36 copper stud. As in power hybrid devices, the beryllium wafer fills the dual role of electrical isolation and superior thermal conduction.

What next for power MOS?

The advances in MOS technology—higher breakdown voltages and greater power handling capability—have been so rapid that one wonders what might key this year's developments. In truth, a temporary plateau at the 500-V breakdown level may have been reached for reasons inherent in MOS technology itself (see "VDMOS and VMOS: Basic Names in MOS Technology").

8. The cellular structure of a new high-voltage VMOS transistor features perpendicular grooves. Developed by Siliconix, the polysilicon gate structure achieves high packing density and high breakdown capability.



7. HEXFET, International Rectifier's MOS process, exemplifies the DMOS technique for manufacturing transistors with high breakdown voltages. The source cells—closed hexagonal channels—are formed by an LSI process, giving a density of more than 500,000 cells per square inch.

In the MOS process, higher breakdown voltages must be accompanied by larger values of on-resistance for a given die area, and the two are exponentially related (Fig. 5). For example, if the breakdown voltage of a 100-V, 1-Ω device is to be increased to 200 V, the die area must increase fivefold to maintain the same on-resistance. Moreover, the technology is such that increasing the breakdown voltage for a given die area reduces the chip's power handling ability. To get more power capability, the die must be made larger.

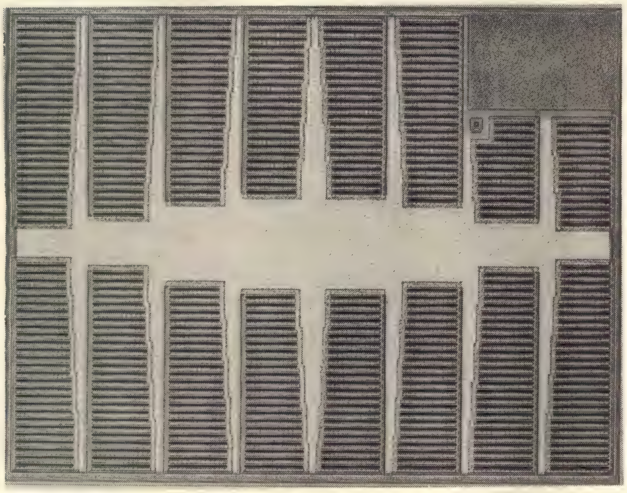
When die size increases, both yields and cost suffer (Fig. 6). Fewer devices are on each wafer to begin with; after processing, the number of surviving chips falls even further. Necessarily, each transistor costs more. For the near term, the nature of the technology will make MOS devices more expensive than comparable bipolar devices. On the other side of the coin, MOS technology has a much faster switching speed, no second breakdown effects and fewer drive circuit requirements than bipolar devices.

One product for the future is the hybrid MOS power device. Putting several paralleled MOS transistors in a single package makes sense because the arrangement capitalizes on one of the technology's strengths—the ability of the devices to share current and avoid the current-hogging problem of bipolars. This approach could relieve some of the pressure to build larger devices, since many of the smaller chips would be suitable for paralleling.

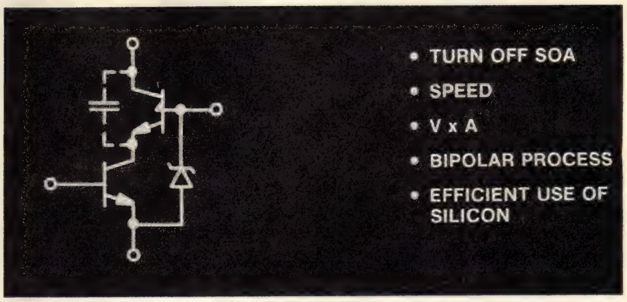
Problems aside, an impressive number and variety of power MOS products are available. In high voltage, International Rectifier (El Segundo, CA) and Supertex (Sunnyvale, CA) have introduced DMOS devices with 400 to 500-V breakdowns. IR's IRF430 and 830 transistors (Fig. 7), are high-power cousins—500-V rated, with $R_{DS(ON)}$ specifications of 1.5 Ω.

The 430 is packaged in metal TO-3 and the 830 in plastic TO-220AB. IR's products come in three forms —metal can, plastic package and chip.

Supertex looks like the high power leader with its VNO4 family, introduced during the past year. Breakdown voltages are rated from 350 to 500 V, and current carrying capability runs as high as 12 A. The chips are packaged in TO-3 for high power applications or TO-39 for low power. Supertex also provides chips for designers who do their own packaging.



9. The bottom of a V-groove flattens out to form a U-groove that eliminates some of the breakdown problems of V-groove devices. Intersil's IVN5200 power VMOS chips embody the U-groove structure, with silicon-gate processing.



10. Switching a 20-A inductive load, the bipolar cascode switch from General Semiconductor Industries turns off much faster than a normal bipolar transistor. And a snubber for inductive loads is not required.

Despite those who think that DMOS technology is the only path to high breakdown, Siliconix (Santa Clara, CA), recently provided an alternative. Long the leader in VMOS, Siliconix now boasts the highest breakdown V-groove transistor—the VN4000A family with drain-to-source ratings of 400 V, and current handling capability of 8-A continuous. The company will not concede that DMOS will command all high-voltage applications. Control of the etching process is the key to manufacturing MOS devices, and Siliconix has more experience than anyone else.

In low-voltage VMOS technology, Intersil offers a very broad line in its IVN5000 series. With breakdown voltages ranging between 40 and 80 V, the family's current ratings span 1.2 to 5 A. Packages include TO-52, TO-39, TO-66 and TO-3 in metal; TO-237, TO-202 and TO-220 in plastic.

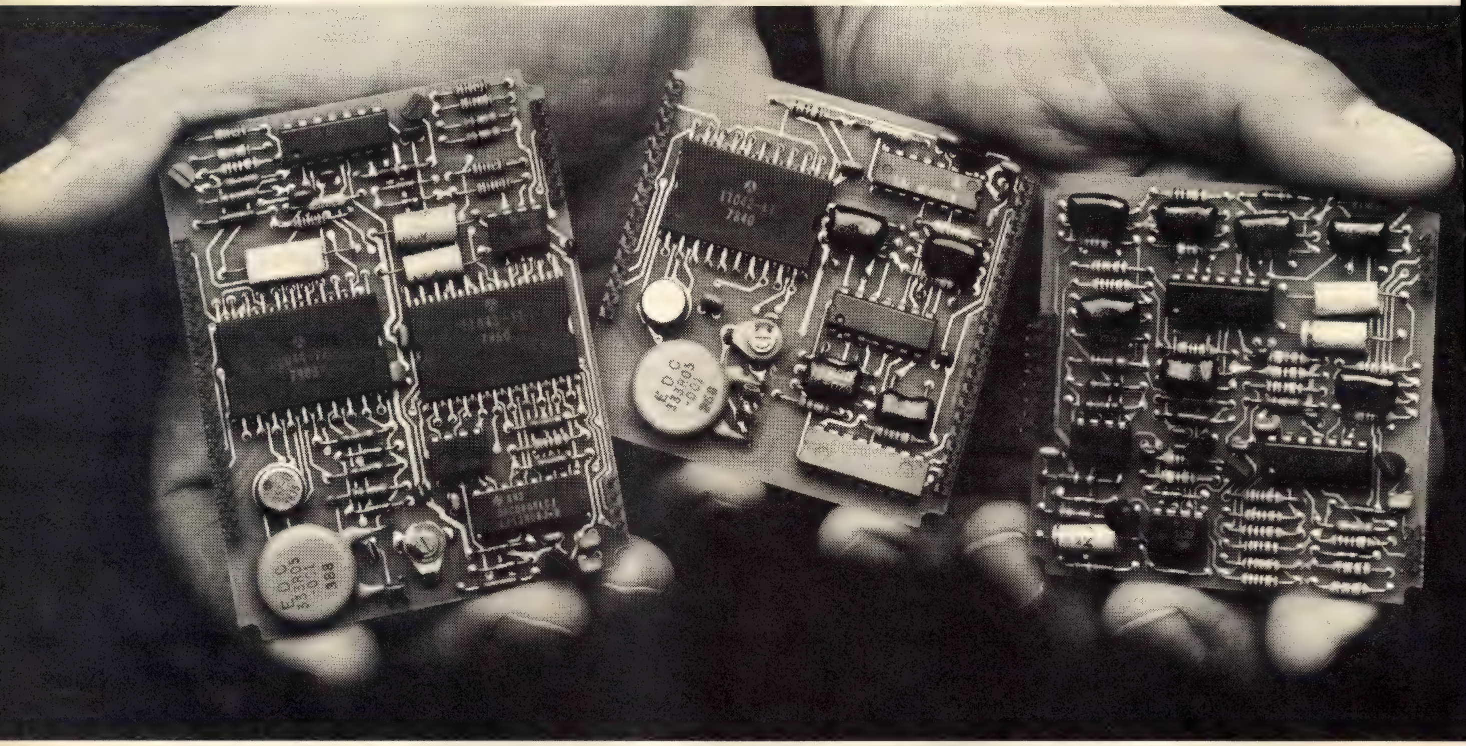
Intersil (Cupertino, CA) has a variation on V-groove, called the U-groove structure. (Siliconix also produces U-groove.) The U-groove eliminates some of the breakdown problems caused by the sharp point of a V-groove (Fig. 9). Texas Instruments builds V-groove, but is considering vertical DMOS for units having higher breakdown voltages.

Texas Instruments uses V-groove techniques for its TIPF series. The 40 to 80-V breakdown parts are plastic packaged (TO-220) and carry current in the 2 to 3 A range.

From Germany, Siemens throws its hat into the MOS ring with a vertical DMOS structure that has not yet led to high-voltage products, although current carrying is impressive. The BUZ series of devices can carry up to 12 A, but breakdown voltages are in the 100-V vicinity. Before long, Motorola and RCA's Solid State Div. will enter the competition.

Rather than introducing devices at the heady pace of recent months, it is more likely that MOS makers will try to consolidate recent gains. To get users interested in the technology, manufacturers must achieve standardization of parts and specifications, in addition to greater production.□

R24. The first 2400 bps modular modem.



Rockwell's compact MOS-LSI modem gives new physical design freedom.

Micro power

Rockwell's R24 Modem is the most compact 2400 bps MOS-LSI modem available today. Its small size and modularity give designers a whole new form factor flexibility. Requiring only 25 square inches of system area, the R24 is ideal for terminals and communications equipment.

The R24 provides functional flexibility also. Of its 3 modules, one is the transmitter, two the receiver. Terminal designers can offer transmit-only or receive-only options. And, the R24 is Bell 201 B/C and CCITT V.26 and V.26 bis compatible.

With its major functions in LSI circuits, the R24 is solid-state reliable and economical. It can be configured for operation on either leased lines or the general switched network. And, each low-profile module can be plugged into standard connectors or wave soldered onto system PC boards.

A new generation of modems from the company that's delivered more high-speed modems than anyone in the world. That's Rockwell Micropower!

For more information, contact Modem Marketing, Electronic Devices Division, Rockwell International, P.O. Box 3669, RC 55, Anaheim, California 92803. (714) 632-5535.

Rockwell International

...where science gets down to business

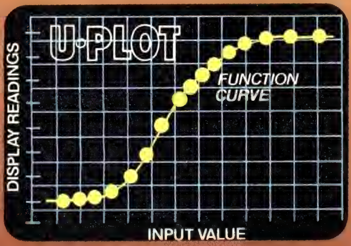
CIRCLE NO. 43

Why is the DigiTec Datalogger 3000 already the most popular logger in the world?

most powerful & easiest to use

The Datalogger 3000 puts more power in your hands than any other datalogger.

MORE DATA ACQUISITION. The 3000 handles the widest variety of inputs: ac and dc voltages, ac and dc currents, resistances, *all* thermocouples, RTD's, thermistors, digital and contact closures—*all standard.*



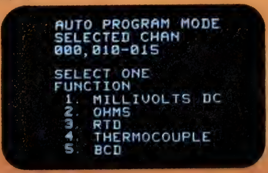
MORE COMPUTATION. The 3000 opens up the power of mathematical computation. It can determine an Average, Difference, Deviation from a Mean, extract Square-Roots and more. You can easily convert to engineering units with 30 programmable offset and scale factors. That's 900 different m x + b equations. Two unique tables feature the exclusive "U-PLOT" function (User-Programmable Linearization Tables). This powerful feature provides linearization for any transducer or transmitter.

MORE DECISIONS. The 3000 offers 100 programmable set-points for alarm detection. You can assign up to 4 different limits, with priority levels, to each channel for "High," "Low," or "Equal to" decisions. You can Alarm on rate of change or alarm transition. Ten *standard* Alarm Relays provide outputs for annunciation and control. And, only DigiTec Dataloggers visually spell out alarm messages on a built-in CRT.

Behind all these standard features is 32K of memory. That's enough power to support a system of up to 1000 points.

The Datalogger 3000 . . . more powerful than any other datalogger.

The Datalogger 3000 is as easy to use as it is powerful. All communication is in everyday English. We spent man-years developing programming innovations so you can program your system in minutes.



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AUTO PROGRAM MODE
SELECTED CHAN
000,010-015

SELECT ONE
FUNCTION
 1. MILLIVOLTS DC
 2. OHMS
 3. RTD
 4. THERMOCOUPLE
 5. BCD
```

PROGRAM PROMPTING. A built-in CRT display provides prompting to guide you through each step of your program. The Datalogger asks you simple questions in plain English and supplies multiple-choice answers. This interactive prompting assures quick and accurate program entry. Programming is further simplified by utilization of conventional data acquisition terms, no need for complex, computer languages.

CASSETTE LIBRARY. Once your program requirements have been defined, they can be saved on the built-in cassette. This lets you create a library of application tapes. Simply drop in a cassette and the Datalogger will completely program itself. Changing programs, therefore, is as easy as changing cassettes. The same cassette deck can be used to record measured data for future reference.

COMPLETE COMMUNICATION. The built-in CRT provides more information than possible with conventional datalogger displays. You can see 10 channels of system information at a single glance. For hard copy, *a standard,* built-in alphanumeric printer quietly records data. To communicate with peripheral devices, the 3000 offers the widest variety of interfaces. ASCII outputs, both serial and parallel, relay outputs, external condition input, and composite video output are all *standard.*

The Datalogger 3000 . . . easier to use than any other datalogger.

For a free brochure or "hands-on" demonstration, just call Daryl Barnaby collect, (513) 254-6251

DigiTec.
UNITED SYSTEMS CORPORATION
918 Woodley Road, Dayton, Ohio 45403
(513) 254-6251, TWX (810) 459-1728

CIRCLE NO. 48

CIRCLE NO. 58

It's a standard, catalogued item. Yet, it probably has everything you'd specify if you were ordering such a connector to be custom-made. Especially if you're concerned about reliability.

This particular connector has bifurcated bellows contacts that are plated with gold over nickel. Its 100 contacts are spaced .125" × .250" centers. Insulator material is diallyl phthalate per MIL-M-14F Type SDGF. The real beauty of it is that you can order 5,000 of these connectors and every one you receive will be like every other one. They're created equal. So, they're all *reliable*.

The same is true of other standard Elco card-edge connectors. They're competitively priced and promptly available from Elco's connector-oriented distributors in popular sizes (up to 100 contacts), with popular spacings (.100", .125", .150", .156"), and with a wide variety of terminal styles.

For the names of Elco distributors near you and a copy of our Card-Edge Connector Catalog, write to ELCO Connector Division, Huntingdon Industrial Park, Huntingdon, Pa. 16652. Tel. 814-643-0700. TWX 510-691-3117.

G+W **Elco Corporation**
a Gulf + Western manufacturing company

CIRCLE NO. 44

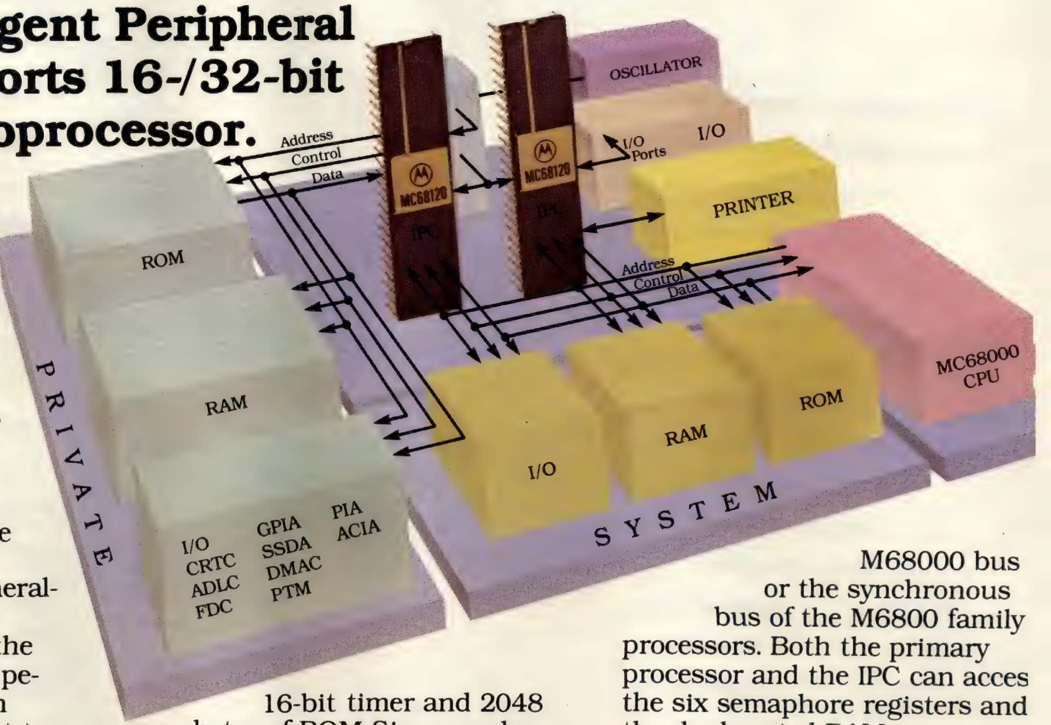
Motorola Reports

INTELLIGENT PERIPHERAL CONTROLLER

☐ MC68120 IPC launches compl
M68000 peripheral-chip famil
☐ LSI simplifies telecommunica
☐ A switch to power supply eco
☐ New help for system data secu
☐ Fast fiber optics scores again

MOTOROLA INC.

Motorola Intelligent Peripheral Controller supports 16-/32-bit MC68000 microprocessor.



Motorola's new MC68120 Intelligent Peripheral Controller (IPC) is the first in a complete peripheral-chip family for support of our advanced 16-/32-bit MC68000 microprocessor.

The powerful MC68000 is in volume production and is available both in chip form and as the brains of the '68KDM design module at the board level.

The MC68120 IPC is a general-purpose, user-programmable peripheral control unit, and the first of the MC68000-system peripherals we will announce in 1980. It's an ideal supplement to the existing family of Motorola support peripherals and provides next-generation enhancements to the MC68000-based systems of today.

Use the IPC for local or customized peripheral control, as an I/O preprocessor or as a satellite processing unit for distributed processing. Typical applications can include functions of a file handler, intelligent floppy disk or hard disk controller, data communications protocol controller, GPIA bus management controller, CRT driver and many others.

The MC68120 is both software and bus compatible with the synchronous bus of the M6800 family processors and peripherals, as well as with the asynchronous bus of the MC68000 for which it was primarily designed. The control program, up to 64K bytes in length, can be stored in the on-board ROM or in external memory which is accessible in one of the expanded operating modes.

Speaking of operating modes, the MC68120 will operate in any of eight Single-Chip, Expanded Non-Multiplexed, Expanded Multiplexed and Test Modes. The IPC contains a dual-port 128-byte RAM with system bus interface, serial communications interface, 21 parallel I/O lines, multi-function 16-bit timer and 2048 bytes of ROM. Six semaphore registers are accessible to both the on-board CPU or an external processor. The CPU executes an enhanced '6800 instruction set and includes an 8 x 8 multiply. The programming model features two 8-bit accumulators which can be used separately, or together to form a 16-bit accumulator.

Access to the MC68120 by the primary processing system is via the IPC's System Bus, which interfaces with either the asynchronous M68000 bus or the synchronous bus of the M6800 family processors. Both the primary processor and the IPC can acces the six semaphore registers and the dual-ported RAM.

The IPC is a vital, versatile M68000 system component, one o an ever growing family. Watch fo the announcements of more famil components soon. In the meantime, the MC68000 is available for evaluation and design-in with high level software and a complet development system.

It's a fast-paced world. M6800 systems can help your products stay in front.

Check ☐ A for information.

Motorola committed to meet standard CMOS deman

Motorola presently offers the industry's best delivery performance of the widest existing selection of CMOS standard functions. Delivery of most standard types is 10 weeks or less, and our capacity is still growing to meet increasing demands.

Two new brochures, the *CMOS Function Selector Guide* and the *CMOS Cross Reference Guide*, detail this broad Motorola standard logic CMOS family.

The selector guide lists more than 110 standard series devices by number and function, plus B Series and UB CMOS information.

Also included is a description of Motorola's "Better" program of three different process flow levels for enhancement of commercial device reliability at a fraction of military grade product costs.

The cross reference lists second sources by device type for Motorol standard CMOS ICs.

As greater complexity is achieved, such as the single-chip combination of analog and digital, CMOS op amps and frequency synthesizers, CMOS viability as an LSI technology is clearly confirmed.

With the broadest standard product line and a factory equipped to meet growing product demand, Motorola enters the '80s prepared to maintain and increase our leadership role in standard CMOS.

Check ☐ B for information.

Cut system cost down to size with Our multi-output mini-switcher.

Now you can have a full-featured switching power supply with l the quality and reliability of igger, more expensive units without all the cost.

Motorola introduces the 0FS65 conomy series of open-frame upplies designed for MPU, terminal, display system and other wer-power applications requiring outputs from 25 W to 65 W.

Cooler and more efficient than quivalent linears, parts count r the family is about 20% less han similar switcher types for igher MTBF — also a key ost reducing element. There are o fans needed for cooling, the esign boasts about 1.5 W output er cubic inch and efficiency for he triple-output supply is approximately 65%.

Small and lightweight (about 1 oz.), the 0FS series offers ophisticated, Cadillac performance in an economy car framework. Fully self-protected from buse at output terminals, shorts nd opens can't damage it with igh, low, or in-between voltages. Overload simply causes periodic recycling with normalcy restored when overload is gone.

And if your system's going to crash due to power line failure, it sends a warning signal to the MPU to unload volatile memory with output voltage remaining within regulation for 32 ms after loss of nominal line voltage. That's about twice as long a hold-up time as others offer.

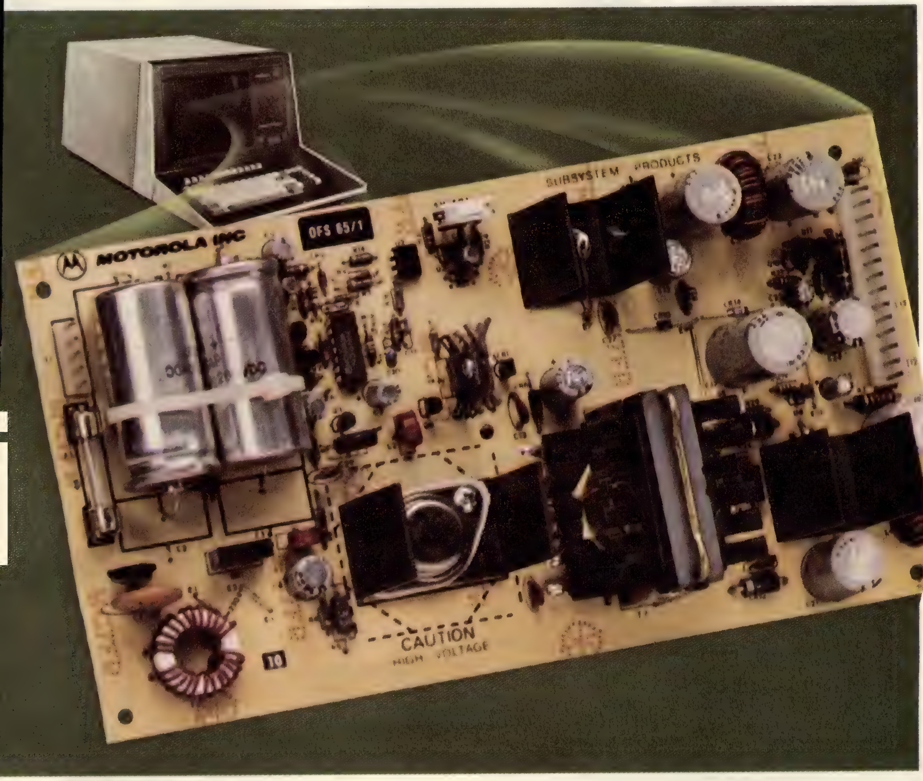
Of course, it provides EMI filter on input, soft start and reverse polarity protection.

Standard, 24-hour burn-in is included and reliability ensured through computer-aided, worst-case analysis and individual testing of every IC and discrete device.

Max load and line reg for the +5, +12 and +15 V outputs are 1% and ± 0.15% and 6% and ± 0.15% for the −12 V and −15 V outputs.

Best of all, prices are down where they should be: $130, 100-249 — and you have Motorola's reputation for quality, integrity and conservative design in the bargain.

Check ☐ C for information.



Kiss complexity goodbye with the first 100 mA, 3-terminal adjustable voltage regulator.

Say hello to LM117L/217L/317L — the first low-current, linear voltage regulator to use just two resistors to set output voltage.

Because it's packaged in a compact TO-39 or TO-92, it's ideal for use freely in spot regulation throughout a board. No large, expensive, single regulators that may or may not keep every isolated subsystem on track. No cross-talk, no loss through line resistance.

Because it's adjustable, there's no need for op amps, caps or stocking many fixed voltages to attain adjustability.

Because it's positive, the IC obviates need for ground referencing. Since you need only a differential voltage to set up V_{out}, the regulator never sees more than the V_{in}-V_{out} value. Operation in floating systems at high voltages with respect to ground is easily attained.

And because it's simple, easy and economical, you have regulation exactly where you want it.

Except for I_{max}, the LM117L/217L/317L provides the same fine specs as the 1.5A LM317: adjustable ouput range from 1.2 V to 37 V; internal thermal shutdown and short circuit protection; ripple rejection almost twice as good as the MC78L series and output transistor safe-area compensation.

Line reg's 0.05%/V max for the '117L/217L and 0.07%/V for the '317L. Type numbers designate military, industrial or commercial temp range.

100-Up price for the LM317LZ series is just 52¢.

Check ☐ D for information.

TYPE	100 mA	500 mA	1500 mA
Pos Adj	117L		117
Pos Fixed	78L00	78M00	7800/C/A/AC, 140/340*
Neg Fixed	79L00		7900C

*Tighter-spec'd 7800 version in TO-3.

A single fast LSI chip increases system security.

You can build extra data protection into your system now with a single LSI device, and still get 400K bps speed.

Motorola's MC6859 provides both the unusual two-key security capability and great speed in performance of the National Bureau of Standards data encryption algorithm. It's far the fastest data security approach able to supply two-key protection.

Previously we made this data encryption device available only as a proprietary function installed in modules and stand-alone systems. Now it's also available in chip form for any system dealing with sensitive or confidential information such as in banks, insurance firms and credit card companies.

The NBS encryption algorithm has been widely accepted as an industry standard for system security. It calls for the "scrambling" of confidential information to make it unintelligible to unauthorized parties. All qualified schemes operate basically by transforming 64-bit (8-byte) wo into different 64-bit words, usi a 56-bit "key" to determine th coding. When the key is know the scrambled data can be deciphered.

Motorola's MC6859 design lows optimum security and fle ibility. It permits several approaches for coding the algorithm. For example, the prima key may encrypt a "coded text" secondary key which is in turn used for encoding the algorith In another approach, the prim key may be followed by a "plai text" secondary key. Or, the us may elect to use only a single k

The MC6859 is a fully comp ble member of the M6800 fami and operates with all family mic processors and microcomputer including the MC6809 and MC6801. As with the other M68 family peripherals, it can also used in systems based on the 16-/32-bit MC68000.

Check ☐ E for information.

5 V EPROMs . . . from 16K to 64K, lowest power and high speed. Immediately available.

The industry's broadest 16K-to-64K family of 5 volt EPROMs is now available from Motorola.

The lowest-power types in the industry, and some of the fastest, are included. They aren't simply introduced, they're available for your use.

Our low power 16K and 32K types operate on just half the power of any others. And the MCM68L764/68L764-35 are far and away the lowest-power 64Ks. This is power performance unmatched anywhere. Our high-speed 16K and 32K selections have maximum access times down to 250 ns.

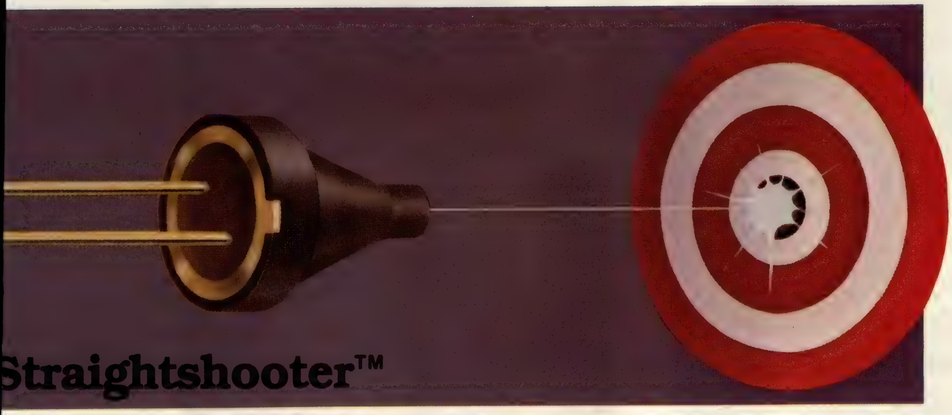
These 5 V EPROMs, including the 64Ks, are also pin compatible, in the same 24-pin package as the 8K through 64K industry standard mask-programmable ROMs. Even the 64K EPROM is a "plug-in" replacement for these ROMs, and for the smaller 5 V EPROMs.

Added attractions such as on-chip overvoltage programming protection circuitry and superior data retention capabilities help put these 5 V EPROMs in a class by themselves. And, by superior data retention, we're talking about a failure rate of only 0.001%/1,000 hours. The high-performance versions are all ±10% supply devices.

Order Motorola 5 V EPROMs now from your local Motorola sales office or authorized distributor.

The 5 V EPROMs are another piece of solid evidence, with our 64K RAM and industry-standard mask-programmable ROM famil that Motorola has taken the lea in MOS memories.

Check ☐ Q for information.



Straightshooter™ fiber optics right on target again with fast LED, detector.

We've notched another bullseye with the introduction of two new Straightshooter devices, each possessing superior response times over previous units.

The PIN photodiode, MF0D104F, has a typical response time of 2 ns at 20 V and 6 ns at 5 V . . . , 10 times faster than other ferrule types. It fits right into analog fiber optics sytems requiring bandwidth up to 100 MHz and in digital systems with speed requirements to 200 MBaud. In data comm links operating at 5 V the detector's usable to 110 MBaud.

The MF0E103F LED emitter offers 15 ns typical t_{on}, t_{off} and is usable in systems to 110 MBaud.

Straightshooter packages are designed to fit directly into AMP Optimate connectors for easy, accurate interconnect with FO cables.

The Straightshooter ferruled package offers greatly improved light transfer efficiency between active device and fiber through intimate bonding of the fiber to the light-emitting or detecting surface of the semi chip. Plus rugged construction well-suited for high-volume, cost-cutting manufacturing and simple, highly-efficient interconnect due to unique, interactive design of device package and cable connectors.

In fact, the only remaining variables for you to figure out are diameter and numerical aperature of the cable according to transmission requirements. Coupling losses are easily calculated.

New, low, 100-up prices on the PIN and LED are $23 and $27.50. Complete-line data sheets are available too, as is the new Motorola LINK kit. It lets you explore the many advantages of FO systems with Straightshooter emitters, detectors, and AMP connectors. It includes basic design equations and examples, circuit ideas and data sheets for just $99.

AMP and Optimate are trademarks of AMP, Inc.

Check ☐ F for information.

Motorola launches 400 mW glass zener into Dash 1 orbit.

That old, established zener that's everybody's commodity and nobody's state-of-the-art has taken another impressive leap forward at Motorola . . . qualification to MIL-STD-19500/117D/127G Dash 1 specs which include JAN, JTX and now the first metallurgically-bonded JTXV units.

In fact, we've never stopped improving the 1N746/957/4370 family. Unlike others, it offers metallurgical bonding over the entire line — from 100 V to 1.8 V. Not a solder, but a homogeneous intermix of metal molecules between die and lead, the bond ensures true metal continuity throughout, superior structural strength, thermal conductivity and electrical integrity from end to end.

In addition, the Motorola DO-35 offers zero-defect material, low-temp glass compatible with the alloy process for sharper breakdown and lower leakage, computerized diffusion and testing, oxide passivation, laser scribing, automatic inspections, MOS-inspired processes, 100% contact tests and the largest active area with the biggest surge current rating of any DO-35.

Not your average zener, by any means.

Check ☐ G for information.

Schottky rectifiers lead total switcher support parade.

Motorola's got it all in Schottkys and fast-recovery units for the 5 V output side and standard recovery devices for the line-voltage inputs in switching power supplies. Plus a new Switchmode™ rectifier application guide.

Our eighteen 1 A to 75 A Schottky units are suitable for 1 A to 250 A (per leg) output designs and offer technological improvements that keep the outside world outside . . . an extra layer of barrier metal that effectively shuts out contamination and failure. Extensively used in LS fabrication, the layer is an interface between working barrier metal of chrome or platinum and the nickel-gold ohmic contact metal.

We tested 840 DO-4 and DO-5 units to MIL-STD-750 criteria, with no-failure results (full reports with variables data are available).

Our fast recovery units for output currents of 0.5 A to 50 A (per leg) are considered by the industry as the finest in the world. And the most available.

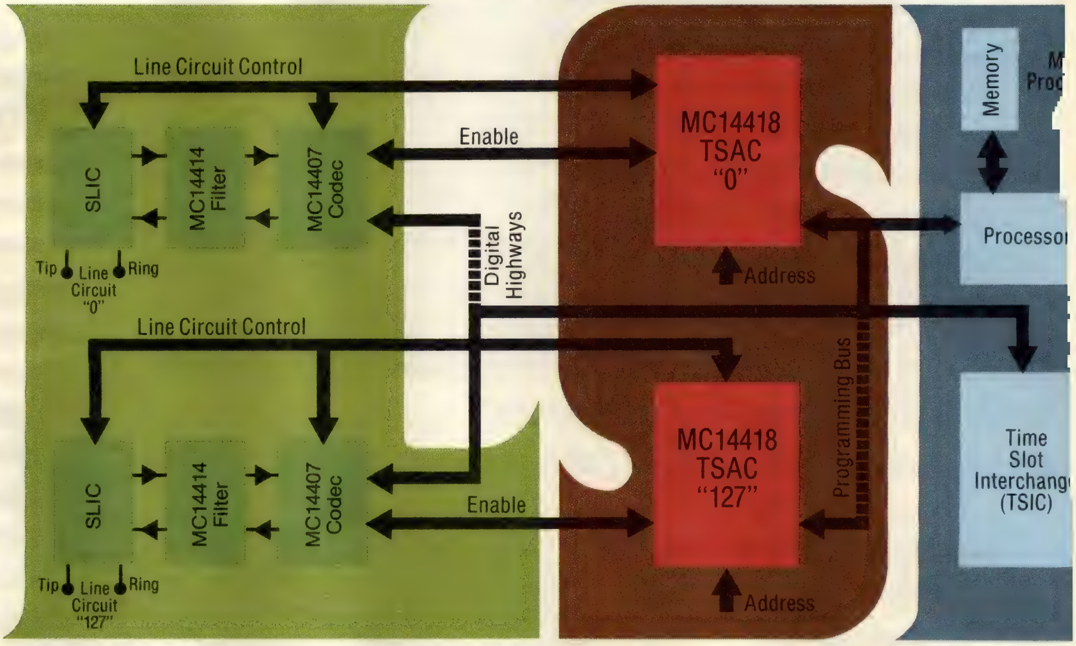
And our line of standard speed rectifiers and bridges for 1 A to 25 A line voltage use includes the Motorola-originated 1N4000 Surmetic™ series that has set the low-cost, high-volume standard for the past 15 years.

Check the reader response and receive a new Switchmode rectifier guide for your next switching power supply design.

Join the Motorola parade.

Check ☐ H for information.

LSI telecommunications circuit cuts per-channel part cou



Motorola's third major MOS LSI telecommunications function introduction in less than a year opens a new approach to per-channel time slot assignments, and simplifies the implementation of a variety of complex control functions.

It's the Time Slot Assigner Circuit. We call it the TSAC. It's an addressable, programmable per-channel unit that allows programming of the variable Codec time slot assignment through a serial microprocessor port. One Codec is assigned to each TSAC. In operation, the major function of the TSAC is to assign the Codec to transmit and receive time slots in a digital serial data stream.

Two versions of the TSAC are available. The MC14416 is a 16-pin version that performs the basic function plus off-hook multiplex control, and the 22-pin MC14418 is the full-featured device that contribues most to design simplification, lower parts count and lower costs.

The MC14418 provides a simple, unique addressing capability that allows the use of a completely parallel back plane in a channel group of PCM Codec-based equipment. It also has additional control bits for the performance of three user-programmed system functions. These might be ring enable and power down, or receive tone/data control. A reset pin which may be used for the ring trip function is also provided.

Both TSACs include chip select and clear-to-send signals for further system design simplification. The metal gate CMOS technology is used to insure maximum reliability, which enhances the increased system reliability obtained by reducing your parts count.

For years we've been supplying the telecom market with pulse converters (MC14408/09), ton encoders (MC14410), key-pad- binary encoders for telephone dialers (MC14419) and cross p switches (MC142100/5100).

Introduction of the TSAC family following our earlier Co (14404/06/07) and matched Fil families (MC14413/14), with planned introduction of SLIC (MC3419) and time slot interchange (MC145420) circuits la this year, is testimony of Motorola's commitment to serving t telecommunications industry with the highest quality, innov tive products.

Check ☐ J for information.

Motorola's full service MOS Hi Rel line now features memories.

The full service MOS Hi Rel product line of Motorola's MOS Integrated Circuit Division now features NMOS memories in addition to logic from CMOS gates to NMOS microprocessors.

Whether it's dynamic and static RAMs, binary ROMs or EPROMs, all are screened to MIL-883. We've standardized our Hi Rel memory numbering system, too, for easy ordering.

Nineteen CMOS gates, flip-flops, buffers and counters are QPL listed Part I. The entire standard CMOS family is available processed to MIL-883, Class B, method 5004 100% processing/qualifications and QCI per method 5005.

The 14000 and 14500 Series CMOS are available over the full MIL temperature range. Custom mask-provided circuits, both metal and silicon gate, can be produced over the same range.

And, don't forget that the MC6800 8-bit MPU and the key M6800 family peripherals are processed to MIL-883, Class B. These are IMHz devices that operate over the military temperature range.

Motorola Hi Rel NMOS Memories

−55°C to +125°C

STATIC RAMs
MCM2114BVBA45
MCM2114BVBA25
MCM21L14BVBA45
MCM21L14BVBA25
MCM6810BJBA

BINARY ROMs
MCM68316BJBA
MCM68332BJCA
MCM68364BJCA

−55°C to +110°C

DYNAMIC RAMs
MCM4027BEBB25
MCM4027BEBB20
MCM4116BEBB25
MCM4116BEBB20

−55°C to +100°C

EPROMs
MCM68708BJBC
MCM2708BJBC
MCM2716BJBC

−55°C to +85°C

DYNAMIC RAMs
MCM4027BEBD25
MCM4027BEBD20
MCM4116BEBD25
MCM4116BEBD20

MIL-883 processing available for all speeds @0°C to +70°C.

Check ☐ K for information.

XORmacs.™ Advanced support for the 16-/32-bit MC68000.

Motorola's EXORmacs is the new, advanced development tem that brings minicomputer ver to support of the state-of- -art MC68000 16-bit micro- cessor.

And it's time to order. The 68000 is readily available in h chip form and in the '68000 sign Module configuration.

Getting the most out of a high hnology microprocessor like MC68000, with its 32-bit ernal features, takes an equally ward looking development stem, and EXORmacs is the only swer.

EXORmacs is the new genera- n 16-/32-bit multi-user system at incorporates state-of-the-art rdware architecture with ad- nced software and self-test pability.

The shipped configuration es four of the 15 available EXOR- acs motherboard slots and rves a single user. The MPU odule has the MC68000 MPU d clock system, with a four- gment memory management nit and diagnostic firmware.

The debug module includes ACSbug™ firmware to help mplify system debug. The intel- gent floppy disk controller odule and a 128K dynamic emory module with parity com- ete the system.

VERSAbus™ is the new-gen- ation system bus for EXORmacs at has been carefully planned the industry standard for sup- orting 16-/32-bit microproces- rs in multi-user and multiple ocessing architectures.

It supports a wide variety of -bit, 16-bit and 32-bit micropro- essor architectures with high- peed data rates, and provides a xible, economical architecture eal for industrial control, com- unications or general business plications. VERSAbus is equally repared for future MPU-based stems.

Very fast cycle time, asynchro- ous bidirectional operation, MA capability, seven-level riority interrupt control, five- vel daisy chained operation and bus arbitration are just a few VERSAbus features.

The EXORmacs operating system is a multi-tasking, multiprogramming system which uses a real-time executive.

Advanced EXORmacs development software includes a PASCAL compiler and a powerful symbolic debugger called SYMbug.™

System peripherals are part of the complete EXORmacs system, too. The floppy disk is a dual-drive, double-sided single density unit providing a megabyte of storage. The line printer provides 132 column, 180 cps upper-and lower-case hard copy for the system. A Motorola EXORterm™ 155 intelligent CRT station rounds out the EXORmacs peripheral system.

Comprehensive EXORmacs support ranges from the user system emulator (USE) through items like universal I/O modules and a VERSAbus Adapter module, to training, field service and complete documentation.

It's all EXORmacs, the total new generation development system that takes you into the future, now.

Check ☐L for information.

Analog Micromodules meet real-world requirements

Motorola's Micromodule™ family is designed to make real-world system design with board-level modules just as easy and cost effective as possible.

Because a lot of that real world is analog, there's a complete complement of analog I/O modules in the Micromodule family.

You select the right A/D or D/A module for your requirements from among the six basic analog types available, hook them up, add a little software code and your system is ready to run.

Analog inputs and outputs are easily interfaced to your microcomputer system. Inputs range from low-level thermocouple (millivolts) to high level (volts), and outputs can be either high-level voltage or current.

ANALOG MICROMODULE FEATURES

High-Level Analog-to-Digital Modules
- 8-, 16-, 32-channel input
- 2.5 V, 5 V, 10 V full scale
- 12-bit resolution
- Resistor/software gain options

Low-level Analog-to-Digital Modules
- 1- and 16-channel input
- 25 mV to 80 mV full scale
- 16-bit resolution
- On-board thermocouple linearization
- Cold-junction compensation

High-Level Digital to Analog
- One-to-four channel output
- 2.5 V, 5 V, 10 V full scale
- 4 to 20 mA full scale

Motorola's Micromodule family is the versatile, powerful method for putting together the ready-to-run system you need, digital and analog.

Check ☐M for information.

53-channel CATV amps push more programs through your cable

Motorola's taken the pressure off the systems operator with introduction of the MHW4171/4172, 53-channel CATV trunk amplifiers offering 18 more channels than previous types. Designed for 40-400 MHz applications, the units offer power gain of 17 dB over the entire band.

They utilize the same, reliable, Nichrome, all-gold-metallized thin-film construction as our 35-channel units which have totalled millions of hours of trouble-free usage. The family consists of a push-pull stage with a pair of cascodes (common emitter with common base) for a total of four transistors and two transformers, a bilfilar transformer at the input and a trifilar at the output.

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You'll find the units designed to provide the best compromise of ruggedness and electrical performance. They're 100% tested to DC current, RF gain, input and output return loss, IMD, XMD at both ends, composite and three-channel triple beat and NF . . . all at 100° C case which serves as an effective burn-in.

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Design

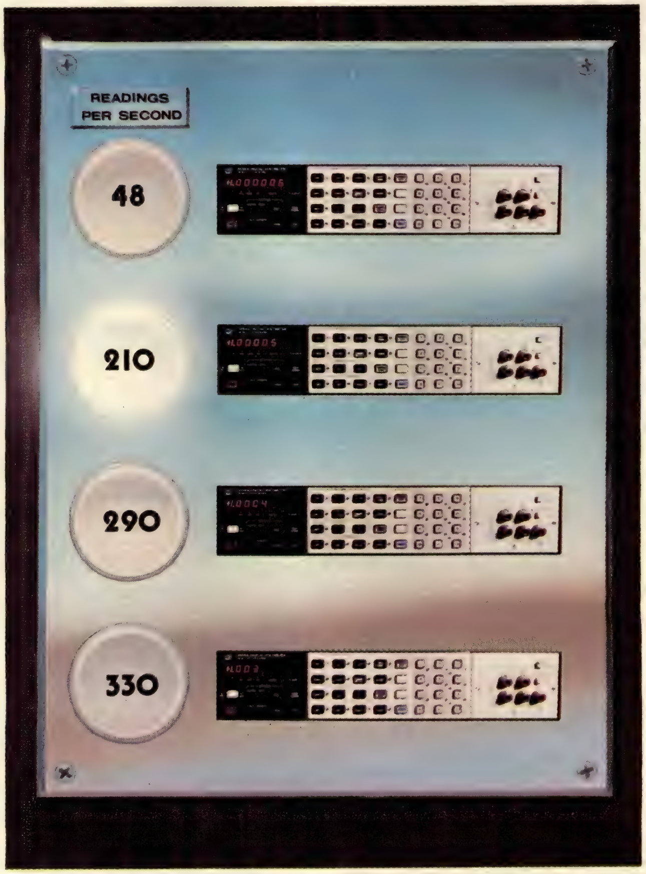
Instead of settling for the usual compromise between reading speed and accuracy or other parameters, a new digital voltmeter makes the best combination available for the choosing.

Digital voltmeter gets speedy, accurate results

Measurement accuracy, resolution or noise don't have to be significantly compromised for fast DMM readings, or vice versa. When Hewlett-Packard's 3456A integrating digital voltmeter takes on the measuring job, a user will be able, for the first time, to push a button to choose the best speed in a systems application or the best accuracy or resolution on the bench. The power behind the performance is selectable integration time; the "secret" behind selectability, an innovative a/d converter (see "Multi Slope II—A New Twist"). When reading rate counts heavily, speed up the rate by cutting integration time. If measuring accuracy takes precedence, stretch the integration time to boost accuracy (Fig. 1). Choose from integration times equivalent to 100, 10, 1, 0.1 or 0.01 power-line cycles, which correspond to rates of 0.59, 5.8, 48, 220 or 330 readings/s. What's more, at its peak, the 3456A can blaze along at almost 50 six-digit readings per second—second to none in combined speed and resolution.

Naturally, resolution will vary as a function of the reading rate. The number of digits displayed changes automatically from a top of six at integration times of 100, 10 and 1 line cycles, to four digits at 0.01 line cycles.

Kenneth Jessen, Engineer
Hewlett-Packard
Loveland Instrument Div.
Loveland, CO 80537

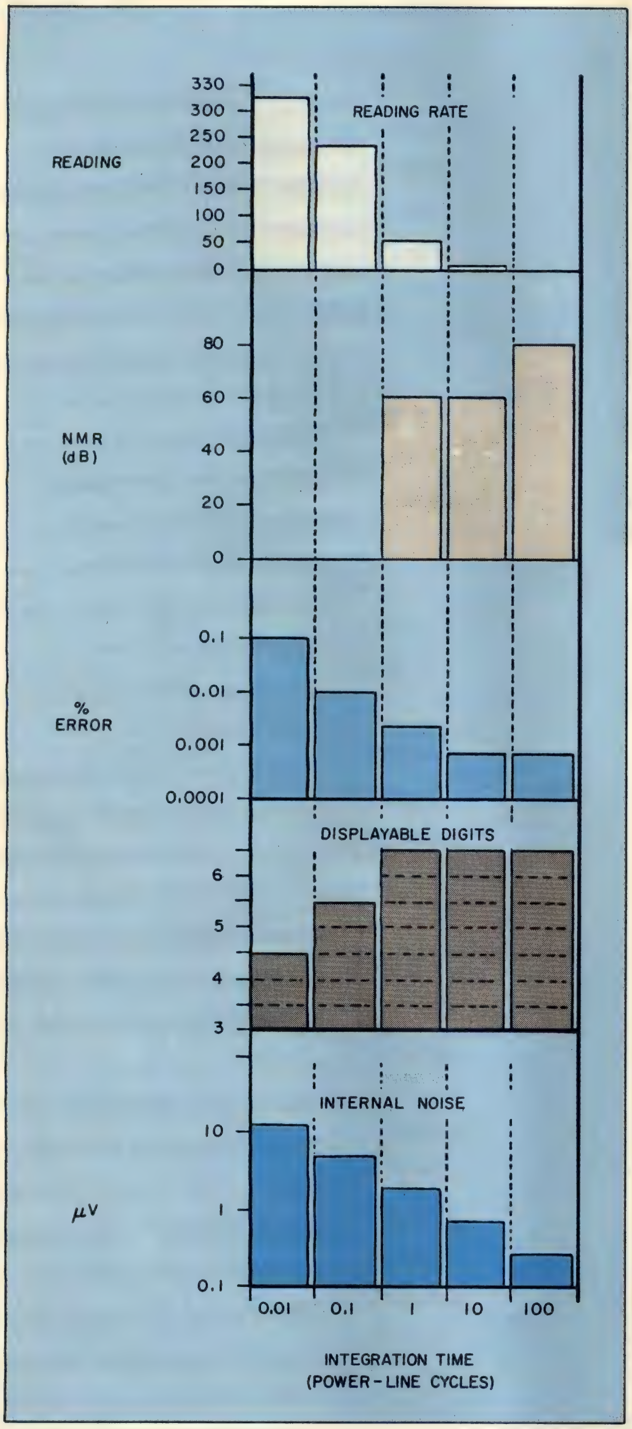


The best absolute accuracy of the 3456A is 10 ppm on the 10-V range, at integration times of 10 or 100 line cycles. On the 0.1-V range, with the same integration times, the accuracy is 46 ppm, but with 100-nV sensitivity in the last digit. Another benefit: The 3456A can be used as a transfer device with ±2-ppm resolution. Thus the unit is ideal for use in calibration labs.

Besides its dc-voltage capability, which extends from 0.1 to 1000 V in five ranges, the fully guarded 3456A measures up to 700 V of calculated true-rms (up to ten readings per second) on four ranges, over 20 Hz to 250 kHz. Best accuracy is 0.05%, resolution is 1 μV; and the crest factor exceeds 7 at full scale.

Resistance measurements, mathematical calculations controlled from the front panel (statistics, null, percentage error, dB, limits, scaling), and a built-in memory complete the unit's measuring repertoire. Front-panel calibration adjustments (Fig. 2), built-in self-testing and diagnostics round out the capabilities.

Not to be overlooked is



1. Performance of a new smart DMM depends heavily on the user's choice of integrating time. Five choices are available, so the user can optimize his application for reading speed or resolution or any other parameter.

the 3456A's ohms converter, which offers conventional two-wire and four-wire configurations, but with a new twist—offset-compensated ohms (see "Ranging In On Ohm Errors"). With offset-compensated ohms switched in, the 3456A corrects resistance measurements for undesirable thermal offsets generated by bimetallic junctions. This frees users to select any kind of metal for the test leads—and they don't have to worry about the metal on the resistor leads.

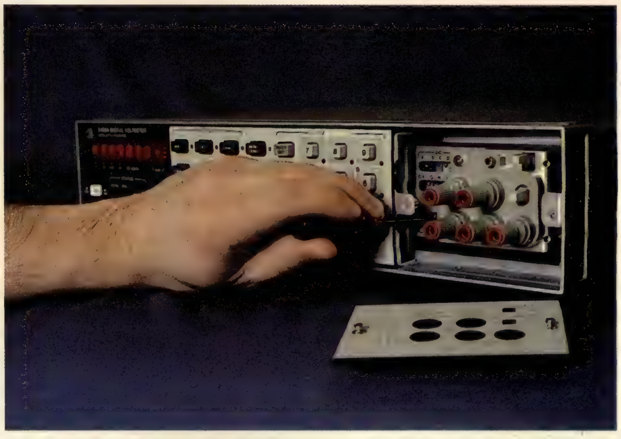
To accomplish this, the instrument first makes a normal ohms measurement, then stores the reading in memory. Next, the unit switches off its constant-current source and makes a voltage reading. Any offsets detected during the voltage reading are subtracted from the ohms measurement before the final results are displayed.

High accuracy

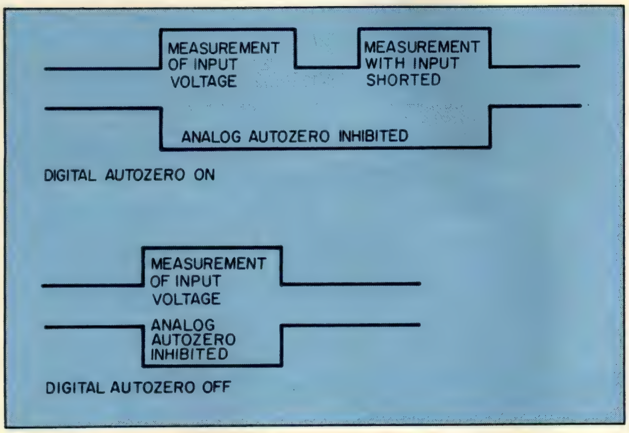
Naturally, the 3456A's ohms converter capitalizes on the low-noise, high-accuracy a/d converter. With six-digit resolution, absolute accuracy is 24 ppm or better on the 1-kΩ, 10-kΩ and 100-kΩ ranges. Ohms-converter speed is also impressive, with reading rates varying as a function of range. For example, 40 readings per second are possible on the 100-Ω through 100-kΩ ranges, 34 readings per second on the 1-MΩ range and 9.9 readings per second on the 10-MΩ range (digital autozero off, one power-line cycle of integration).

In addition, the 100-MΩ and 1-GΩ ranges are designed to give the user a general feel for extremely high resistance values. Accuracy on these respective ranges is 1.3% and 11%. Measurements are computed with a 10-MΩ shunt across the output and a 500-nA current source.

As a systems meter, the 3456A remembers up to 1400 bytes of combined measurement results and



2. One quality that is important in a systems or bench meter like the 3456A is ease of calibration. Here, all calibration adjustments are made from the front panel, so the DMM can stay in the system, and no covers need be removed.


MEASUREMENT OF INPUT VOLTAGE
MEASUREMENT WITH INPUT SHORTED
ANALOG AUTOZERO INHIBITED
DIGITAL AUTOZERO ON
MEASUREMENT OF INPUT VOLTAGE
ANALOG AUTOZERO INHIBITED
DIGITAL AUTOZERO OFF

3. In the 3456A's digital autozero mode, the meter cycles through a complete measurement, but with its input shorted. All offsets are subtracted out, at a speed tradeoff.

program information (range, function, integration time, delay, etc.). A typical set of program instructions could be 8 bytes long, leaving room for 348 readings. Delays to 999.999 s can be programmed to allow unattended operation for up to 96 hours.

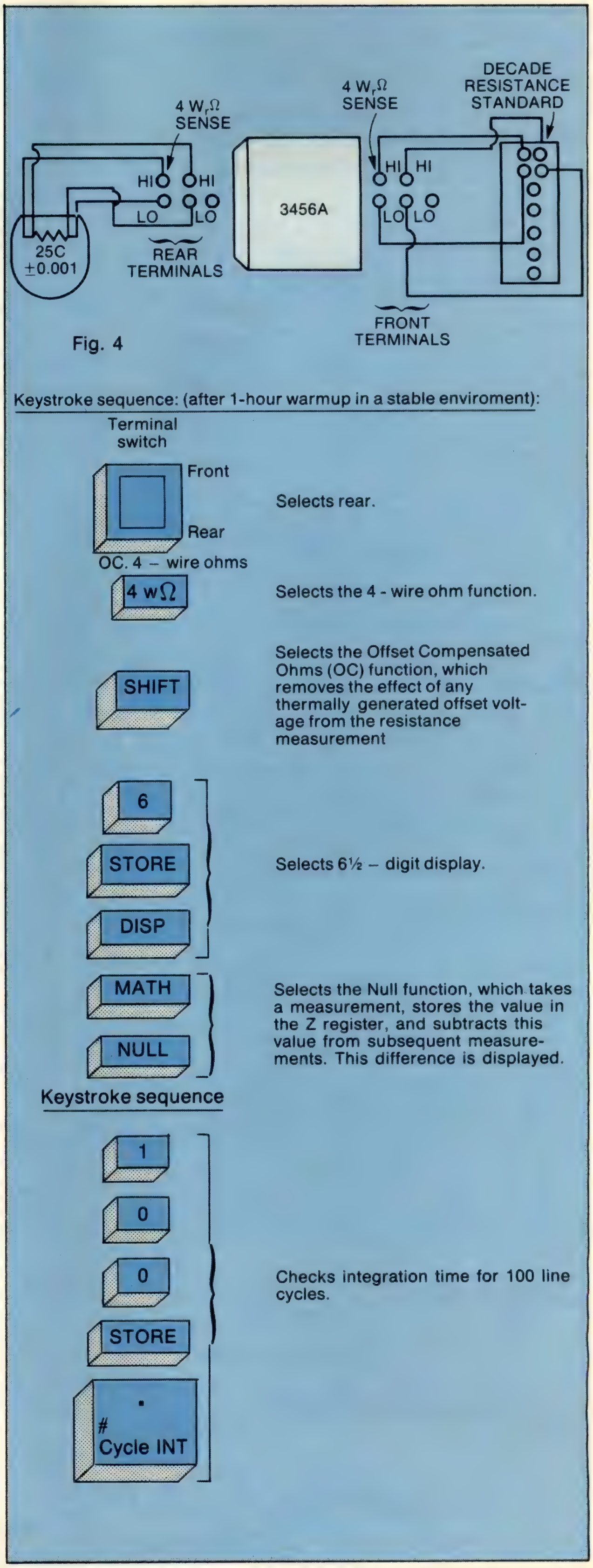
The 3456A can take a burst of measurements and store each reading for recall at the end of the burst. Or, a computer can transfer a complex sequence of program information into its memory. The instrument executes the commands, stores the result of each reading and flags the computer when the sequence is complete. The computer doesn't have to wait for the DVM; the DVM doesn't have to wait for the computer. Both devices operate at the best speed.

Even better, the unit transmits a scanner-advance signal after each reading. As a result, scanner-DVM measurement sequences can be executed at up to 330 readings per second without computer intervention.

Also selectable is the digital autozero function. When selected, autozero goes through an entire measurement cycle but with the input shorted to ground. The autozero results are stored, then subtracted from the normal measurement. (This form of autozero is not to be confused with the analog autozero performed between measurement cycles.)

Watch the glitches

Because the digital autozero is a second complete measurement, it reduces the speed of the 3456A by 1.5 to 2 times (Fig. 3). At the maximum speed, with 0.01 line cycles of integration, 220 readings can be made every second with digital autozero on and 330 with it off. Following the philosophy that a DVM's first reading should be correct, the 3456A performs one digital autozero initially, even if the function is set to OFF. The only disadvantage in having digital autozero off is that the drift of the input amplifier can be seen in the reading.



Keystroke sequence: (after 1-hour warmup in a stable enviroment):

Selects rear.

Selects the 4 - wire ohm function.

Selects the Offset Compensated Ohms (OC) function, which removes the effect of any thermally generated offset voltage from the resistance measurement

Selects 6½ – digit display.

Selects the Null function, which takes a measurement, stores the value in the Z register, and subtracts this value from subsequent measurements. This difference is displayed.

Keystroke sequence

Checks integration time for 100 line cycles.

4. A standards laboratory can call upon the 3456A's rocklike stability to transfer calibration results to working standards. Here, a precision resistance is checked. Transfer repeatability of the measurement is ±2 ppm.

Multi Slope II—a new twist

For quiet, stable readings with high normal-mode rejection, integration stands out as the best overall approach. But integration is slow. To go fast as well as slow—while offering high accuracy and resolution—the 3456A uses a new multislope a/d conversion technique.

The 3456A design takes two points into consideration:

1. Microprocessors can add and subtract a lot faster than they can multiply.
2. Considerable time can be saved during the measurement cycle if the final reading can be developed as the DVM is measuring. (One reason, for example, why successive approximation is so fast is because the reading is developed one digit at a time, so that no final tally of counts is required at the end of the measurement cycle.)

With the multiplication-process speed limits in mind, every effort has been made to force timing errors, leakage errors and the like into an offset error, which can be removed simply through addition or subtraction. This means that emphasis had to be placed on highly stable circuit gains. This was done with in-house designed and produced super Ta_2N resistors.

One good way to understand the operation of the 3456A's a/d converter is to recall the traditional dual-slope technique (Fig. A). In this approach, the input voltage is integrated during runup and the input measurement is made during rundown. Not until the final zero crossing is the answer known. Of course, the rundown slope could be made steeper to speed the measurement, but at the cost of required highspeed logic.

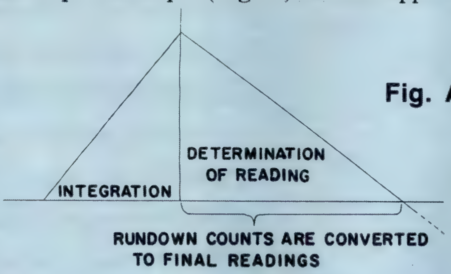


Fig. A

An early speedup scheme went beyond two slopes to multiple slopes, in which measurement times are shortened by using an extra-steep slope initially after rundown begins. Before the zero crossing, the slope is switched to a shallow one (Fig. B).

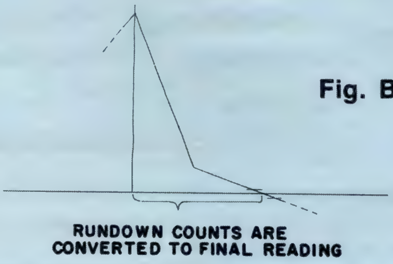


Fig. B

The a/d technique in the 3456A could very well be dubbed Multi-Slope II since it calls on many of the features of the original multislope technique:

- It's designed to go fast.
- It avoids high-speed logic in the zero comparator.
- It keeps the runup slopes steep to extend the effective dynamic range of the integrator.
- It converts during the measurement cycle.
- It pushes gain and timing errors into offset errors so they can be subtracted out.

In the 3456A, a steep rundown is applied initially (Fig. C), but a finite amount of overshoot remains beyond the zero crossing. Next, a slope exactly a decade less in steepness is applied to the remaining voltage until a second zero crossing is made, also with some overshoot. At this point, a third slope, another decade less in steepness, is applied. Then, after zero crossing, comes a fourth slope, only one thousandth as steep as the initial slope.

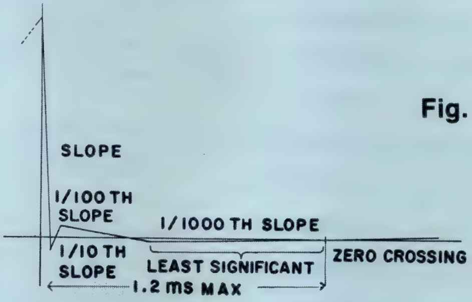


Fig. C

At the beginning of each slope, a clock starts, then stops at the zero crossing for each slope. In this way, the four least significant digits are developed sequentially for each of the four slopes during rundown from the stored counts. The rundown, therefore, has a dynamic range of ±10,000 counts. Note that the steepest slope applied initially is the least critical in absolute time for zero crossing.

The usable sensitivity of the DVM is, in part, determined by the final zero crossing, with the shallowest slope, since time to cross determines the least significant digit. In summary, the final reading is developed during rundown, not after completion.

Multi Slope II also makes contributions during runup, the integration period. With the integration time set to 100, 10 or 1 power-line cycles, the unit resolves six digits, with the first two digits established during runup.

Remember, in the dual slope's simple linear runup, the input voltage is allowed to ramp during the integration period so that the dynamic range of the integrator is not fully exploited for all input voltages. With low input voltages, the charge remaining on the integrator capacitor is proportionately less and therefore more susceptible to noise. The original version of Multi-Slope takes a sawtooth approach to keep the integrator capacitor charging at a fast rate, yet periodically switching in the reference to ramp down (Fig. D).

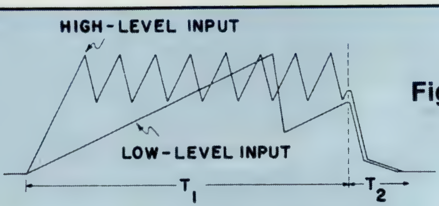


Fig. D

The problem with both techniques is that, for large input voltages (relative to full scale), the average voltage on the integrator capacitor is large prior to the rundown. Multi Slope II attempts to keep the average voltage after runup as low as possible to avoid dielectric absorption problems. But it uses the sawtooth to keep the charging rate high.

Small variations in switching time cause errors in the final reading, and if there is a lot of switching of the reference voltage, the variations can be considerable. In the original multislope technique, the magnitude of the input voltage relative to full scale determines how many switching points are made. In Fig. D, two input voltages are shown, one for a small input and the other for full scale.

By contrast, Multi Slope II holds the number of transitions constant regardless of the magnitude of the input voltage. In this way, potential timing errors are converted into an offset error. Fig. E illustrates how Multi Slope II looks for both a full-scale input and for one less than 10% of full scale.

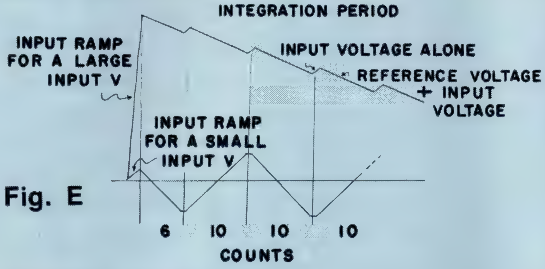


Fig. E

Because of the 3456A's autozero technique, only one reference voltage is necessary to generate both positive and negative ramps. An abbreviated schematic of the integrator is shown in Fig. F. When both S_{+4} and S_{-4} are switched to ground, as shown in Fig. F, the current (I) from the 12-V supply passes through the summing node into the integrating capacitor (C). (The summing node is a virtual ground.) This generates a negative-going ramp at the output of the integrator.

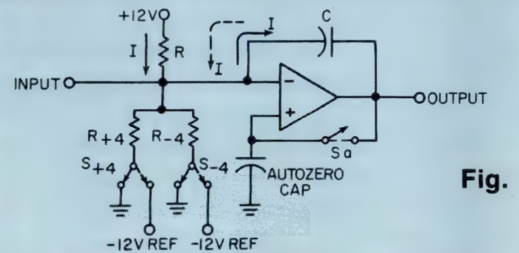


Fig. F

If both S_{+4} and S_{-4} are switched to the −12-V reference, current is sucked away from the summing node—twice that supplied by the +12-V supply. The balance of the current required to achieve equilibrium is removed from the integrator capacitor, thus generating a positive ramp on the output of the integrator.

Between each measurement cycle is an analog autozero interval. Here, S_{+4} is closed to the −12-V reference but S_{-4} is switched to ground. Since the resistances are approximately equal, any error (e) in voltage on the +12-V supply appears at the summing node as e/2 and, with S_a closed, is stored (as e/2) on the autozero capacitor.

During ramp generation, the autozero switch S_a opens and the error voltage held on the autozero capacitor elevates the positive input of the operational amplifier, thus subtracting any error in the +12-V supply. The supply, therefore, needs to have only good short-term stability. Put another way, any error in the +12-V supply is converted to an offset and subtracted during the measurement cycle.

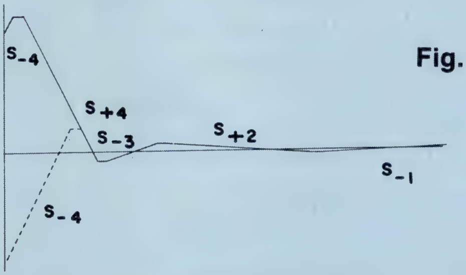


Fig. G

Small differences between R_{+4} and R_{-4} can also be averaged out simply by alternating between the two during autozero cycles—another example of how a potential gain error is converted into an offset error. In reality, R_{+4} and R_{-4} have a tolerance of 0.01%, but in effect are matched within 1 ppm.

Since the zero comparator exhibits a finite hysteresis, not only is the number of switch transitions kept constant during rundown, but ramping is arranged so that the final zero crossing always occurs from the same direction. To accomplish this, both S_{-4} and S_{+4} slopes must be applied during the rundown of both a positive and a negative voltage (Fig. G). The switch transitions are balanced and, at the same time, the final—most critical—zero crossing is made with a positive-going ramp. Note also that the number of ramps is limited to S_{-4}, S_{+4}, S_{-3}, S_{+2} and S_{-1}.

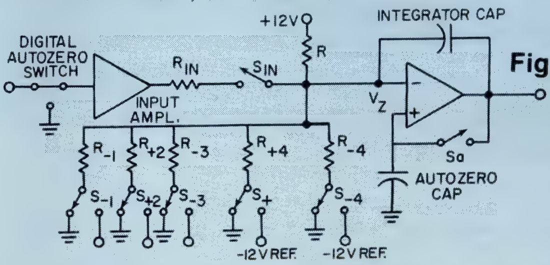
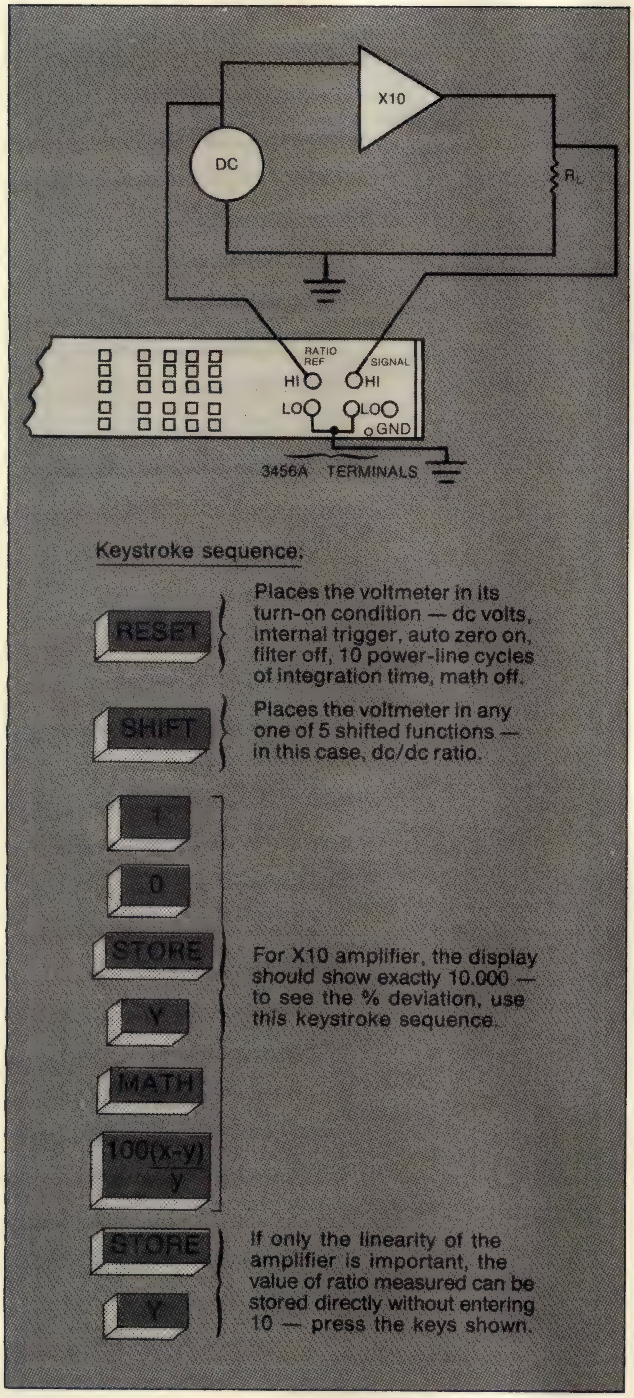


Fig. H

A more general view of the integrator is shown in Fig. H. Note that an R_{+4} and R_{-4} are required for the S_{+4} and S_{-4} slopes but that the remaining slopes needed for rundown require only three resistor-switch combinations.



Places the voltmeter in its turn-on condition — dc volts, internal trigger, auto zero on, filter off, 10 power-line cycles of integration time, math off.

Places the voltmeter in any one of 5 shifted functions — in this case, dc/dc ratio.

For X10 amplifier, the display should show exactly 10.000 — to see the % deviation, use this keystroke sequence.

If only the linearity of the amplifier is important, the value of ratio measured can be stored directly without entering 10 — press the keys shown.

5. Mathematics, the ability to form ratios, and excellent conversion linearity come together in this measurement aimed at pinning down the linearity of a dc amplifier. Deviations are displayed directly or as a percentage error.

Speed consideration is not the only reason for making autozero selectable. Because a shorting switch at the input of the DVM is required for digital autozero, troublesome glitches can appear while measurements are being made from a high-impedance source. Now, glitches can be eliminated by not switching the input.

Smart autoranging circuits work to keep the 3456A speedy. Autoranging is so fast, it's almost undetectable. In earlier instruments, autoranging occurred only after runup. In the 3456A, autorange aborts the runup cycles whenever the input exceeds the instrument's range setting. To perform the cutoff, comparators are set to the full-scale limits of the integrator input. When the limit is reached, a range-advance command is issued and the reading begins over again.

For downranging, the measurement cycle is completed and, when the reading drops to 1/100 of full scale, the ranging signal tells the instrument to drop two ranges. With signals greater than 1/100 of full scale, but less than 1/10, the instrument drops just one range. In this way, every effort is made to reach the correct range in the least amount of time.

Four applications show off the 3456A at its best. In the first, a standards lab calls on the stability of the 3456A to transfer the accuracy of precision fixed resistors, held at a constant temperature within 0.001 C, to decade-resistance standards to be used both in the R & D lab and on the production line. Features and modes needed include four-wire ohms, offset compensation, both 10 and 100 power-line-cycle (PLC) integration times, 6½ digits, and the null function (X-X_1, where X_1 is the first reading). The measurement requires 2-ppm transfer repeatability and must be fast enough for convenient adjustment response. Fig. 4 shows the test setup and the keystroke sequences.

The decade-resistance standard is set to the appropriate value and the terminal switch is set to the front terminals. The decade-resistance standard is adjusted until the display reads 0.000000. The integration time is now changed to check the adjustment value to 100 PLC.

The second application, measuring the linearity of a dc amplifier, calls on three features of the 3456A to accomplish the measurement objective: the basic linearity of its a/d converter, its dc/dc ratio capability and its math functions. This kind of application will most often be found in an R & D lab or in production testing. The basic test setup may be as shown in Fig. 5. The procedure given in the figure checks the amplifier's linearity over a 1 to 10-V range, and reads out deviations as a percentage error, or as a deviation from the measured ratio.

Another application, data acquisition, typically calls for measuring the output of transducers, whose signals are routed through a multiplexer to the voltmeter. The signals may require the use of ac, dc or ohms function, and both fast and slow measurement capability may be required—fast, to scan quickly all the channels connected to the voltmeter (to get a "snapshot" of the events); slow, to monitor long-term drift or a slowly changing signal.

In most cases, a computer orchestrates the sequence of measurements and relay closures. Because of the computer's speed, HPIB data-transfer rates may vary from milliseconds to microseconds. So, voltmeter and computer speeds should be independent of each other.

A typical data-acquisition sequence could run as follows:

1. Take 30 low-level (10 mV) ac measurements (2800 Hz) in 2 s.
2. Take ten low-level dc measurements (thermocouples), as fast as possible, with high NMR.
3. Take 20 thermistor (resistance) measurements at 300 readings/s and convert the readings to temperature at data transfer.

Signal multiplexers (such as the HP 3495A) can be sequentially advanced from one channel to the controller board. A command sequence to perform this application follows (the sequence assumes a judicious selection of channel conversion):

```
L1 F2 Z0 1STI D0 P1 30 STN .05 STD RS1 T3
F1 10 STN
0 STD T3 F3 R3 20 STN .01 ST1 T3 S01
P0 M5 −20 STR RE R
M0 −70 STR RER Q H X1
```

The sequence between L1 and Q is stored in the 3456A's built-in memory and is executed any time the 3456A receives an X1 command. A detailed look at the sequence is shown in Fig. 6.

A fourth application, production testing, calls on the 3456A both as a precision DVM and as a limited distributed-systems controller. Because of the DVM's memory, it can operate independently of the computer, leaving the computer free to perform many more operations. The keys to this application include program memory, reading store, front-panel SRQ, voltmeter-complete signal, and external trigger.

For example, the 3456A, in conjunction with a

Ranging in on ohms errors

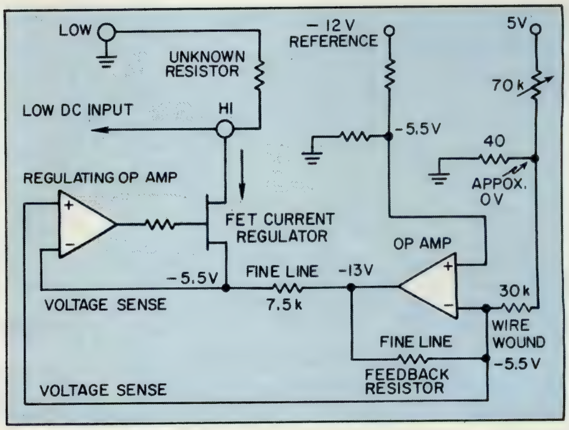
The ohms converter in the 3456A is designed to ensure accuracy while minimizing noise. To fight noise, the unit calls on a stable current source, instead of the combination current-voltage sources found in other converters. The current source is designed to be immune to the drift of the reference voltage.

To see how the converter works, look at the figure. At the op amp (on the right-hand side), a voltage divider made up of ratio-trimmed fine-line resistors produces −5.5 V from the −12-V reference. The lower leg of the op amp ties to ground through a 30-kΩ wirewound and a 40-Ω resistor. The 70-kΩ potentiometer makes slight corrections in the current injected to the op amp for calibration purposes. The feedback loop is arranged to produce −13 V at the op amp's output. If the reference voltage drifts, the current changes by the same amount as the voltage calibration of the a/d converter.

A second, regulating op amp drives a FET current regulator whose inputs can be viewed as voltage sense leads, one tied to −5.5 V at the feedback resistor and the other tied to the reference 7.5-kΩ resistor. To satisfy circuit conditions, the regulating op amp drives the FET so that −5.5 V appears at both of its inputs. This forces a well-regulated drop of −7.5 V across the 7.5-kΩ reference resistor, thus creating a solid 1-mA current source. Calibration is accomplished simply by adjusting the divider on the lower leg of the op amp.

Converter accuracy depends greatly on the ratio match between the fine-line resistors. Stability with temperature depends on the temperature (TC) tracking of these resistors. These in-house designed and produced Ta_2N resistors are ratio-matched to within 0.01% and TC tracking is held to 1 ppm/°C. The 30-kΩ wirewound resistor is also a critical element; its TC is also held to 1 ppm/°C. As a final source of error, the FET current regulator's leakage current is held to 3 pA.

The 1-mA current source works on the 100-Ω range. To make a more stable measurement, the current source is boosted to 50 μA, 5 μA and 500 nA on the 100-kΩ, 1-MΩ and 10-MΩ ranges. These ranges are created by switching-in other FET current regulators and adding, in series, other fine-line resistors to the 7.5 kΩ. Current is boosted by altering the voltage across the 7.5-kΩ reference resistor to 3.75 V instead of 7.5 V.



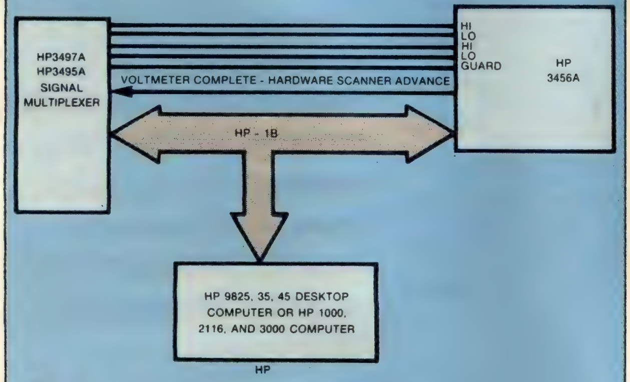

HP3497A
HP3495A
SIGNAL
MULTIPLEXER
VOLTMETER COMPLETE - HARDWARE SCANNER ADVANCE
HI
LO
HI
LO
GUARD
HP
3456A
HP - IB
HP 9825, 35, 45 DESKTOP COMPUTER OR HP 1000, 2116, AND 3000 COMPUTER
HP

Fig. 6

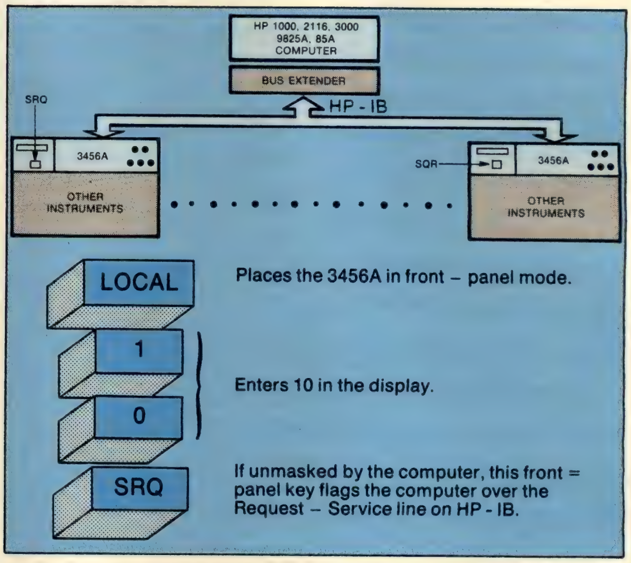
Command Sequence

L1 — Marks the beginning of the sequence to be stored in programming memory.
F2 — Selects ac.
Z0 — Turns autozero off.
First 1 STI — Selects 1 PLC integration time.
D0 — Turns the display off.
P1 — Turns the packed mode on.
30 STN — 30 readings are taken per trigger.
.05 STD — Stores 50 milliseconds between measurement cycles.
RS 1 — Turns readings stored on.
T3 — Gives the voltmeter a 5-cycle trigger.
F1 — Selects dc.
10 STN — 10 readings/trigger.
0 STD — 10 Seconds between measurement cylces.
T3 — Trigger the burst.
F3 — Selects 2 wire ohms.
R3 — Selects range 4 (10 wire ohms).
20 STN — 20 readings/trigger.
0.01 STI — 0.01 PLC integration time
T3 — Trigger the burst.
P0 — Packed off.
MS — Selects thermistor linearization.
-20 STR — Stores the location 20 in register R. The negation sign tells the voltmeter to scroll the data from the location selected to location one or until halted by the computer.
RE R — Recall R: Begins the scrolling process from location 20.
SO1 — System output on: Requires a handshake between readings to tranfer data from the voltmeter to the computer.
M0 — Turns the math off.
-70 STR — Tells the voltmeter to go to location 20 in memory and get ready to scroll data out.
RE R — Tells the voltmeter to begin scrolling.
Q — Marks the end of the sequences stored in program memory.
H — Software RESET
X 1 — Executes program memory.

6. Acquiring data is the 3456A's forte. To measure the output of multiplexed transducers requires both fast scanning and the ability to slow down to catch long-term drift. And the 3456A can work with a computer at top speed.

programmable source, can automatically test the linearity of a dc amplifier and flag the computer if out-of-tolerance measurements occur. This test or any others can be conducted in parallel at other test stations using the same computer. The keystroke sequences are shown in Fig. 7.

The computer goes to subroutine 10, transfers the measurement command sequence to the 3456A's built-in memory, and sets up the programmable source (for example, an HP 3325A function generator is set to a slow-ramp function). To begin the measurement sequence, the 3456A is triggered by the sync pulse from the function generator. The DVM measures the output of the amplifer and compares it on the dc/dc ratio function with the input from the 3325A. The 3456A's pass/fail-limit test compares the preprogrammed limits with the measurement and pulls SRQ upon failure. After checking 100 cardinal points in 20 s, the DVM tells the computer it is finished by flagging SRQ again and setting the status byte.

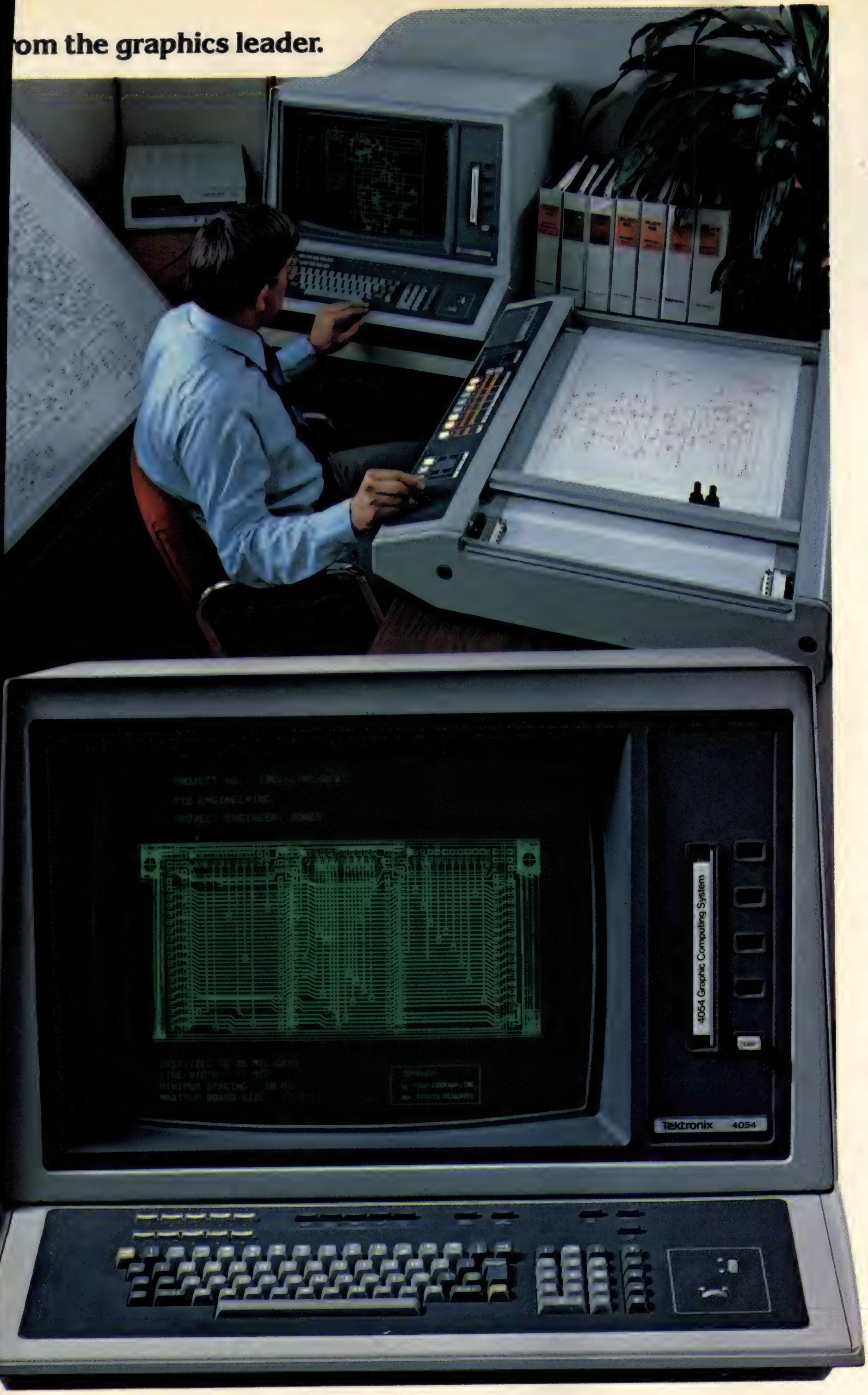

HP 1000, 2116, 3000
9825A, 85A
COMPUTER
BUS EXTENDER
HP - IB
SRQ
3456A
OTHER INSTRUMENTS
SQR
3456A
OTHER INSTRUMENTS
LOCAL
Places the 3456A in front – panel mode.
1
0
Enters 10 in the display.
SRQ
If unmasked by the computer, this front = panel key flags the computer over the Request – Service line on HP - IB.

7. Synergism with a computer system is accomplished with the front-panel SRQ button. The computer and the DMM operate at speed—without waiting for each other.

If the limits are 1% and the amplification is ten, subroutine 10 will contain the following:
L1 S1 100 STN T2 1 STI M1 10.1 STU 9.9 STL SM200 Q H SM002 X1
The subroutine also holds the commands for the programmable source.□

How useful?	**Circle No.**
Immediate design application	544
Within the next year	545
Not applicable	546

om the graphics leader.



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LED

Near IR Emission	930 nM
T_r	0.6 µS
High efficiency solution grown	
P_O	5 mW @ I_F = 100 mA
High pulse current	30 A

PHOTODIODE

T_r	5 nS
I_L	40 µA @ H = 5 mw/cm² V_R = 20V
Application	Linear, analog or hi-frequency

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PHOTOTRANSISTOR

T_r	5 µS
I_L	12mA @ H = 5 mw/cm² V_{CE} = 5V
V_{CE} (SAT)	0.2V @ I_C = .4 mA
Application	General Purpose Detectors

PHOTODARLINGTON

T_r	100 µS
I_L	6 mA @ H = 0.2 mw/cm² V_{CE} = 5V
V_{CE} (SAT)	1.1V @ I_C = 1 mA
Application	High current or high light sensitivity requirements

PHOTO IC

Schmitt Trigger Output	
T_r, T_f	50 nS
Output Sink	10 TTL loads @ $V_{CE} \leq .4V$
Propagation Delay	5 µS
T_{op}	−55 to +100°C
Application	Opto Switching

CIRCLE NO. 46

The Macrocell Array concept relies on sets of SSI and MSI functions, computer-aided design and high-density bipolar technology to create high-speed VLSI quickly and reliably.

Macrocell approach customizes fast VLSI

The MECL 10,000 Macrocell Array concept answers the problem of designing economical, yet high-speed, custom LSI. For a two-level, series-gated ECL design, typical delays are just 0.8 ns. Because the ICs are fabricated with a high-density bipolar process (see "Mosaic I—A New Process for High-Density Bipolar Circuits"), one chip can replace an entire circuit board containing approximately 50 IC packages. Other advantages accrue over discrete designs —reductions in cost, size and power consumption (up to 80% less power). With fewer electrical and mechanical components, a system also demonstrates better reliability.

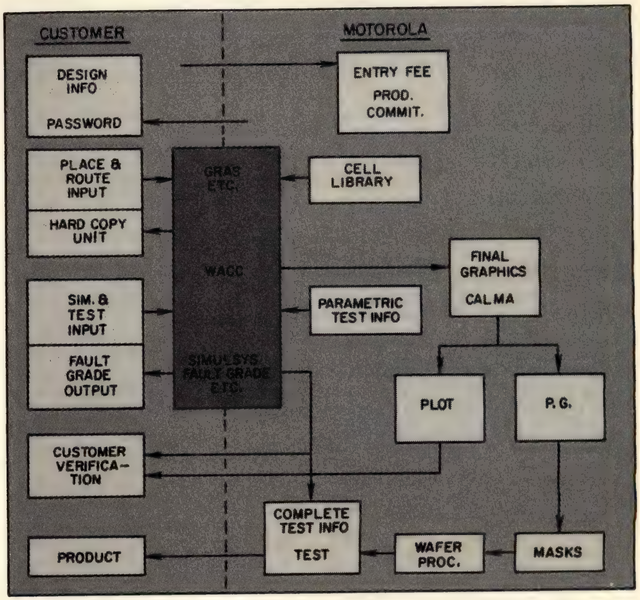
The Macrocell Array relies on a comprehensive set of SSI and MSI functions, called "macros." The metal interconnect pattern for each macro is stored in a time-shared, computer-aided design (CAD) library. More than 100 library macros are currently available. With the help of CAD, the macros are placed into the cells of a logic array; each cell contains transistors and resistors. The outputs and inputs interconnect on two layers. Because all designs are processed by the same procedure (up to the metal interconnect), custom designs can be turned around quickly (see "The Macrocell Array Concept").

The beauty of the Macrocell Array is that the logic designer can design systems with standard logic families—latches, flip flops, adders, decoders and multiplexers. The input-to-output delay for each path on the array is a known quantity calculated from Motorola specifications.

With discrete logic, the interconnect and fanout delays on a circuit board must be calculated for each case. Interconnect delays between chips are a major factor in speed degradation and run 2 to 3 ns per foot of line, depending on fanout. In the Macrocell Array, however, most interconnects are on-chip, rather than between chips; therefore, delays are minimized.

CAD speeds up circuit development

The designer obtains a finished product from the initial layout using computer-aided design. CAD greatly speeds up circuit development and simplifies communications between the designer and manufacturer (Fig. 1), since the designing takes place at the

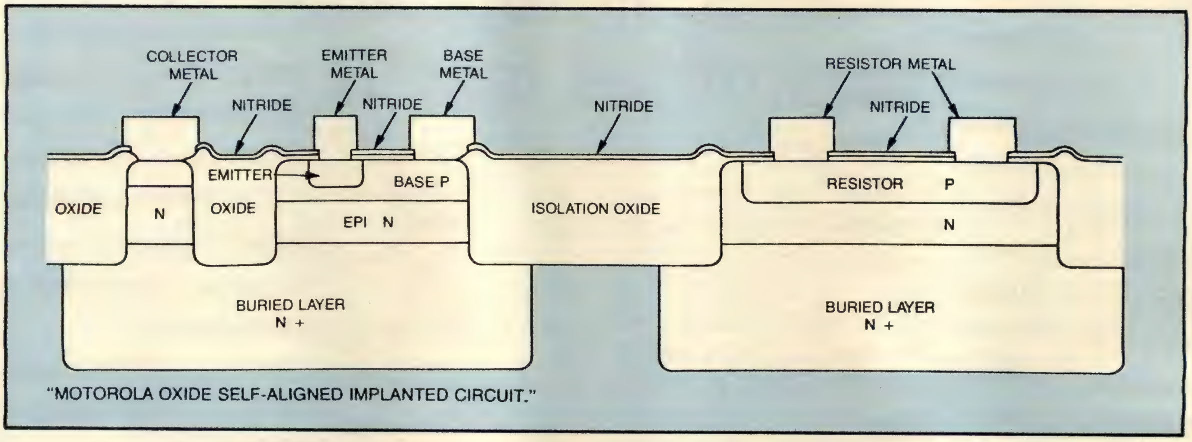


1. A closely-coupled interface between customer and IC manufacturer is essential in using computer-aided design to develop a Macrocell custom LSI circuit. Phone lines tie the designer to Motorola's in-house computer.

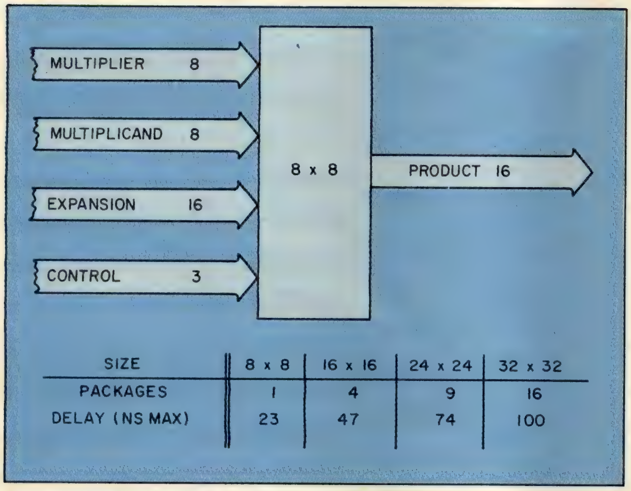
Jerry Prioste, Systems Engineer
Bipolar LSI and Memory Products
Motorola, Inc.
2200 W. Broadway Rd., Mesa, AZ 85202

MOSAIC I—a new process for high-density bipolar circuits

The MOSAIC I process couples a nonwalled emitter with a walled base (see Fig.). An isotropic etch produces oxide isolation between devices; the peaking of the oxide is controlled and monitored to guarantee flatness—a thickness of less than 4000 Å—during processing. The first layer of metal, 10,000 Å thick, covers the peaking of the oxide. A nitride surface then covers the oxide. *Thus*, the metal system is over nitride, a normal arrangement in MECL processes. The base and emitter diffusions are controlled by ion implantation to conventional junction depths. Among its other benefits, the oxide-isolated process achieves a high packing density and good yields.



"MOTOROLA OXIDE SELF-ALIGNED IMPLANTED CIRCUIT."



SIZE	8 x 8	16 x 16	24 x 24	32 x 32
PACKAGES	1	4	9	16
DELAY (NS MAX)	23	47	74	100

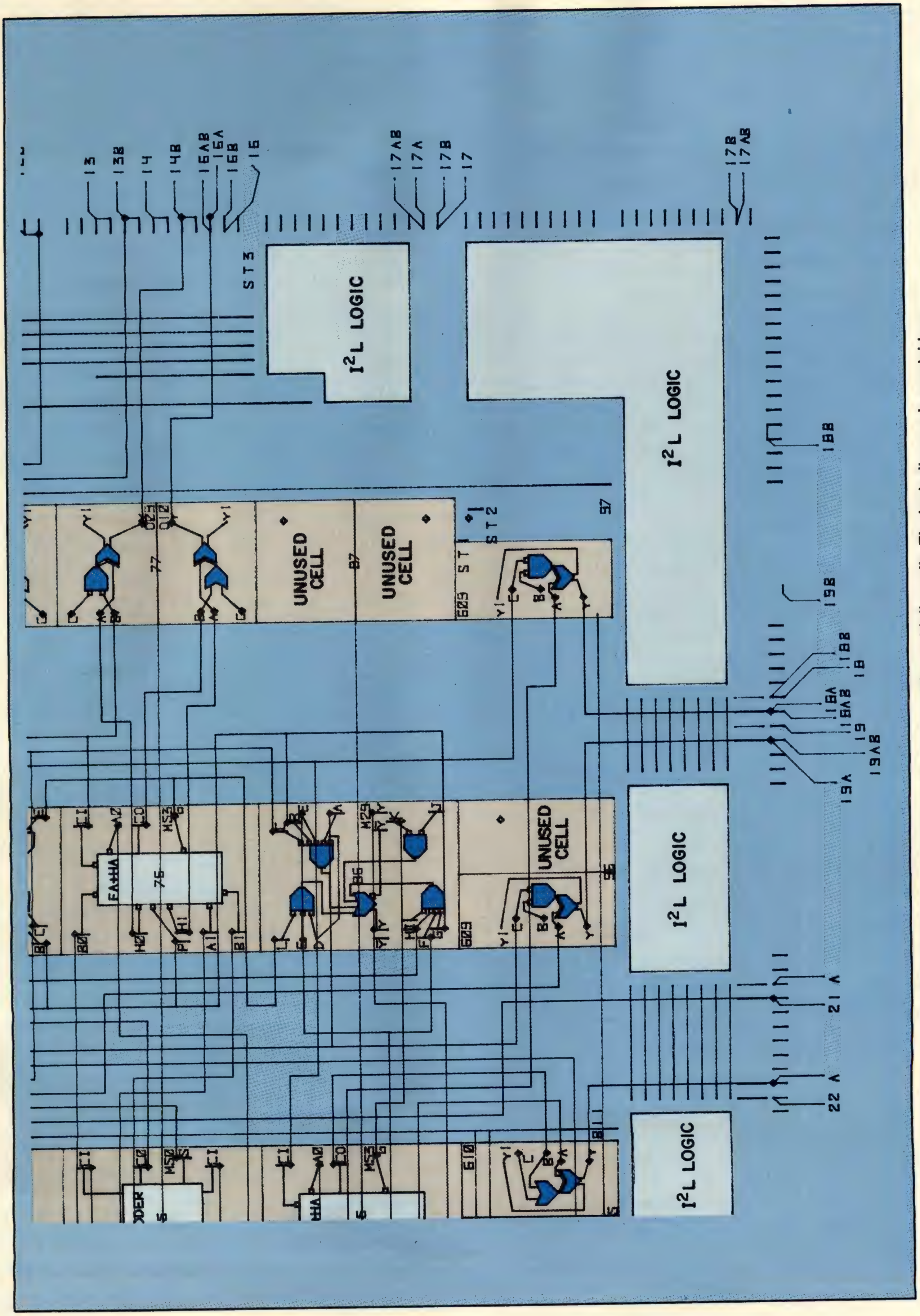
2. The design of an 8-by-8 array multiplier demonstrates the steps going into a Macrocell design. Speed is obtained by judicious partitioning of the cells.

customer's facility over phone lines to Motorola's computer center. The CAD interface provides:

- An interactive CRT display for macro placement and interconnection
- A plotter to generate the worksheet, showing the I/O ports of the placed macros, and to digitize the channel routing
- Software to simulate the logic design and verify the interconnects
- Documentation (plots) of the logic design and the metal interconnects
- Software for fault-grade analysis
- Conversions of test vectors generated during simulation to the format required by automatic test equipment for functional testing
- Conversions of the final interconnect into a format compatible with the production of metal masks.

In general, the design steps are as follows: First, the system is partitioned so that each option uses no more than 48 major cells, 32 interface cells and 26 output cells. The final logic design for each option must employ the macros in the Macrocell Library. A wire list of all interconnects is then entered into the CAD system, which simulates and analyzes the logic design. (If simulation is delayed until the layout is complete, the CAD system can generate the wire-list equations.)

Next, for determining the best macro placement,



3. A CAD plot shows a portion of the layout of the multiplier cells. The logic diagram is overlaid on each cell for clarity. Colors can be used to represent the various layers.

The Macrocell Array concept

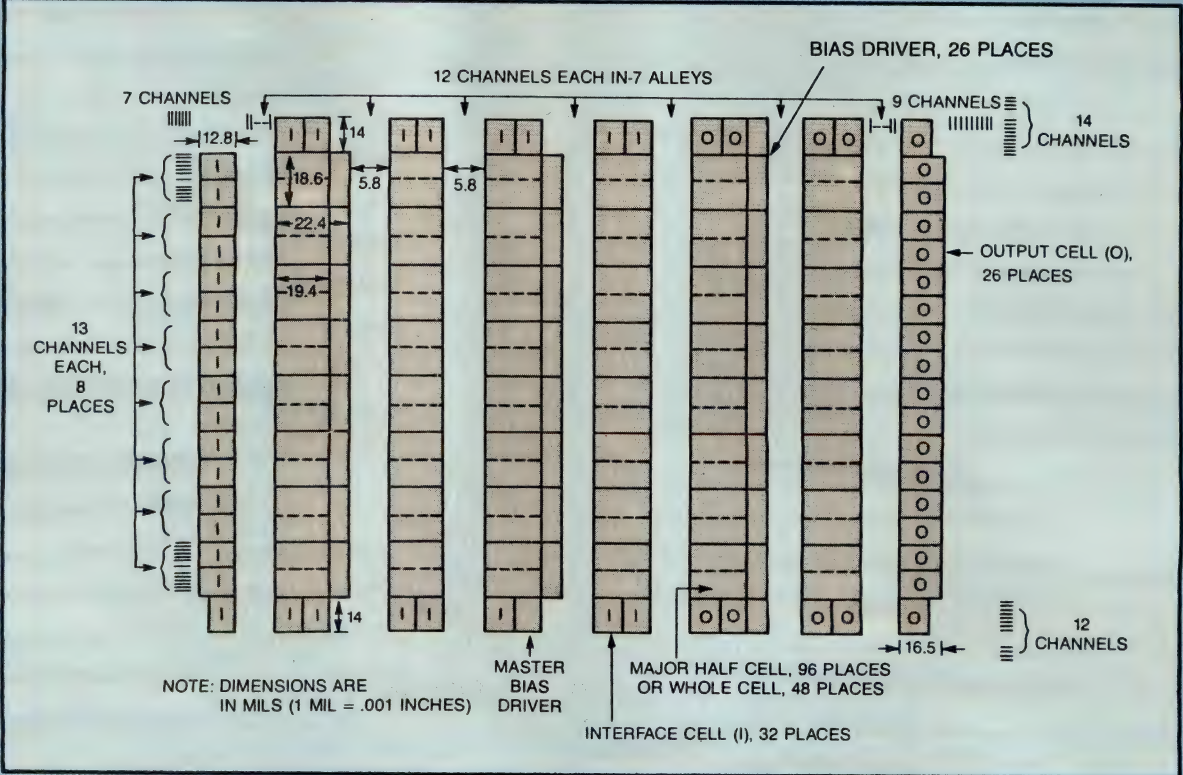
The MECL 10K Macrocell Array contains 48 whole or 96 half cells, 32 interface cells and 25 output cells (below). The interface and output cells provide extra logic power and interfacing between packages. The major cells provide most of the array's logic power. The many cells in the array make it possible to design custom circuits that are more complex than, say, the MC10800 series. For instance, 8-bit ALUs could be designed as easily as 4-bit ALUs.

The number of components for the three kinds of cells has been optimized with ECL series-gated circuit techniques to generate a comprehensive set of macros. The figure at the right shows series gating in the design of a 4-input, exclusive-OR gate using one-half of a major cell. If gates were used, then eight 4-input AND gates plus one 8-input OR gate would be needed. The gate equivalent for this function is nine gates dissipating only 15 mW (or 1.7 mW/gate), for a speed-power product of 3 picojoules. The user has a choice of three emitter-follower currents to maximize speed for fanout and metal length.

I^2L diagnostic and chip-control logic for the macrocell is optional. The option solves field-testing problems by letting the user monitor 39 internal signals; assign a 9-bit part number during the layout and monitor it electrically after the chips are packaged; load eight latches externally (the latch outputs control internal functions within the ECL array); and operate three independent reset signals externally, to initialize or control functions in the ECL array.

Macrocell CAD library functions

Half-cell major macros	Whole-cell major macros
D flip-flop Dual latch Dual exclusive OR Dual, 2 to 1 MUX Full adder 4-input exclusive OR Various OR, NOR, AND, NAND functions	Fast full adder Lookahead carry functions 4-bit group generate and propagate 4 to 1 MUX with enable 1 to 4 decoder with enable Priority encoder Priority expander Various gate functions
Interface-cell macros	**Output-cell macros**
2 to 1 MUX D input latch Dual OR, NOR, AND, NAND gates Exclusive OR/NOR Differential receiver (being evaluated) TTL to ECL translator (being evaluated)	2 to 1 MUX with enable D input latch Various OR, NOR, AND, NAND gates Exclusive OR/NOR 25-Ω bus transceiver ECL to TTL translator (being evaluated)


BIAS DRIVER, 26 PLACES
12 CHANNELS EACH IN 7 ALLEYS
7 CHANNELS
9 CHANNELS
14 CHANNELS
12.8
14
18.6
5.8
5.8
22.4
19.4
13 CHANNELS EACH, 8 PLACES
OUTPUT CELL (O), 26 PLACES
14
16.5
12 CHANNELS
NOTE: DIMENSIONS ARE IN MILS (1 MIL = .001 INCHES)
MASTER BIAS DRIVER
MAJOR HALF CELL, 96 PLACES OR WHOLE CELL, 48 PLACES
INTERFACE CELL (I), 32 PLACES

a layout worksheet is generated manually or by the CAD system to show the macro I/O ports and available channels for interconnect.

The macro I/O ports are interconnected, as indicated by the logic drawing, using the available channels on the worksheet. Then, this routing is entered into the CAD system. If the CAD generated the worksheet, the plotter digitizes the channel routing. If the user generated the worksheet, the routing is entered via the CRT display, using the cursor controls; a logic simulation verifies that the routing connects the logic correctly. A fault-grading program is also available, to help generate the test sequence.

When the design is finished, the information in the CAD system is transferred to Motorola for mask generation. Within 12 weeks, the customer receives ten functional parts.

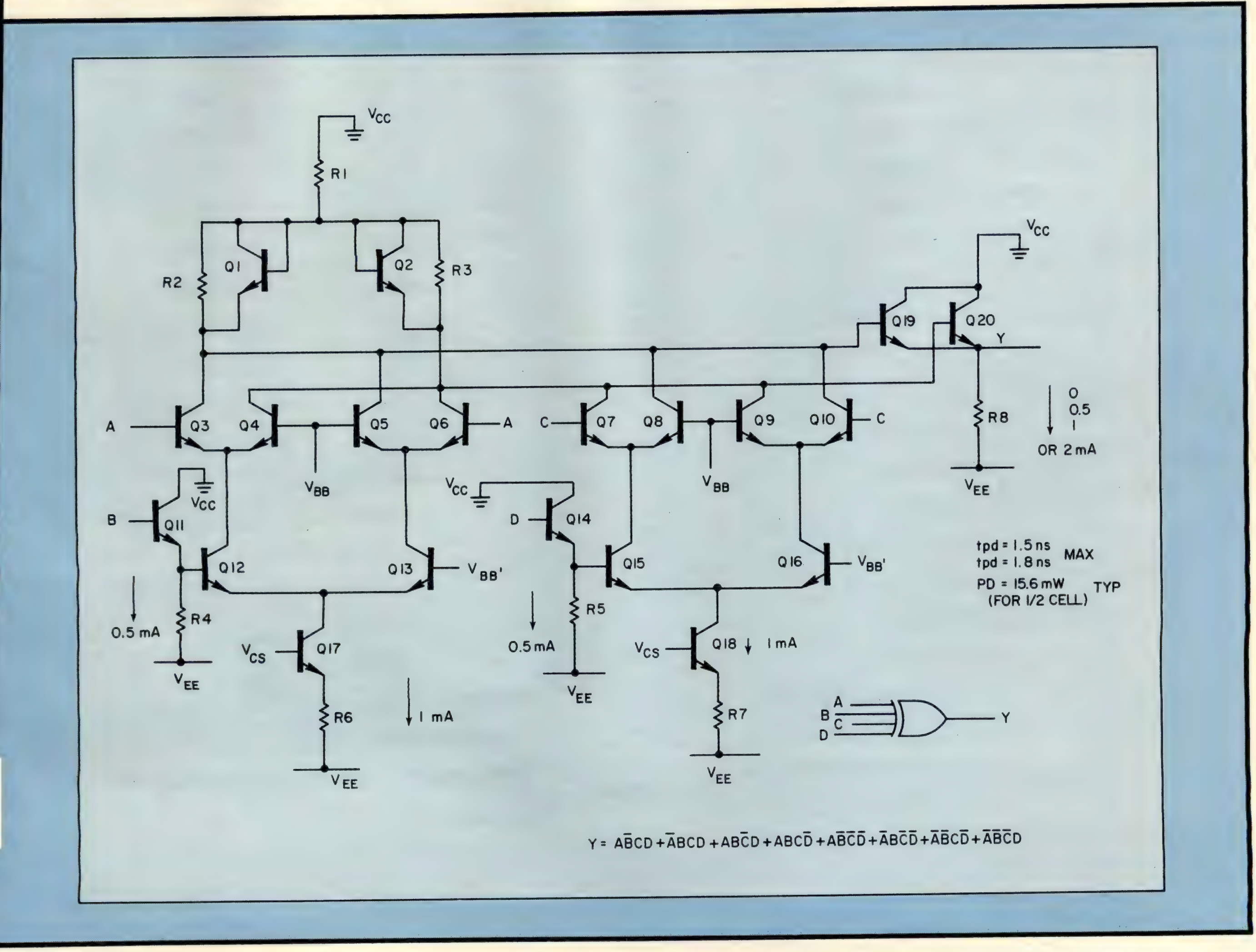
CAD designs a multiplier

The flexibility and usefulness of the CAD system is best illustrated with a practical design; for example, an 8 × 8 two's-complement multiplier (Fig. 2). The multiplier is partitioned to achieve the fastest speed possible using a majority of the cells in the array. The logic design calls for 48 major cells, 26 internal cells and 16 output cells.

Fig. 3 shows a CAD plot of the lower right corner of the multiplier layout (one-ninth of the array); the logic drawing is also plotted in the cell locations for the selected macros. The output cells are shown along the right column and bottom row; the major cells are elsewhere. I^{2}L logic—used for diagnostics—is shown in boxes between the cells and the periphery of the array. The plot is easier to read if different colors are selected for different layers.

The short horizontal lines on the right edge of the array indicate the horizontal channels (second metal) available for routing. The numbers along the right and bottom indicate where package pins can be picked up for routing to internal logic. The A and B symbols next to the numbers indicate the base of an output emitter follower.

The Y output of an output macro must connect to the base of an output emitter follower. The symbol AB next to a pin number indicates that the pin can



$$Y = A\bar{B}CD + \bar{A}BCD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D$$

Wire List

```
BP33    =91A-B   ,71A-B2  ,21A-B2  ,42B-B2  ,43B-B2  ,73B-B2  ,73A-B2  ,53B-B2  .
BP34    =20A-A   ,30B-B   ,50A-A   ,60B-A   ,70A-A   ,80B-A   ,90A-A   ,92A-D   ,92B-B  ,
         94A-D   .
BP35    =91A-A   ,91B-A   ,92A-C   ,92B-A   ,94A-A   ,40A-A   ,40B-A   ,50B-A   ,70B-A  .
         80A-A   .
BP36    =90A-B   ,20B-A   ,30A-C   ,31B-B1  ,60A-A   ,71B-B2  ,62A-B1  ,73B-B1  .
BP37    =80B-B   ,10A-B   ,30A-A   ,31A-A1  ,31A-A1  ,51B-B1  ,52B-B2  ,73A-B1  ,63A-B1 .
```

4. After the layout is finished, the computer-aided design system automatically generates a wire list showing all bonding pad (BP) to cell interconnections. A partial listing is shown for the 8 × 8 multiplier.

Total number of equivalent gates	Top half of array: Number used and macro type	Top half of array: Macro function	Total macro power (mW)
48	3-M53	2-bit adder	93.6
55	5-M50	Fast full adder	143
7	1-M28	Carry lookahead	23.4
36	3-M54	Dual half-adder	46.8
240	12-M52	Dual adder	499.2
20	5-I11	Exclusive OR/NOR	52.0
10	5-I01	Dual OR gate	52
8	2-O09	Exclusive NOR	57.2
20	5-O10	Exclusive OR	143
444	Totals		1110.2

Output follower power = (102) (5.2)
= 530.4 mW
Total power for top half of
The array (from pin 60) = 1110.2 + 530.4
= 1640.6 mW

Top half of array has 5.7% less power than the bottom half

Total number of equivalent gates	Bottom half of array: Number used and macro type	Bottom half of array: Macro function	Total macro power (mW)
64	4-M53	2-bit adder	124.8
55	5-M50	Fast full adder	143
7	1-M28	Carry lookahead	23.4
10	2-M29	Carry lookahead	46.8
36	3-M54	Dual half-adder	46.8
180	9-M52	Dual adder	374.4
44	11-I11	Exclusive OR/NOR	114.4
4	2-I01	Dual OR gate	20.8
2	I-I03	Dual AND gate	18.2
2	1-I04	Dual NAND gate	18.2
1	1-I08	3 Input OR/NOR	5.2
16	4-O09	Exclusive NOR	114.4
20	5-O10	Exclusive OR	143
441	Totals		1193.4

Output follower power = (105) (5.2)
= 546 mW
Total power for bottom half of
the array (from pin 26) = 1193.4 + 546
= 1739.4 mW

Total output emitter follower
power from output cells = (16 outputs) (15 mW/output) = 240 mW
Total bias driver power = 327 mW
Total chip power = 327 + 240 + 1640.6 + 1739.4 = 3.95 W
Total gate equilvalent = 444 + 441 + 3 = 888 gates
(the 3 gates are for wire ORs in logic)
Power per equivalent gate = 4.45 mW/gate
Chip utilization = $\frac{232.5}{250} \times 100\% = 93\%$

5. The power dissipation of the multiplier design is calculated separately for the top and bottom halves of the array. Dissipation from the upper half should be within 10% of that from the lower half.

connect to the bases of two output emitter followers. This connection is made whenever the driver from an output cell must drive a 25-Ω load, instead of 50-Ω load.

A connection to a macro I/O port is shown with a diamond-shaped symbol called a via. To save plotting time, vias are not illustrated in the channel area unless two connected lines cross.

Before committing his project further to the CAD system and the Macrocell Array, the system designer can refer to a preliminary design manual (provided by Motorola) that analyzes the alternatives and the resulting performance, power and cost. If the CAD system is chosen, the next step is to determine the best logic placement for shortest wire lengths.

As the macros are placed on the worksheet, the logic diagram should be labeled with the cell location, so that similar macros can be distinguished. From the logic diagram, a wire list of all the interconnections can be written. The designer can refer to these equations, instead of the logic diagram, when connecting the macro I/O ports on the available channels of the worksheet.

After the equations have been written, they are entered into the CAD system for simulating the logic, either at once or after the layout is completed. The CAD system then generates the wire list automatically from the completed layout.

Fig. 4 shows a portion of the wire list printout. The first line states that bonding pad 33 (BP33) connects (=) to the B2 input of cell location 71A (71A-B2), the B2 input of cell 21A, the B2 input of cell 42B, and so forth.

After all the macros are placed, either of two interconnection methods will work. The first uses a "C"-sized printed-layout worksheet. The I/O ports are placed in the proper cell and channel locations with sticky-backed paper (available from Motorola). The I/O ports are then interconnected using the wire list equations or the logic diagram or both. The CRT terminal enters the layout interconnections into the system.

In the second method, a plotter generates the layout worksheet along with the I/O ports of the selected macros. The I/O ports are then connected on the available channels, according to the logic diagram. The routing lines are traced over with a plotting pen; and the plotter digitizes the information into the system. When all the lines are inked, the digitizing is complete. This method appears to produce less errors.

Some of the CAD commands are listed in Table 1. Placement commands enter and modify selected macros in the array; routing commands enter and modify the wiring between I/O ports, by means of the CRT or the digitizing plotter. Scaling commands

Table 1. Some of the CAD commands

Placement	
M	Define Macro name
P	Place Macro (if half cell, both halves placed)
H	Place half-Macro
I	Identify Macro name or placement
A	Delete placement (identify first)
G	Modify port or pad (see next page)
Routing	
T	Beginning or ending of routing
Space	Intermediate routing point (change direction)
Z	Digitize routing (up to 200 points)
R	Remove routing segment (to end or via)
E	Remove a via
N	Identify a net
F	Display the net identified
C	Clear routing
Displayed layers	
1. OL	Macro outline layer
2. RT	Routing layer
3. RC	Routing channels
4. NM	Macro names at placements
5. GN	Placement position names
6. IO	Macro I/O connection ports
7. LD	Logic diagram
8. BP	Bonding pads and chip outline
9. OB	Obstruction layer
10. MC	Macro name list

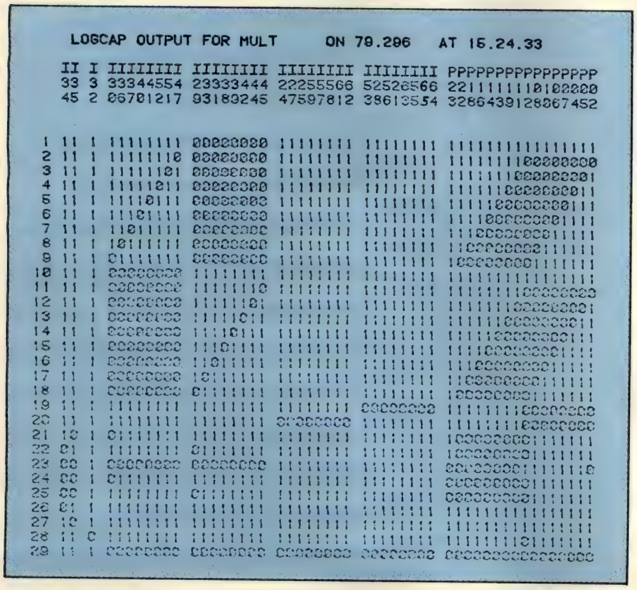
Table 2. Violation list commands

Enter	Response
B	To go back to the Array
Q	To quit session
P	For unused ports
C	For a list of modified follower currents
V	For unnecessary vias
N	For net errors
W	For the wire list
R	To remove unused ports
D	To delete unnecessary vias
S	To set plot flag to plot listings
M	To display this menu
L	For list of via spacing violations
I	To list input pads with load resistors
T	For untied ports of the same name and macro

select the viewing area of the design—ten layers can be shown independently and plotted in various colors. In Fig. 3, layers 1, 5, 6 and 8 can be plotted in one color, layers 3 and 7 in another, and layer 2 in a third color.

After the wiring information has been entered into the system, possible violations are listed (Table 2). A list of unused ports checks the wire list for agreement with the logic drawing.

The emitter-follower current of internal array outputs is selectable—0.5, 1 or 2 mA. The CAD system automatically selects 1 mA for outputs that are connected, and 0 mA for unused outputs. High fanout demands 2 mA; lower power, 0.5 mA. Fig. 5 shows the power dissipation of the top and bottom halves of the array. Two V_{CC} buses distribute the power, which must be balanced within 10%; the CAD system calculates the power of the top and bottom halves to establish this balance.



```
     LOGCAP OUTPUT FOR MULT       ON 78.286    AT 15.24.33

    II I IIIIIIII IIIIIIII IIIIIIII IIIIIIII PPPPPPPPPPPPPPPP
    33 3 33344554 23333444 22255566 52526566 2211111110100000
    45 2 06701217 93180245 47597812 38613554 3286439128067452


  1 11 1 11111111 00000000 11111111 11111111 1111111111111111
  2 11 1 11111110 00000000 11111111 11111111 1111111100000000
  3 11 1 11111101 00000000 11111111 11111111 1111111000000001
  4 11 1 11111011 00000000 11111111 11111111 1111110000000011
  5 11 1 11110111 00000000 11111111 11111111 1111100000000111
  6 11 1 11101111 00000000 11111111 11111111 1111000000001111
  7 11 1 11011111 00000000 11111111 11111111 1110000000011111
  8 11 1 10111111 00000000 11111111 11111111 1100000000111111
  9 11 1 01111111 00000000 11111111 11111111 1000000001111111
 10 11 1 00000000 11111111 11111111 11111111 1111111111111111
 11 11 1 00000000 11111110 11111111 11111111 1111111100000000
 12 11 1 00000000 11111101 11111111 11111111 1111111000000001
 13 11 1 00000000 11111011 11111111 11111111 1111110000000011
 14 11 1 00000000 11110111 11111111 11111111 1111100000000111
 15 11 1 00000000 11101111 11111111 11111111 1111000000001111
 16 11 1 00000000 11011111 11111111 11111111 1110000000011111
 17 11 1 00000000 10111111 11111111 11111111 1100000000111111
 18 11 1 00000000 01111111 11111111 11111111 1000000001111111
 19 11 1 11111111 11111111 11111111 00000000 1111111100000000
 20 11 1 11111111 11111111 00000000 11111111 1111111100000000
 21 10 1 01111111 11111111 11111111 11111111 1000000001111111
 22 01 1 11111111 01111111 11111111 11111111 1000000001111111
 23 00 1 00000000 00000000 11111111 11111111 0000000001111110
 24 00 1 01111111 11111111 11111111 11111111 0000000001111111
 25 00 1 11111111 01111111 11111111 11111111 0000000001111111
 26 01 1 11111111 11111111 11111111 11111111 1111111111111111
 27 10 1 11111111 11111111 11111111 11111111 1111111111111111
 28 11 0 11111111 11111111 11111111 11111111 1111111101111111
 29 11 1 00000000 00000000 00000000 00000000 0000000000000000
```

6. To check each logic element, a simulation test sequence called Logcap runs a truth-table test to compare actual and anticipated outputs.

Path	Total Macro Delay (ns)	Fanout Degradation (ns)	Metal Degradation (ns)	Input Follower delay (ns)	Worst case Total delay (ns)
11 MACROS (X0 to $\overline{P14}$)	21.4	0.12	0.588	0.3	22.4

7. Calculation of the longest delay path in the multiplier shows that metal degradation contributes only 2.6% of the total delay.

Next, the user works with the logic drawing and truth tables to generate a test sequence that checks the input and output of each logic element. The tables are keyed into the CAD system. A simulation program, called Logcap, operates on the truth table and interconnected macros to generate output data, which can be compared with expected outputs.

Fig. 6 is an example of the simulation program. The input pins are labeled with an I; the output pins, with a P. The first two inputs control two's complement, or sign, magnitude; input I32 covers sign-bit expansion; I30 to I47 are the X7 through X0 data inputs; I29 to I45 are the Y7 through Y0 data inputs; I24 to I62 are the M7 through M0 expansion inputs; I53 to I64 are the K7 through K0 expansion inputs, and P23 to P02 form the multiplication result (MSB to LSB).

As shown in Fig. 6, inputs and outputs can be printed in any order. Only 29 vectors are needed for functional tests of the multiplier. A timing diagram and plot of the input vectors lets the designer visualize the results more clearly.

Manual calculation of the worst-case path (Fig. 7) accounts for the various delays caused by metal degradation. Because of the low capacitance of the metal and the low-impedance drive of the emitter followers, metal delay contributes only 2.6% of the total delay.

The Logcap program can fault-grade the test sequence. The program holds every node sequentially at a ONE or a ZERO and then compares the results from good and bad networks. The number of faults detected by the input vector sequence, divided by the total number of faults, is displayed at the test-sequence efficiency. The nodes not detected are listed so that additional test vectors can be added, to increase testing efficiency. Ideal efficiency is 100%.

In the future, additional software and hardware, plus a second-source agreement with National Semiconductor, will enhance the Macrocell design, bringing automatic placement, routing and test generation and higher performance LSI.□

How useful?	**Circle No.**
Immediate design application	**547**
Within the next year	**548**
Not applicable	**549**

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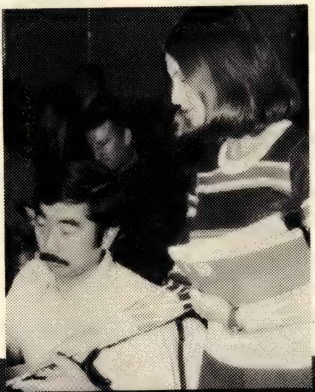

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MONDAY/LINEAR I

Three New Linear Families. New video SOS a/d flash converters, CA3179 1.3-GHz prescaler, divide-by-4 prescaler and precision BIMOS op amps are introduced. Hal Wittlinger, RCA, Somerville, N.J.

ICL7650 Glitchless Chopper-Stabilized Amplifier. Offers low offset voltage and exceptionally low input bias current at a very attractive price. Skip Osgood, Intersil, Cupertino, CA.

Am6300 Power-Supply-Control Subsystem. Computer-controlled, power-supply controller for sophisticated power-supply systems. Brian Gillings, Advanced Micro Devices, Sunnyvale, CA.

National's New Developments. A look at new low-power references, high-power regulators, and precision op amps coming from National Semiconductor.

DG211 4-Channel Switch. Fits a variety of low-cost applications. Jerry Mandel, Tom Cate. Siliconix, Santa Clara, CA.

CMOS Voltage Regulators, References and Voltage Detectors. Micropower devices covered include two-terminal voltage references, positive and negative programmable regulators and over-and-under voltage detectors. Jerry Zis, Intersil, Cupertino, CA.

New Voltage/Frequency Converter Techniques. New techniques lead to 18-bit a/d conversion with 1 ppm/°C gain stability. A 1.3-V (single-cell) supply circuit is also discussed. Bob Pease, National Semiconductor, Santa Clara, CA.

Analog/Digital LSI Design With I^2L Gate Arrays. A cost-effective approach. Bill O'Neil, Exar, Sunnyvale, CA.

RM4200 Analog Multiplier. Applications for a precision monolithic multiplier/divider are covered. Jim Schmoock, Raytheon Semiconductor, Mountain View, CA.

TUESDAY/LINEAR II

The HI5900 and HI5712: A Complete Microprocessor-Compatible System. An analog signal-processing front end and a 12-bit a/d converter form a high-speed, high-performance data-acquisition system. Al Morton and Rich Antalik, Harris Semiconductor, Melbourne, FL.

New Texas Instruments' Op Amps and Interface Circuits. Discusses single-supply, n-channel, FET-input op amps, comparators, new EIA RS-422 line circuits and 3-A peripheral drivers. Dale Pippenger, Texas Instruments, Dallas, TX.

BUF-03: Industry's Fastest Voltage-Follower Amplifier. Boasts a 300-V/µs slew rate and 55-MHz bandwidth. Two applications are described. With an OP-16, it forms a current booster capable of driving heavy capacitive loads; with a 500-pF holding capacitor, it functions as a fast sample-and-hold amplifier. Shelby Givens, Precision Monolithics, Santa Clara, CA.

9708 8-Bit, 6-Channel A/D Converter and 9706 12-Bit 8-Channel D/A Converter. Use in microprocessor-based control systems described. John Conover, Fairchild Semiconductor, Mountain View, CA.

OP-220 Dual Micro-Power Op Amp. Industry's first low-power, high-precision dual op amp. Lowest input offset voltage, lowest bias current over temperature, and lowest input-offset-voltage temperature coefficient of any dual amplifier. CMVR includes ground which makes this device ideal for light, compact battery-operated instrumentation. Tom Schwartz, Precision Monolithics, Santa Clara, CA.

Microprocessor-Compatible Conversion ICs. Discussion of new a/d and d/a converters and sample-and-hold amplifiers. Steve Sockolov and Phil Marcoux. Signetics, Sunnyvale, CA.

New Motorola Industrial ICs. Describes IC drive system for stepper motors. Speakers to be announced. Motorola, Phoenix, AZ.

Monolithic ICs for FSK Modem Design. A two-chip FSK modem design. Joel Silverman, Exar, Sunnyvale, CA.

Power Interface Circuits. Introduces UDN-2949Z bipolar half-bridge motor driver and UCN-4202A stepper motor translator/driver. Paul Emerald, Sprague, Worcester, MA.

WEDNESDAY/MICROPROCESSORS I

Microcomputers From Intel in the 1980s. Integrating software into silicon; simplifying the interface to the user. Dane Elliot, Intel, Santa Clara, CA.

Introduction to Signal-Processor ICs. Features, architecture and instruction set described. Bob Holm, Intel, Santa Clara, CA.

The Intel 2920 Signal Processor. A discussion of 2920 applications. Bob Holm, Intel, Santa Clara, CA.

Microcontrollers: System-Designed

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Microcomputers. New signal processors and microprocessors. Dick Barck, American Microsystems, Cupertino, CA. Santa Clara, CA.

The S68045 CRT controller. Reduces CRT system cost design. Frank Toth, American Microsystems, Santa Clara, CA.

Motorola's New Family of CMOS Microprocessors. Five new CMOS ICs with a/d converter, RAM, ROM and EPROM on the chips. Jim Farrell, Motorola, Austin, TX.

Fast Error Detection and Correction for Memory Systems. Use of AM2960 16-bit EDC IC is described. John Mick, Advanced Micro Devices, Sunnyvale, CA.

MB1412A 8-bit-slice ECC IC. Use of error-checking-and-correction chip described. Alan Heimlich, Fujitsu Microelectronics, Sunnyvale, CA.

THURSDAY/MICROPROCESSOR II

The NS16000 Family: Support for Software Modularity. NS16000 architecture eliminates the need to modify machine code. Linking process *illustrated*. Brian Marley, National Semiconductor, Santa Clara, CA.

Software Solutions for Board Applications. The software exists to design your next microprocessor-based board product. Joanne Pearson, Intel, Santa Clara, CA.

Transparent Addressing Resolves Memory Contention in Terminal Application. SY6545 allows addressing of screen-refresh memory transparent to processor to improve overall design efficiency. Conrad Boisvert, Synertek, Santa Clara, CA.

Mask-Programmable Low-Power-Schottky Gate Array. Shrinking system design. Cliff Vaughan, Raytheon Semiconductor, Mountain View, CA.

2653 Polynomial Generator Checker. Performs block/check character and parity generation, checking, single-character detection and two-character sequence detection. Alex Goldberger, Signetics, Sunnyvale, CA.

Bipolar Arithmetic Devices Support New MOS Microprocessor. Multiplier/divider enhances performance of otherwise slow MOS microprocessor. Shlomo Waser, Monolithic Memories, Sunnyvale, CA.

NE5560 Switched-Mode Power-Supply Control Circuit. For flyback forward or double forward (push-pull) outputs, provides all control interfacing needed. Norm Matzen, Signetics, Sunnyvale, CA.

Leadless Carrier Memory Arrays. Describes applications techniques. Charles Hochstedler and Jeff Wilkinson, Harris Semiconductor, Melbourne, FL.

FRIDAY/MICROPROCESSOR III

Single-Chip Fairchild Microcomputers. Describes applications for currently available F3870 devices and explores the use of tomorrow's multiple-function-on-a chip ICs. Jim Lang, Fairchild Semiconductor, So. San Jose, CA.

NSC800 In Low-Power Systems. Uses new high-density CMOS process called P²CMOS. An 8-bit CPU and supporting components are covered. Keith Winter, National Semiconductor, Santa Clara, CA.

Design and Use of Mostek PROM Programming Unit. Applies MK3873 single-chip microcomputer. Don Folkes, Mostek, Carrollton, TX.

The CONCEPT-48 Development Tool. Single-board system for 80C48 family. Gopal Ramachandran, Intersil, Cupertino, CA.

Z80 As a Versatile Communications Device. Z80 FIO as used in BiSync, HDLC, and SDLC communications protocols. James Booth, Mostek, Carrollton, TX.

PALs Replace Random Logic in Microprocessor Designs. Use of PAL series 20 to replace 7400 series MSI/LSI devices in microprocessor applications. Saeed Kahmi, Monolithic Memories, Sunnyvale, CA.

NS16000 Supports Virtual Memory. Virtual memory, a mainframe concept in the past, is applicable to microprocessor-based designs thanks to the 16000 microprocessor. Su Bhash Dal, National Semiconductor, Santa Clara, CA.

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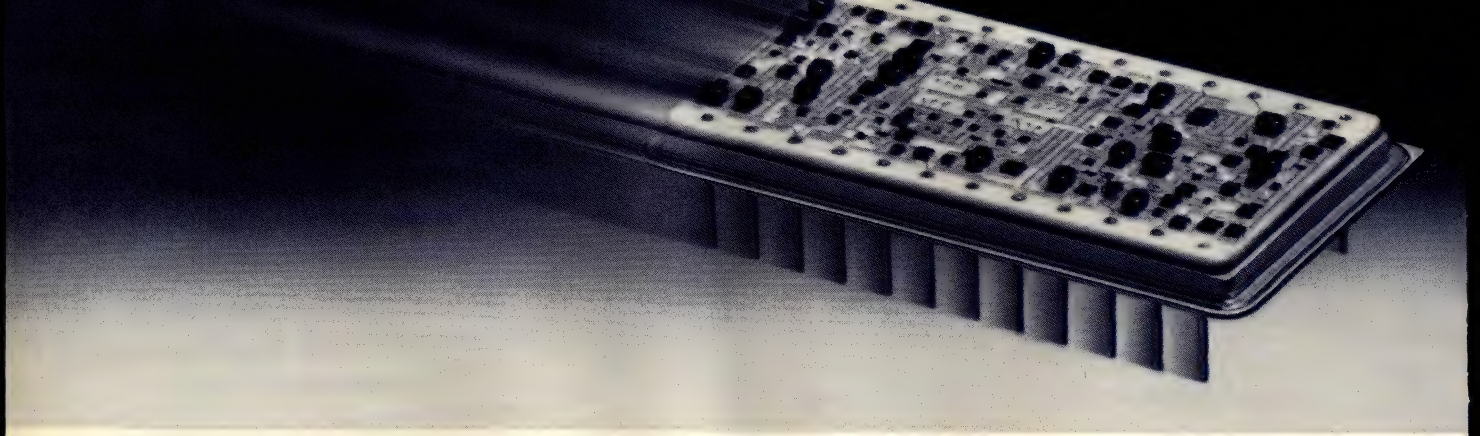

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CIRCLE NO. 47

The general, floating-point and special-purpose registers, addressing modes and instructions of the 16000 processor demonstrate its aptitude for high-level languages and large-scale computations.

Architecture of 16-bit micro underpins VLSI computing

The architecture of the 16000, a VLSI processor family that provides the capabilities of a large-scale computer, encourages efficient programming in high-level languages. Symmetric with respect to memory and register usage, as well as operand length, the 16000 architecture encompasses a full 32-bit virtual memory with a 16-Mbyte uniform address space, employs over 30 registers and handles high-performance floating-point computations. A single instruction can load or store a field of 1 to 32 bits anywhere in memory or in a register.

(For an overview of the 16000 processor family, see ELECTRONIC DESIGN, Jan. 18, 1980, p. 66. For more about the floating-point slave processor, see ELECTRONIC DESIGN, March 1, 1980, p. 77.)

The 16000 and Pascal—a good matchup

Compilers can easily generate compact high-performance code for the 16000. Its architecture avoids special-case instructions and addressing modes that compilers cannot use. The 16000 is particularly well suited to the Pascal high-level language. In fact, a compiler can generate a Pascal program for the 16000 that is smaller than the equivalent program for a stack-oriented P-code interpretive machine. Because of the 16000's general-purpose registers, the program also executes faster.

The paged virtual memory of the 16000 is as powerful as any available on a large computer. A VLSI chip in the 16000 family uses a content-addressable cache memory to translate the most recent virtual addresses. With the memory-to-memory architecture, every basic instruction can use an

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Table 1. Registers

```
          General registers
 ------------------------------------
|---------------r0-----------------|
|---------------r1-----------------|
|---------------r2-----------------|
|---------------r3-----------------|
|---------------r4-----------------|
|---------------r5-----------------|
|---------------r6-----------------|
|---------------r7-----------------|
 31                                0

       Floating point registers
 ------------------------------------
|---------------f0-----------------|
|---------------f1-----------------|
|---------------f2-----------------|
|---------------f3-----------------|
|---------------f4-----------------|
|---------------f5-----------------|
|---------------f6-----------------|
|---------------f7-----------------|
 31                                0

      Special purpose registers
 ------------------------------------
|---------------fp-----------------|
|---------------sb-----------------|
|---------------pc-----------------|
|---------------us-----------------|
|---------------is-----------------|
|---------------intbase------------|
|---------------ptb1---------------|
|---------------ptb2---------------|
|---------------error--------------|
|---------------fsr----------------|
|---------------msr----------------|
|-----psr-------|--------mod-------|
 31                                0
```

addressing mode for any operand—that is, instructions do not require that a register always contain one special operand. This flexibility eases a critical bottleneck in the allocation of registers. Memory locations can be used as accumulators or pointers.

The 16000 has a uniform address space of 16-million bytes, and it uses 32-bit pointers. Unlike some other 16-bit processors, the 16000 allows 16-bit words and 32-bit double-words to start on odd addresses and to cross word boundaries. With many other 16-bit microprocessors, 16-bit words and 32-bit double words must be stored at even addresses.

To implement reliable operating systems, the 16000 has two operating modes—a supervisor mode and a user mode. The operating system runs in supervisor mode, in which any instruction may be executed. Most configurations restrict privileged instructions—interrupt processing, scheduling and memory management—to the operating system. Therefore, a user program cannot damage the operating system or other user programs. Most programs run in the user mode.

The registers of the 16000 comprise eight 32-bit general-purpose registers, eight 32-bit floating-point registers, thirteen 32-bit special-purpose registers, and other registers for software debugging. The general registers are used for arithmetic and logic computations, as well as for holding addresses. The floating-point registers participate in floating-point computations and hold floating-point values. These registers can also be used in even/odd pairs as 64-bit registers.

Special registers handle special needs

Of the thirteen special-purpose registers (Table 1), the frame pointer (fp) is setup when a procedure is entered. The procedure parameters are addressed with positive offsets from the frame pointer; the local variables of the procedure are addressed with negative offsets from the frame pointer. Similarly, the static-base (sb) register is set up by the external procedure-call instruction and the return instruction. This register points to the statically allocated variables of a module or procedure.

The program counter (pc) register points to the first byte of the current instruction. After the instruction is completed, the program counter is updated to point to the next instruction. As its name implies, the user-stack (us) register points to the top element of the user stack.

Table 2. Program status word

```
Program Status Word

              |x x x x I P S U|N Z F x x L T C|
              |15            8|7             0|
              |supervisor PSR | user PSR      |

User PSR

    C: Carry    (Borrow)
    T: Trace    (Single step)
    F: Flag     (Error status)
    L: Low      (unsigned less than)
    Z: Zero     (equal)
    N: Negative (less than)

Supervisor PSR

    U: User mode
    S: US/IS selection for stack
    P: Pending  (Hardware flag)
    I: Interrupt enable
```

Table 3. Addressing Modes

Addressing Modes

Number	Syntax	Name
0-7	r0 or f0	register
8-15	disp(r0)	register relative
16	disp(disp(fp))	frame memory relative
17	disp(disp(sp))	stack memory relative
18	disp(disp(sb))	static memory relative
19		reserved for future
20	value	immediate
21	disp	absolute
22	ext(disp)	external
23	tos	top of stack
24	disp(fp)	frame memory
25	disp(sp)	stack memory
26	disp(sb)	static memory
27	disp(pc)	program memory
28	mode[r0:b]	index byte
29	mode[r0:w]	index word
30	mode[r0:d]	index double
31	mode[r0:q]	index quad

The interrupt stack (is) pointer is the stack used by the interrupt mechanism and the operating system. The interrupt table base (intbase) points to the interrupt vector table. Page table base 1 (ptbl) points to the primary virtual-memory page table for the current process; page table base 2 (ptb2) points to the secondary virtual-memory page table for the current process; and the module (mod) register points to the descriptor for the program module that is currently executing.

When read, the error register gives the address of the most recent virtual-memory page fault. When written, the error register specifies a virtual page that is no longer valid. The floating-point status register (fsr) consists of the floating-point status and control flags, which include the trap enable and occurrence flags. The memory management status register (msr) holds the memory management status and control flags. It is only accessible in the supervisor mode.

The program status register (psr) consists of the central-processor status and control flags. This last special-purpose register is split between the user psr and the supervisor psr (Table 2). The latter may only be accessed in supervisor mode.

Many instructions and addressing modes include an offset value called a displacement, which may be one, two or four bytes long. The size of the displacement is encoded in its first two bits. The encoding of displacements affects both program size and speed of execution. Most offset values are small enough to fit in one byte, so the encoding saves one byte in most memory-reference instructions. However, some offset values are too big to fit in one word. In these cases, the 16000 can use a long displacement, whereas a machine with only word-length offsets would have to generate one or two extra instructions.

Table 3 lists the addressing modes of the 16000. As the operand, the register modes use either a general-purpose register or a floating-point register, depending on the type of instruction. The register-relative modes compute an effective address by adding a displacement to a general-purpose register. The frame, stack and static memory relative modes compute an effective address by: adding a displacement to one of the special-purpose registers (either user stack or interrupt stack, frame pointer, or static base), fetching a double word from this address, and then adding a second displacement to this value so

Table 4. Formats

```
Instruction Format

    |0 0 0 1 0 1 1 1|1 1 0 0 0|0 0 1 1 1|0 0 1 1|0 1|
    |      23       |  (fp)   |   r7    | add   | w |

                   addw r7,23(fp)

----------------------------------------------------------------------

Storage of integer data types in memory

                                                 _ _ _ _ _ _ _ _
                                                |_|_|_|_|_|_|_|_| byte
                                 _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
                                |_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_| word
 _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_|_| double
                                                                  word
|31          24|23            16|15            8|7             0|
|    addr+3     |    addr+2     |    addr+1     |    addr       |

----------------------------------------------------------------------

Floating Point Formats


                                  _ _______ ________________________
                                 |_|_______|________________________|
                                 31|30   23|22                     0|
                                   S  exp        fraction
    ________________________________________________________________
   |_|__________|___________________________________________________|
   63|62      54|53                                                0|
    S   exp              fraction

----------------------------------------------------------------------

Bit field in memory

   ________________________________________       ______________________
   |______LLLLLLLLLL|LLLLLLLLL_______|_____       _____|________________|
    7              0 7              0                7              0
                      base +                ....          base
                      offset div 8

           |<--------------->|<----->|<----       ---------------------->|
                              offset                     offset
                 length       mod 8                      div 8
                 bits         bits                       bytes
----------------------------------------------------------------------


Decimal formats


                                 |dig1|dig0|  byte

                       |dig3|dig2|dig1|dig0|  word

   |dig7|dig6|dig5|dig4|dig3|dig2|dig1|dig0|  double word
   |<--------increasing significance------<|

   |31               16|15      8|7       0|  bit #
   | addr+3  | addr+2  | addr+1  |  addr   |  address
```

as to form the final effective address.

The *immediate* addressing mode takes its operand from the instruction. The absolute addressing mode takes a displacement following the instructions for its effective address. The external addressing mode computes the effective address of a static variable in another module. The top-of-stack mode uses the top of the stack as an operand. If the operand is read, the top is popped off the stack; if it is written, the result is pushed onto the stack; if it is both read and written, the operand is popped off the stack and then the result is pushed on the stack. The frame, stack, static and program memory addressing modes compute an effective address by adding a displacement to a special-purpose register (either user stack or interrupt stack, frame pointer, static base, or program counter).

The index-addressing modes compute an effective address from a register and a second addressing mode. The register value is multiplied by one, two, four or eight (index byte, index word, index double, index quad). The effective address of the second addressing mode is added to the multiplied register value to form the final effective address. Index-addressing modes are used for addressing into arrays, when the elements of the array are bytes, words, double words, floating-point numbers or long floating-point numbers. Powerful and easily generated by compilers, index-addressing modes eliminate the need for autoincrement and autodecrement modes.

Simple formats aid efficiency

Table 4 illustrates the instruction, floating-point, and decimal formats of the 16000, and shows how the processor stores integer data and bit fields in memory.

An instruction may have from zero to four operands, separated by commas. Data normally flow from left to right, and instruction operands are evaluated from left to right. The table shows an add word. The instruction adds the low-order 16 bits of r7 to the word addressed by 23(fp), and stores the result in 23(fp).

The 16000 architecture symmetrically supports 8, 16 and 32-bit binary two's-complement integers. These may be treated as either signed or unsigned numbers. When integers are stored in memory, the least-significant byte is stored at the lowest address; the most significant byte, at the highest address. The number bits within a integer start at 0, which is the least-significant bit.

Floating-point numbers are stored in memory with the least significant bit of the fraction in bit 0 of the lowest address, and with the sign bit as bit 7 of the highest address. A floating-point number consists of a 1-bit sign, a biased exponent and a fraction. Conversion is provided from every integer and floating format to every other integer and floating format.

A bit or contiguous sequence of up to 32 bits in memory or in a register may be read or written by: a base address, which may be an 16000 effective address; a bit offset, which may be an 8, 16 or 32-bit value; and a length from 1 to 32. A bit is a bit field of length one.

The 16000 supports three packed-decimal formats consisting of two, four or eight digits for byte, word or double-word formats. Decimal digits are BCD digits encoded two digits per byte. Within a byte, the least-significant digit is stored in bits 0 to 3; the most-significant digit is stored in bits 4 to 7. In memory, the least-significant byte of a decimal number is stored in the lowest address; the most-significant byte, in the highest address.

A powerful set of instructions

The instruction set (Table 5) of the 16000 is very versatile. For instructions that have integer operands, the opcode includes an operand length represented by I, which may be replaced by b, w or d (specifying byte, word, or double-word length).

Very useful for compiled code are the block move (movm) and block compare (cmpm) instructions. These very short instructions can be used without setting up any registers beforehand. They are written the same way as the standard memory-to-memory move and compare instructions, except for the addition of a third displacement operand, which specifies how many elements (bytes, words or double words) are to be moved or compared. The movil and cmpil instructions are quick forms of the standard move and compare instructions. These instructions encode a small integer operand, in place of a second addressing mode.

Arithmetic instructions have two operands. The opcode specifies the length of each operand. The sec ond operand stores the result of the arithmetic operation. Two pairs of divide instructions—div and mod, quo and rem—round off the final answer. The first pair rounds towards zero (the standard for most machine division), and the second pair always rounds downward (the standard for most algorithms).

The 16000 is the only microprocessor to use 64-bit operands for integer multiple and divide. For these extended multiply and divide (mei and dei), all operands are unsigned. The opcode specifies the length of the first operand; the second operand is twice the length of the first. For shift operations, the second operand is shifted by the number of bits specified by the first operand. If the first operand is negative, the shift is to the right; if it is positive,

Table 5. Instruction set

Instruction Set

Abbreviations used in the instruction set list:

I	b,w, or d (Byte, word, or double)
F	f or l (floating or long floating)
mode	Any addressing mode
disp	Displacement
imme	Immediate
regi	Any general purpose register

Move and Compare

movI	mode,mode	Move integer
moviI	immi,mode	Move immediate integer
movmI	mode,mode,disp	Move multiple integer
mova	mode,mode	Move address
cmpI	mode,mode	Compare integer
cmpiI	immi,mode	Compare immediate integer
cmpmI	mode,mode,disp	Compare multiple integer

Arithmetic Class

addI	mode,mode	Add integer
addiI	immi,mode	Add immediate integer
addcI	mode,mode	Add with carry integer
subI	mode,mode	Subtract integer
subcI	mode,mode	Subtract with carry integer
negI	mode,mode	Negate integer
absI	mode,mode	Absolute value integer
mulI	mode,mode	Multiply integer
divI	mode,mode	Divide integer
modI	mode,mode	Modulus integer
quoI	mode,mode	Quotient integer
remI	mode,mode	Remainder integer

Extended multiply and divide

meiI	mode,mode	Multiply extended integer
deiI	mode,mode	Divide extended integer

Logical operations

andI	mode,mode	And
orI	mode,mode	Or
bicI	mode,mode	Bit clear
xorI	mode,mode	Exclusive or
comI	mode,mode	Complement
notI	mode,mode	Not

Shifts

lshI	mode,mode	Logical shift
ashI	mode,mode	Arithmetic shift
rotI	mode,mode	Rotate

Floating point

movF	mode,mode	Move floating
cmpF	mode,mode	Compare floating
addF	mode,mode	Add floating
subF	mode,mode	Subtract floating
mulF	mode,mode	Multiply floating
divF	mode,mode	Divide floating
negF	mode,mode	Negate floating
absF	mode,mode	Absolute value floating
polyF	regi,mode,mode	Polynomial step
polyfl	regi,mode,mode	Extended polynomial step
dotF	regi,mode,mode	Dot product step
dotfl	regi,mode,mode	Extended dot product step

Format conversion

movzII	mode,mode	Move zero extended
movxII	mode,mode	Move sign extended
movIF	mode,mode	Move integer to floating
movrFF	mode,mode	Move rounded floating to floating
movrFI	mode,mode	Move rounded floating to integer
movtFI	mode,mode	Move truncated floating to integer

Branches, jumps, and conditionals

beq	disp	Branch if equal
bne	disp	Branch if not equal
blt	disp	Branch if less than
ble	disp	Branch if less than or equal
bgt	disp	Branch if greater than
bge	disp	Branch if greater than or equal
blo	disp	Branch if low
bhi	disp	Branch if high
bls	disp	Branch if low or same
bhs	disp	Branch if high or same
bfs	disp	Branch if f set
bfc	disp	Branch if f clear
bcs	disp	Branch if c set
bcc	disp	Branch if c clear
seqI	mode	Set if equal
sneI	mode	Set if not equal
sltI	mode	Set if less than
sleI	mode	Set if less than or equal
sgtI	mode	Set if greater than
sgeI	mode	Set if greater than or equal
sloI	mode	Set if low
shiI	mode	Set if high
slsI	mode	Set if low or same
shsI	mode	Set if high or same
sfsI	mode	Set if f set
sfcI	mode	Set if f clear
scsI	mode	Set if c set
sccI	mode	Set if c clear
jmp	mode	Jump
bra	disp	Branch
caseI	mode	Case branch
acbiI	imme,mode,disp	Add compare and branch immediate
jsr	mode	Jump to subroutine
bsr	disp	Branch to subroutine
ret	disp	Return from subroutine

Strings

movs	b	b	u
cmps	w	-	w
skps	d		-
	t		
move string	byte	backward	until match
compare string	word	-	while match
skip string	double		-
	translated		

Bits

tbitI	mode,mode	Test bit
sbitI	mode,mode	Set bit
sbitiI	mode,mode	Set bit with interlock
cbitI	mode,mode	Clear bit
cbitiI	mode,mode	Clear bit with interlock
rbitI	mode,mode	Reverse bit

Bit Fields

extbfI	regi,mode,mode,disp	Extract bit field
insbfI	regi,mode,mode,disp	Insert bit field
extbfsI	mode,mode,imme,imme	Extract bit field short
insbfsI	mode,mode,imme,imme	Insert bit field short
cvtbfp	regi,mode,mode	Convert bit field pointer

Find First Set

ffsI	mode,mode	Find first set

Decimal

addpI	mode,mode	Add packed
subpI	mode,mode	Subtract packed

Arrays

checkI	regi,mode,mode	Check bounds
indexI	regi,mode,mode	Index array

Register Manipulation

enter	imme,disp	Enter subroutine
exit	imme	Exit subroutine
save	imme	Save registers
restore	imme	Restore registers
sfreg	imme	Save floating registers
rfreg	imme	Restore floating registers
lprI	imme,mode	Load processor register
sprI	imme,mode	Store processor register
adjspI	mode	Adjust stack pointer
bispsrI	mode	Bit set PSR
bicpsrI	mode	Bit clear PSR

Processor Control

nop		No operation
wait		Wait for interrupt
dia		Diagnose
svc		Supervisor call
flag		Flag trap
bpt		Break point
setcfg	imme	Set configuration

External Procedures

cxp	disp	Call external procedure
cxpd	mode	Call external procedure with desrciptor
rxp	disp	Return from external procedure
rett	disp	Return from trap
reti		Return from interrupt
lxpd	mode,disp	Load external procedure descriptor
cvtxpd	mode,mode	Convert external procedure descriptor

Memory management

rdval	mode	Read validate
wrval	mode	Write validate
movf1I	mode,mode	Move from space 1 to space 2
movf2I	mode,mode	Move from space 2 to space 1

the shift is to the left.

The architecture symmetrically supports both the 32-bit and 64-bit IEEE floating-point formats. The opcode for instructions that apply to floating-point operands has a length represented by F, which may be specified as for 32 bits or l for (long) 64 bits.

To simplify the handling of Boolean expressions in compilers, a conditional set instruction stores a 1 into its only operand if a condition code check is satisfied; if not, it stores a 0. The 16000 also implements a position-independent high-level-language case statement (computed goto). The case instruction performs a program-counter relative branch.

Working with strings

There are 48 combinations of string instructions. General-purpose registers point to the operands of these instructions. Strings are arbitrarily long sequences of bytes, words or double words.

Strings can be moved or compared, and an optional translation table may be specified. To avoid destructive overwriting, the operation can proceed from low addresses to high addresses, or vice versa. The operation can proceed unconditionally, or it may be terminated when a comparison condition is met. The operation may stop either when a specific value is encountered or when a value is no longer encountered. A string of instructions may be interrupted, and then restarted where it left off.

All bit instructions store the value of the selected bit into the F flag of the program status register before modifying that value. The interlocked instructions implement multiprocessor test and set, as well as test and clear.

Extract instructions read a bit field, expand the result to the length specified in the opcode, and then store the expanded result into another operand. Insert instructions read an operand of the length specified in the opcode and store the low-order part into a bit field. The convert bit-field pointer converts a byte address and a bit offset into a bit address.

The find first set (ffs) instruction searches a sequence of bits, either in memory or in a register for a bit that is set to 1. The length of the first operand is specified by the opcode; the second operand is a byte. If the first operand has no bits set to 1, a special condition code is returned. Otherwise, the position of the least-significant bit with a value of 1 is returned in the second operand.

For decimal instructions, all operands are of the length specified in the opcode. Both the add and subtract decimal instructions use and set the carry flag, so they can be employed in multiple precision operations.

More general than the similar instructions provided on other microprocessors, the array-bounds-check instruction lets the user specify both a lower bound and an upper bound. It also subtracts the lower bound from the value being checked and stores the difference in a register, where it can be used by an index instruction or an index addressing mode.

The 16000 offers a unique array indexing instruction, which performs one step of a multidimensional array-address calculation. The opcode specifies the length of the second and third operands; the first operand is a general-purpose register. The index instruction does a multiplication and an addition, leaving the result in a register. The result is then used in another index instruction for the next dimension, or it is used in an index addressing mode.

The 16000 also offers flexibility for register manipulation. The procedure entry instruction (enter) saves registers, saves the previous stack frame and allocates variables for the procedure. The procedure exit instruction (exit) deallocates the procedure variables, restores the previous stack frame and restores the registers saved by the enter instruction. The return instruction (ret) returns to the caller and removes the parameters pushed on the stack.

Manipulating registers

The register save and restore instructions include an immediate field of 8 bits, which correspond either to the eight general-purpose registers or to the eight floating-point registers, depending on the instruction. The appropriate registers, for which corresponding bits are set in the mask, are pushed or popped, depending on the instruction.

The lpr and spr instructions allow the loading and storing of any special-purpose register. (In these instructions, imm refers to one of the 16000 special-purpose registers.) The bispsr and bicpsr instructions set and clear bits in the program status register.

The external call and return instructions deal with the modular software and interrupt system. The modular software system implements high-level-language modularity in hardware. It includes provisions for external procedure calls, external variables, Fortran common variables, runtime program relocation and linking, and software libraries that can be distributed in ROMs.

All memory management instructions are privileged. Memory management provides facilities for control of virtual memory, memory protection, memory relocation, multiple address spaces, program flow tracing, and program and data breakpoints.□

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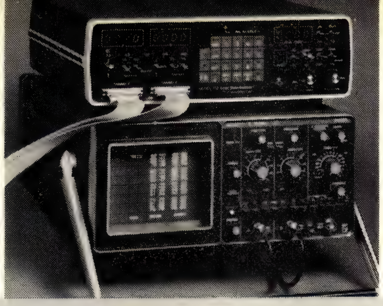

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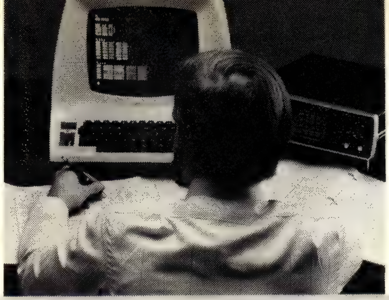

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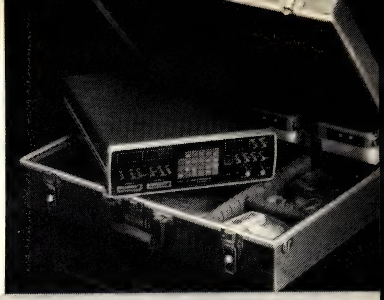

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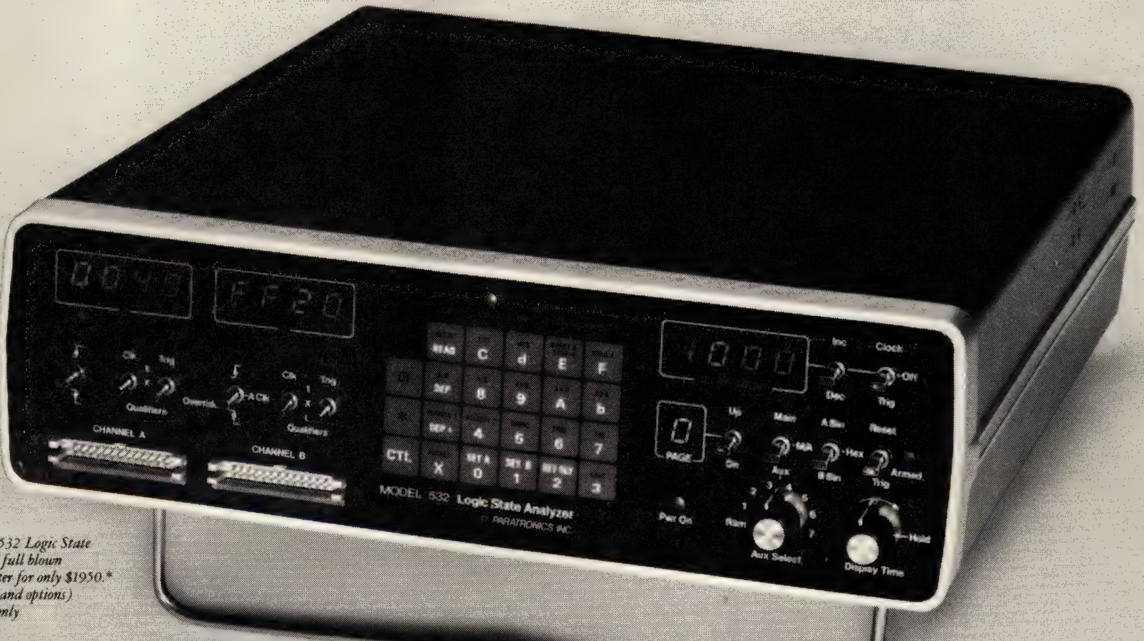

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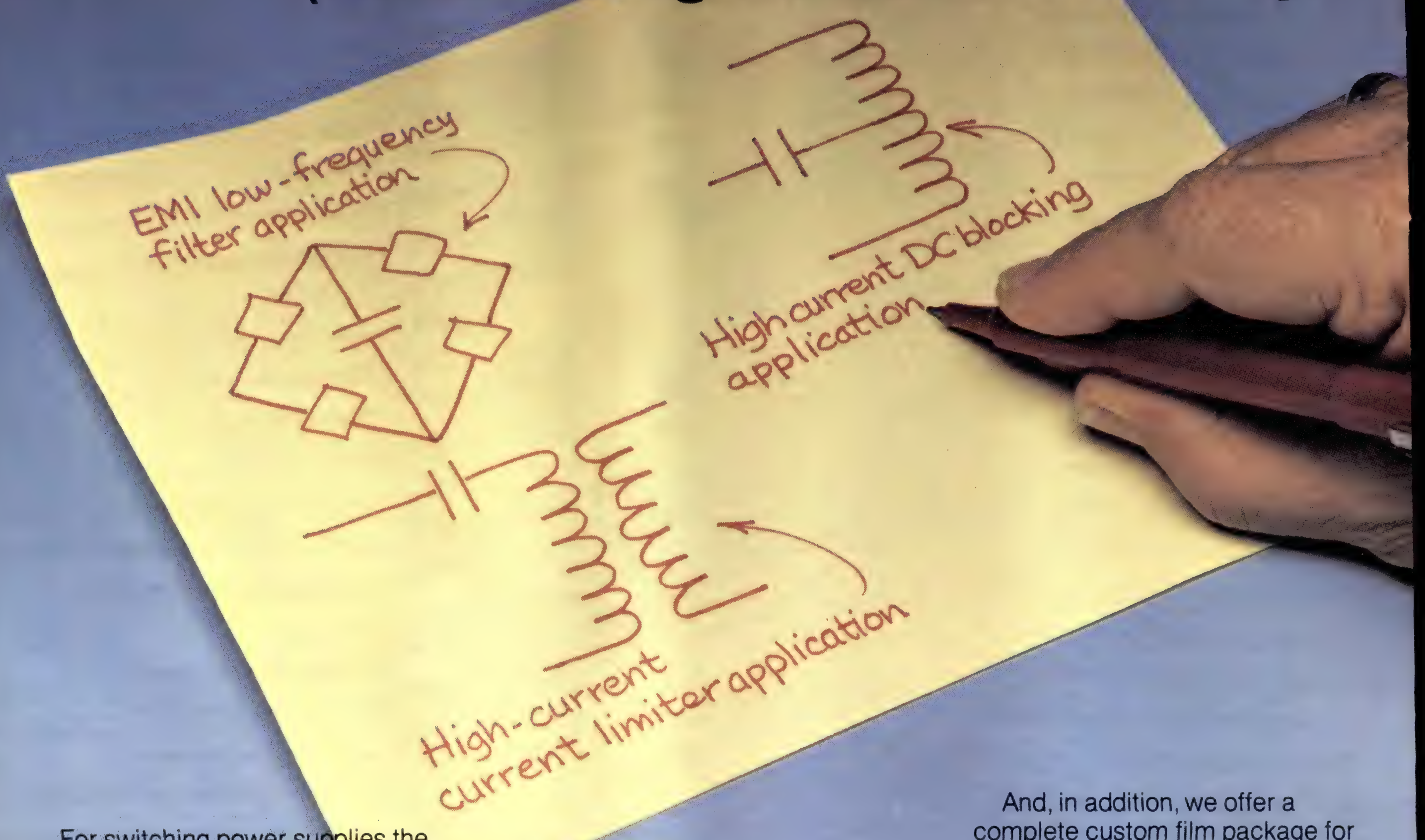
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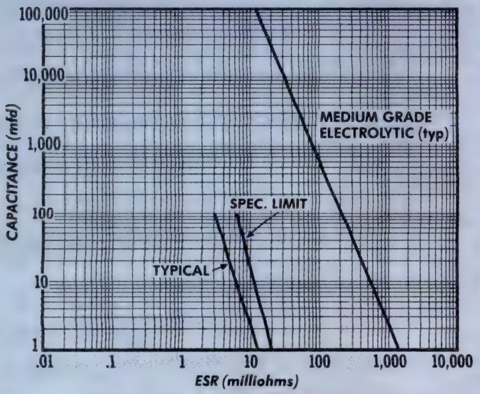

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Analog-to-digital and digital-to-analog IC converter components come in a choice of technologies: bipolar, CMOS or hybrid. Each offers special advantages. But which advantages will do the most good?

Match the converter with the application

With three major converter technologies to choose from—bipolar, CMOS and hybrid—the best way to select an a/d or d/a converter is to match the technology to the application. Each offers distinct advantages—and disadvantages: Monolithic bipolar converters provide precision and speed, and are complete and ready to use. Monolithic CMOS devices, on the other hand, are versatile, can be combined with many logic processes on the same chip, and consume very little power. Multichip hybrids emerge as the most economical alternative where production runs are small, where the bit resolution, accuracy, and speed required are currently unavailable in monolithic form, or where incompatible chip processes are required in the same converter (see "Converter technology tradeoffs"). The application will determine which advantages are most useful.

Bipolar processing produces precision high-speed monolithic converters, complete with references and amplifiers. Until recently, it was impossible to put high-quality logic on the same chip with high-quality linear devices using bipolar processing. Now, both analog and digital circuitry can be fabricated on the same chip using linear-compatible integrated injection logic (I^2L) to produce high-density, low-power logic gates.

Jeffrey R. Riskin, Manager
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Bipolar fabrication begins with the complete standard process, which relies on the laws of physics and photolithography for its initial accuracy, but by itself produces low-cost, medium-precision converters with untrimmed accuracy up to 10 bits. Super-beta transistors can be added to provide amplifiers with very low input bias currents and reasonable stability over temperature. High-quality FETs can be provided on the same chip with ion implantation.

The addition of a bandgap reference will produce precision references for single logic-level power supplies (+5 V), while a buried zener will produce low-noise voltage references. Bipolar current-steering switches produce the high output impedance and low capacitance essential to high-speed operation.

Moreover, precision resistor networks, including the R/2R ladders on data converters, can be deposited accurately on a chip using silicon-chromium thin films, which are laser trimmed to scale. In

Converter-technology tradeoffs

	Monolithic bipolar	Monolithic CMOS	Multichip hybrid
Benefits	Completeness—all elements available High accuracy/stability High speed Analog functions High reliability Low cost	Versatile—Four-quadrant multiplying due to bilateral switches Extensive logic capabilities Good voltage switches Low power High reliability Low cost	Complex designs possible Fast turnaround Highest performance Small quantities possible
Limitations	Unilateral reference capability High power Limited logic	Poor analog functions No references Low speed Low accuracy	Low reliability High cost Large size

contrast to precision resistors—which are diffused into the surface of the chip and which can be trimmed only by cutting jumper links or by zener-zap techniques—deposited thin-film resistors can be laser-trimmed without affecting the silicon substrate. As a consequence, the ratio-match and TCR tracking of laser-trimmed thin films is generally ten times better than diffused resistors. Thin-films can show a ratio match of ±0.005% and TCR tracking of 2 ppm/°C after trimming, compared with ±0.02% ratio-matching and 20 ppm/°C TCR tracking for the trimmed diffused resistors. Laser trimming can be performed on the completed device in a test fixture to obtain a particular measured value, or can be completed on an entire wafer before the individual chips are mounted in an expensive hermetic package. Finally, high-density, low-power logic gates that are completely compatible with linear signal processors can be put on the same piece of silicon using I^2L.

All of these process technologies can be joined in a single bipolar converter chip to produce complete successive-approximation ADCs or complete monolithic DACs with no external components or user trims required to interface with μP data buses.

The recently introduced AD558, for example, is a totally integrated monolithic 8-bit DAC that combines I^2L data latches and an ECL control gate for μP interfacing, a precision bandgap reference (for logic-level supply operation), a laser-trimmed, thin-film R/2R ladder network (for full calibration and monotonicity over temperature), pnp switches for single-supply operation, and an output buffer amp (Fig. 1). Able to run off one +5 to +15-V supply, the AD558 will also interface any μP or data bus with no additional components or power supplies required. The output will settle in less than 1 μs to ±1/2 LSB. This part costs as little as $6.00 apiece in production quantities.

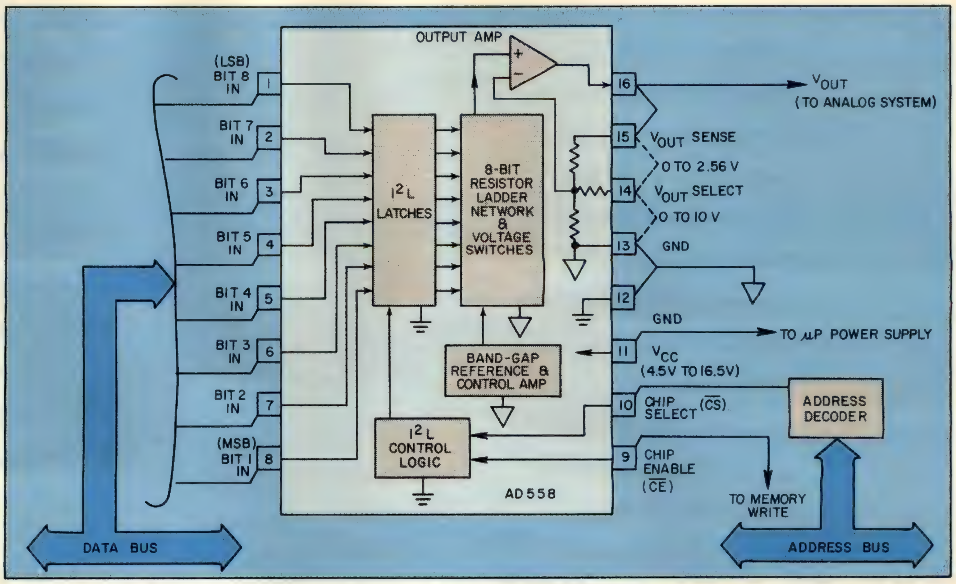
Meanwhile, monolithic bipolar DACs are now available with up to 12 bits, a current output and no μP interface. Eight bits is currently the limit for complete DACs, though devices with more than 8-bit resolution are on their way.

Like bipolar DACs, monolithic bipolar ADCs may include interface and control circuitry, a precision reference and comparator on the same factory-trimmed chip—all to make the part useful without additional components. In addition, the conversion technique most suited to data-acquisition applications is successive approximation.

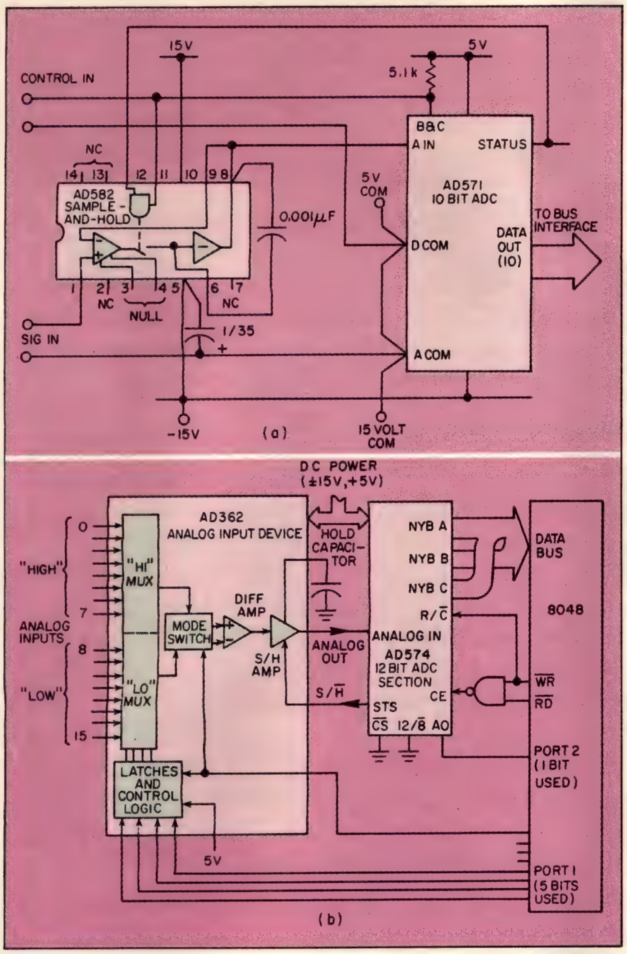
Here, the analog input signal is compared to the analog output of a precision DAC. Each bit is "tried" in succession, most significant bit first. If the input exceeds the DAC output, the bit in question is left on; if smaller, that bit is turned off.

For an n-bit ADC, for example, the DAC must be cycled only n times (plus one to signal the end of conversion). This technique results in a fairly rapid converter, with the DAC and comparator accounting for most of the accuracy and speed restrictions.

Ten bits is the present limit for complete monolithic successive-approximation ADCs. A good example of a complete 10-bit successive-approximation ADC is the Analog Devices AD571, which provides I^2L and bipolar processes, laser-trimmed thin-film resistors and a buried-zener reference—all on one chip. The ADC provides a 30-μs conversion time, requires a −15 V and a +5 V power supply,



1. Bipolar DACs like the AD558 provide I^2L data latches, R/2R ladders networks, pnp switches and a precision bandgap reference all on the same chip.



2. Data-acquisition systems using high-resolution successive-approximation a/d converters may require a sample-and-hold circuit (top) or fast multiplex switches (bottom), to accommodate analog input signals, which change before the conversion is complete.

and has three-state output buffers. For input signals changing more than 1/2 LSB in 30 µs, a sample-and-hold circuit, such as Analog Devices' AD582, can be used to freeze the input signal until the entire successive-approximation conversion cycle can be completed (Fig. 2a).

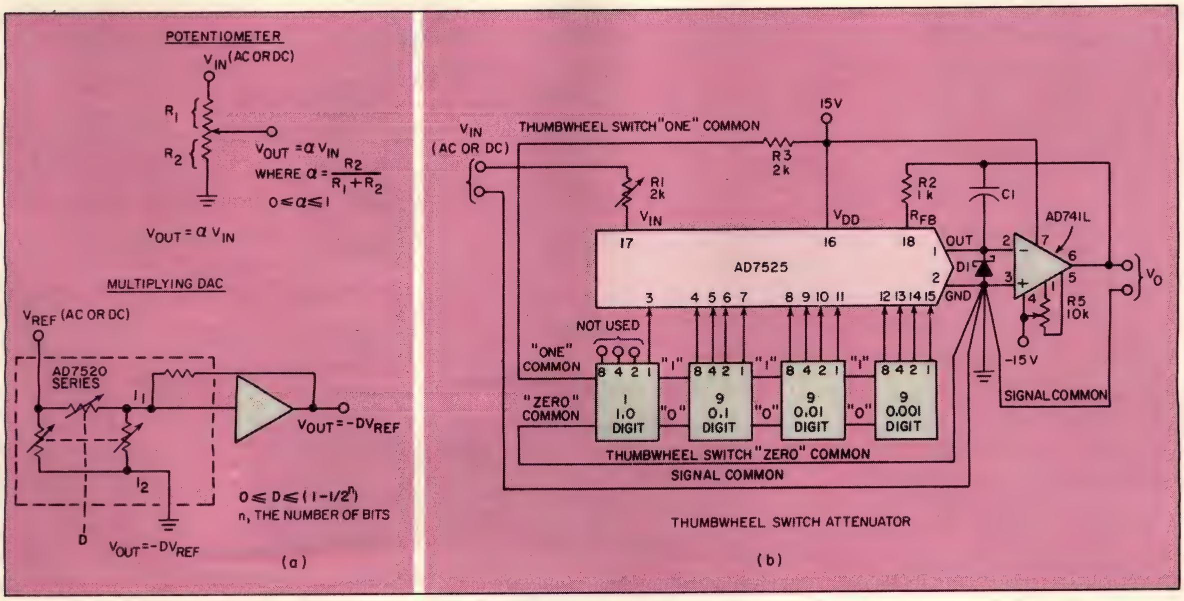
Due to chip size limitations, bipolar monolithic 12-bit a/d converters are still on the horizon; in the mean time, two-chip devices like the AD574 perform 35-µs conversions with a minimum of interface circuitry (Fig. 2b). The monolithic version is a year or so away.

CMOS versatility

While bipolar processing provides completeness, precision and speed, the tradeoff is chip size and power. CMOS devices, on the other hand, require very little current to operate, which suits them to remote or battery-powered applications. Low power consumption, in addition, means that complex logic functions may be put next to a precision converter (on the same chip) without generating heat, which would cause linearity errors by a shift in the values of the bit-weight resistors.

Because CMOS devices are manufactured without references, and because CMOS switches are bilateral, the devices can digitally control virtually any external reference voltage—positive or negative, ac or dc. So if the application calls for the applied analog voltages to be controlled—as in audio signal processing or motor controls—the absence of a precision internal reference need not be a disadvantage, but actually an added measure of versatility.

The bilateral capability of CMOS switches, in fact, allows CMOS DACs to operate in a multiplying

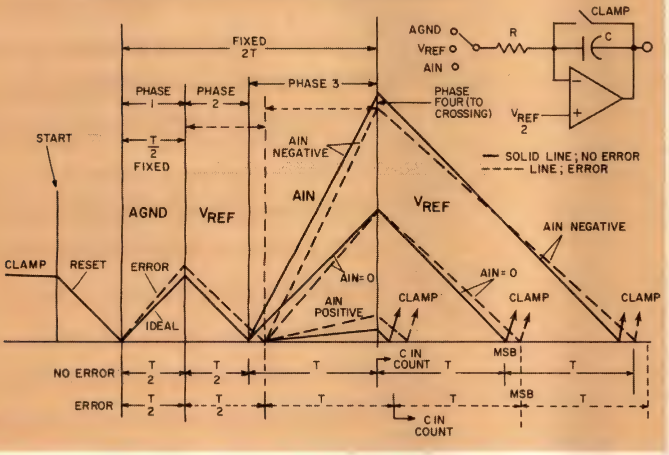


3. A CMOS multiplying DAC can serve as a precision analog signal attenuator (left). Application requires BCD coded switches and an external op amp (right).

Quad-slope integrating converters

The prime advantages of integrating converters, especially in digital multimeter circuits, are that they are inexpensive and accurate. While the integrating converter will require an external capacitor and a precise external reference voltage, everything else —comparator, control logic, clock, and counter circuitry—can be fabricated on one CMOS chip. But CMOS amplifiers and comparators suffer large input voltage offsets and offset drifts, so complex autozero techniques are frequently required to realize the potential accuracy of integrating converters.

The approach used by Analog Devices on its CMOS integrating converters is the patented Quad-slope method. Here, the converter functions very much like a dual-slope converter, but actually includes two additional integration phases to cancel offset and scale-factor errors. Quad-slope conversion assumes, in fact, that the effect of an error is to shift the times of all zero crossings in the conversion process. That is, if all pulses are counted from the zero crossing and from time T, the effect of an error term will be to initiate the counting process at time T + Δ T. The quad-slope approach, simply stated, relies on additional counting processes—initiated at T + Δ T —specifically intended to track the error term (ΔT) and digitally subtract it from the final product term when the conversion is completed.



mode; that is (digital signal) × (analog signal). Ordinarily with DACs, the internal reference will control the amplitude of the analog output signals with given digital inputs. In principle, an external reference voltage will accomplish the same thing. But in the multiplying mode, the reference input can take the form of any analog signal voltage, and can be processed through the DAC using the digital inputs as the control variable.

This can be illustrated in the AD7525 multiplying DAC, which easily serves as an analog signal attenuator with BCD-coded thumbwheel switches at the digital input and an external op amp to provide the analog output (Fig. 3).

Because CMOS is more process-dependent than bipolar, the accuracy of CMOS DACs may not be as great. Without on-chip amplifiers and references, moreover, increasing the sophistication of monolithic CMOS converters requires increasing the accuracy as well as the number of bits, and adding digital interface circuitry (such as latches and registers). Eight-bit CMOS converters with no on-chip interface circuitry go for as little as $2. However, 12-bit CMOS DACs like the AD7542 provide on-chip registers for full digital interfacing and go for as little as $10.00 in OEM quantities (Fig. 4).

Ratiometric ADCs

The complement to the CMOS "multiplying DAC," is the complete CMOS "ratiometric ADC," whose ability to work "referenceless" makes it a versatile device, especially in transducer applications. The ability to measure transducer outputs without a reference is made possible by using the full-scale transducer output as the reference and interpreting the output of the conversion process as a percentage of full scale. A good example of a useful data acquisition component is the AD7574 8-bit a/d converter, which has a full μP interface (Fig. 5). CMOS processing limits the performance of linear circuits, like amplifiers and comparators, to the 8-bit level. More bits require an external comparator, as in the 10-bit AD7570.

At this point, CMOS devices do not lend themselves easily to high-resolution successive-approximation a/d converters, primarily because of the comparator, which is a quasilinear device. Currently, comparator stability is limited to the 10 to 20-mV error region, or ±1/2 LSB at eight bits for a 10-V full scale. However, CMOS converters offer a distinct advantage in interfacing with low-level logic circuitry. Integrating converters, such as those used in digital multimeters and other digital displays, are typically fabricated in CMOS. On-chip CMOS switches permit correction techniques such as Analog Devices' patented "quad-slope" method (see "Quad-slope Integrating Converters") to the conversion process.

Although time-consuming, this correction process will add accuracy to the device and will function within the digital display type speeds of this type of converter, which can deliver up to 13 bits in monolithic form (AD7550) but up to 5-1/2 digits (18 bits) can be achieved with external bipolar amplifiers and comparators (AD7555).

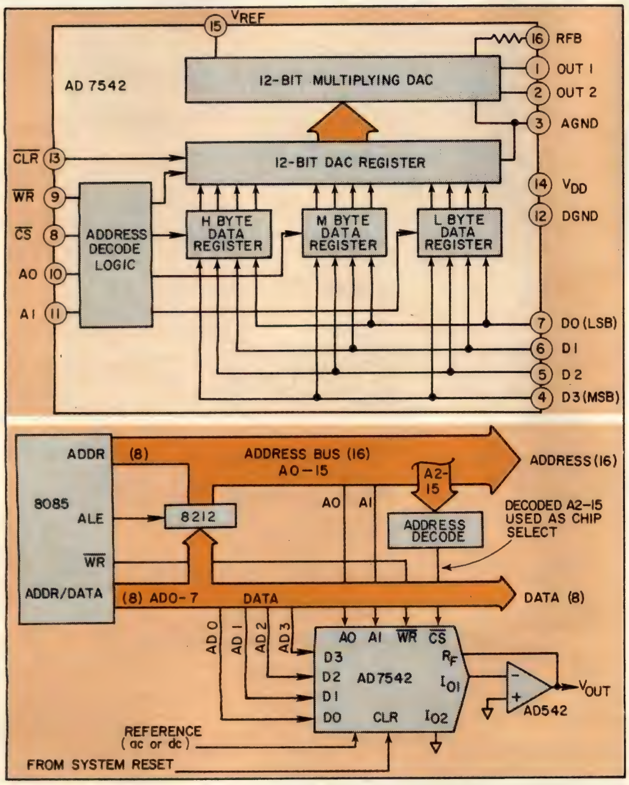
High-performance hybrids

But where monolithic versions would be too expensive, either because of low yield or because of limited production requirements, and where high performance and complexity are required, hybrid converters have the advantage. Combining several monolithic chips on the same substrate allows specialized processes on the same device.

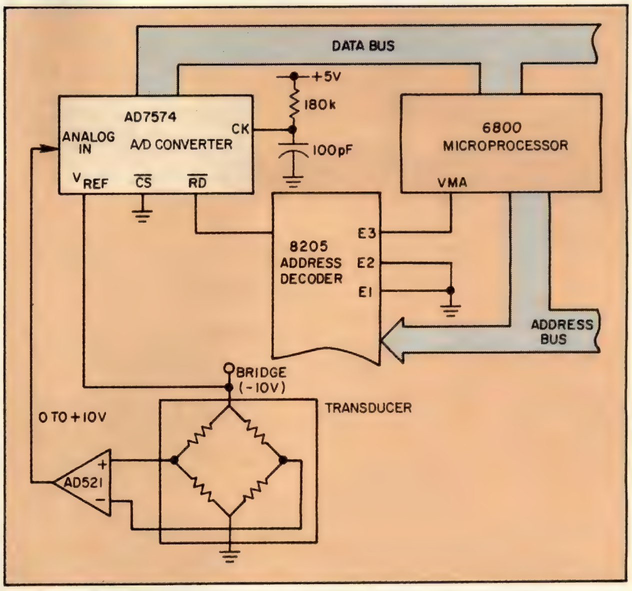
The small volume or special product, in fact, is often best implemented in hybrid form. It takes up to a year to produce a monolithic IC once the design is firm. A low-volume hybrid or multichip design, on the other hand, can be turned around in the time it takes to obtain the chips if an in-house thick-film/substrate capability is available.

The original AD563 12-bit bipolar reference DAC required three chips each for switches, resistors and reference. Initially, some were made in monolithic form but, due to chip size, low yields drove the cost out of sight. But now, new processing techniques allow the AD563 to be produced economically on one chip, whose area is approximately equal to the sum of the three original chips. And a new design, using new circuit and processing techniques (the AD565), gives five times the speed of the AD563 with a smaller chip area.

When extremely high speed or accuracy is required, exotic IC processes supply very fast monolithic converters, but their prices are pushed up by a low yield that reflects the difficulty of the process and the large size of the chip. Furthermore, performance is currently in the 8 to 10-bit region.



4. High-density CMOS switches provide an assortment of on-chip logic, such as three 4-bit data registers on a 12-bit multiplying DAC (top). The registers provide direct interface with the 8085 and other popular μPs (bottom).



5. "Referenceless" CMOS successive-approximation a/d converters readily digitize transducer inputs for data acquisition and industrial-process controls.

Hybrid fabrication, however, economically combines nearly mutually exclusive processes such as fast gold-doped pnps and high-beta npns in one component by using two different chips. The fastest (and hottest) logic may be put an inch away from the DAC resistors. And rework is possible if a chip fails to live up to its dynamic specs. Currently, the state of the art for commercial production hybrids includes 20-ns, 8-bit and 35-ns, 12-bit DACs (such as the Analog Devices HDH/HDS series), along with 1.2-μs, 8-bit and 2.2-μs, 12-bit ADCs (HAS series).

When extreme complexity is required, wafer yield is usually the biggest concern. Chip size prohibits the manufacturer from making the entire analog section of a data-acquisition system on one chip. Even if it were possible, performance would suffer. For example, CMOS makes ideal multiplexers for interfacing to sensitive transducers. But bipolar is better for linear devices such as amplifiers. And TTL logic is faster than CMOS or I^{2}L. Until very complex multiprocessing techniques are developed, combining these three processors on the same chip will be incompatible from an economic standpoint. In the mean time, a multitechnology device such as the 12-bit AD362, which consists of multiplexer, differential amplifier, sample-and-hold and control logic, will use several different chips mounted.□

How useful?	**Circle No.**
Immediate design application	541
Within the next year	542
Not applicable	543

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CIRCLE NO. 61

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Freedom for the CPU.

Our new 8272 double density floppy and mini-floppy disk controller is the right solution for systems designers. It saves time, reduces power dissipation and slices the high cost of burdening an 8-bit or a 16-bit CPU with floppy disk control functions. A powerful instruction set built into Intel's new 8272 controller will reduce your programming efforts up to 50%. Less code is required, so you spend less time and use less memory.

Intel's 8272 solution also tackles the problem of CPU overhead and software intervention. Our double density floppy disk controller has the capability of scanning a single sector or an entire track's worth of data fields. Data on the floppy disk gets compared byte-by-byte with data in your system memory. And, since a single command locates and compares the data, no additional software is necessary.

Faster data access.

Our new 8272 controller does more than drive up to four floppy disks simultaneously. It handles parallel seek on up to four disks for faster data access.

With multi-sector and multi-track transfer capabilities, the CPU is freed from time-consuming I/O commands. Our new double density floppy disk controller removes the limitations of reading or writing only the number of characters a physical sector allows. The 8272 automatically transfers data across the disk's consecutive sectors... and, as a result, the CPU isn't forced to wait until the next sector is positioned. With Intel's new 8272, you not only free the CPU, you get the assurance of higher system performance.

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CIRCLE NO. 60

How to avoid buying ATE hardware this year that you'll have to replace next yea

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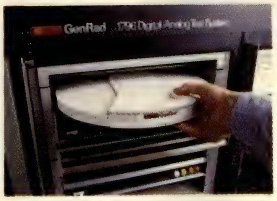
All GenRad functional board test systems are software-based. To adapt to a new technology, you simply install an updated software package.

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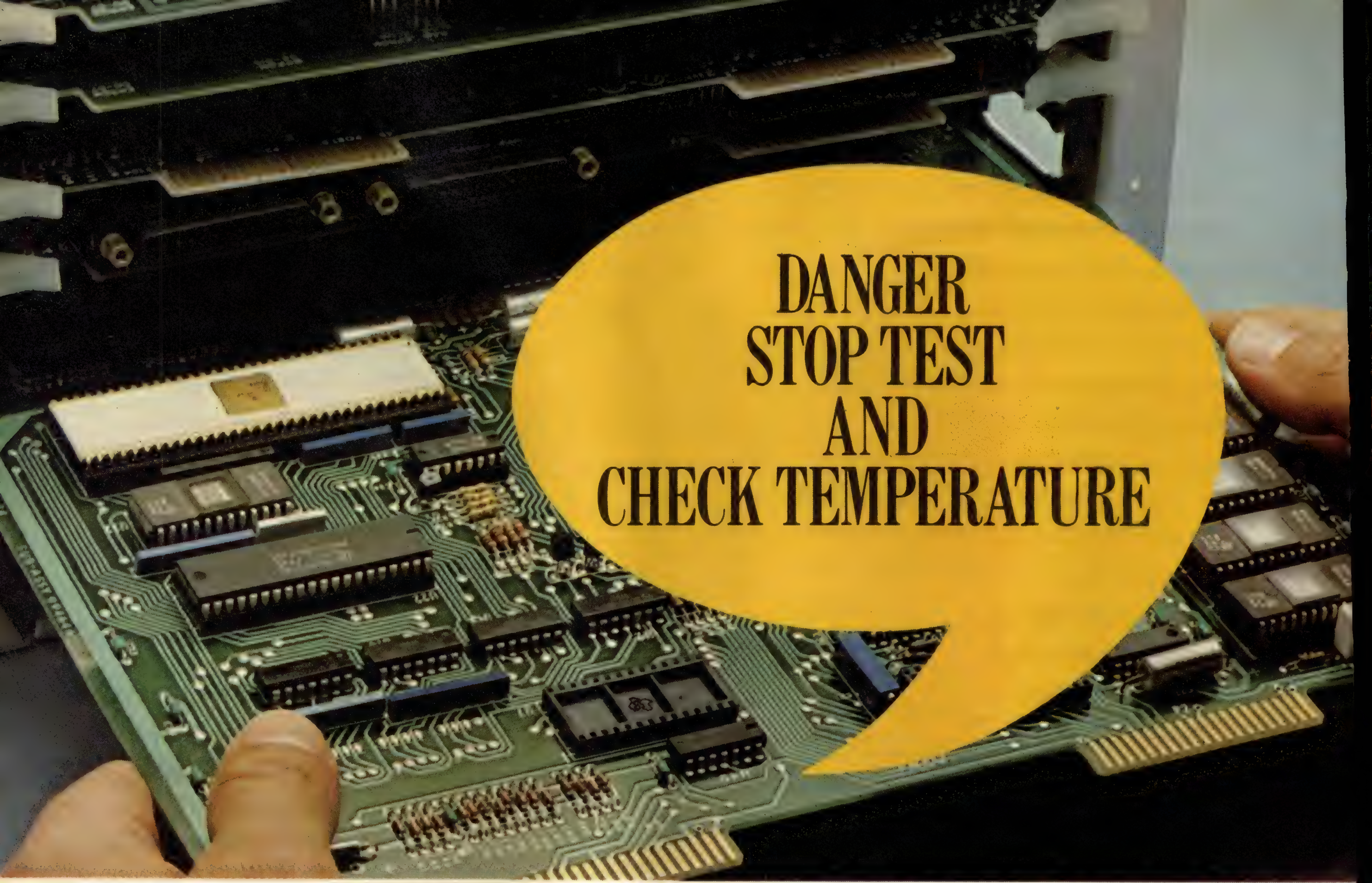
CIRCLE NO. 59



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CIRCLE NO. 62

Bring the advantages of synchronous data-link control to 16-bit μP systems with a synchronous controller that simplifies interfacing.

Controller plugs SDLC into 16-bit μP systems

Incorporating synchronous data-link control (SDLC), a widely used data-communications protocol, brings great advantages to 16-bit μP systems —and problems. This bit-oriented technique offers excellent error detection and recovery procedures; at the same time, its bit-pattern structure must be followed exactly—and the required circuitry can be complex. The TMS 9903 synchronous communications controller (SCC) greatly alleviates such problems for systems based on the TMS 9900 CPU.

Basically, the SCC facilitates microcomputer control of a communications channel by serializing and deserializing data. Fabricated in n-channel silicon-gate MOS, it operates from dc to 250 kbits/s, is compatible with TTL on all inputs and outputs, and uses a 5-V power supply and a single-phase clock.

The system CPU communicates with the SCC by means of the controller's communications register unit (CRU), one of five major sections that include a transmitter section, a receiver section, an interval-timer section and an interrupt section (Fig. 1). The CRU interface consists of nine lines: five address-select lines (S0 through S4, a chip-enable line $(\overline{CE})$, and three CRU lines. An additional input to the CPU is the SCC interrupt line $(\overline{INT})$.

Just about any communications system involving a TMS 9900 CPU and a TMS 9903 SCC may be represented by the block diagram of Fig. 2. The SCC occupies 32 bits of CRU space. The least significant bits of the address bus are connected to the select lines. The 32 bits are selected individually by processor-address lines A10 through A14, which are connected to SCC-select lines S0 through S4, respectively.

The most significant address bits are decoded to select the TMS 9903 using the chip-enable signal. When this line is inactive (high), the SCC CRU interface is disabled. The SCC $\overline{INT}$ line is sent to the TMS 9901 programmable systems interface (PSI) for prioritization and coding.

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Gary Brown, Engineering Manager for AMPL
Texas Instruments, Inc.
8500 Commerce Park, Houston, TX 77036

The SDLC connection

For SDLC, communications channels can be configured in two basic ways: point-to-point and multipoint. To see how the SCC fits in, examine a loop (Fig. 3) configured as unidirectional, half-duplex, point-to-point.

A loop contains one primary station, or loop controller, and any number of secondary stations (the loop in Fig. 3 contains two). A secondary station is physically disconnected from the loop when its power is off; all loop traffic bypasses the terminal through a set of relay points. When power is applied, the terminal is connected to the loop and immediately begins monitoring it for an end-of-poll (EOP) character. When an EOP (01111111) is detected, the terminal switches a 1-bit delay into the loop.

If a secondary terminal employs a TMS 9903 to handle its communications, the 9903 is initialized in the loop slave pending configuration. In this configuration, the 9903 monitors the loop for an EOP and automatically introduces the 1-bit delay when the EOP is detected.

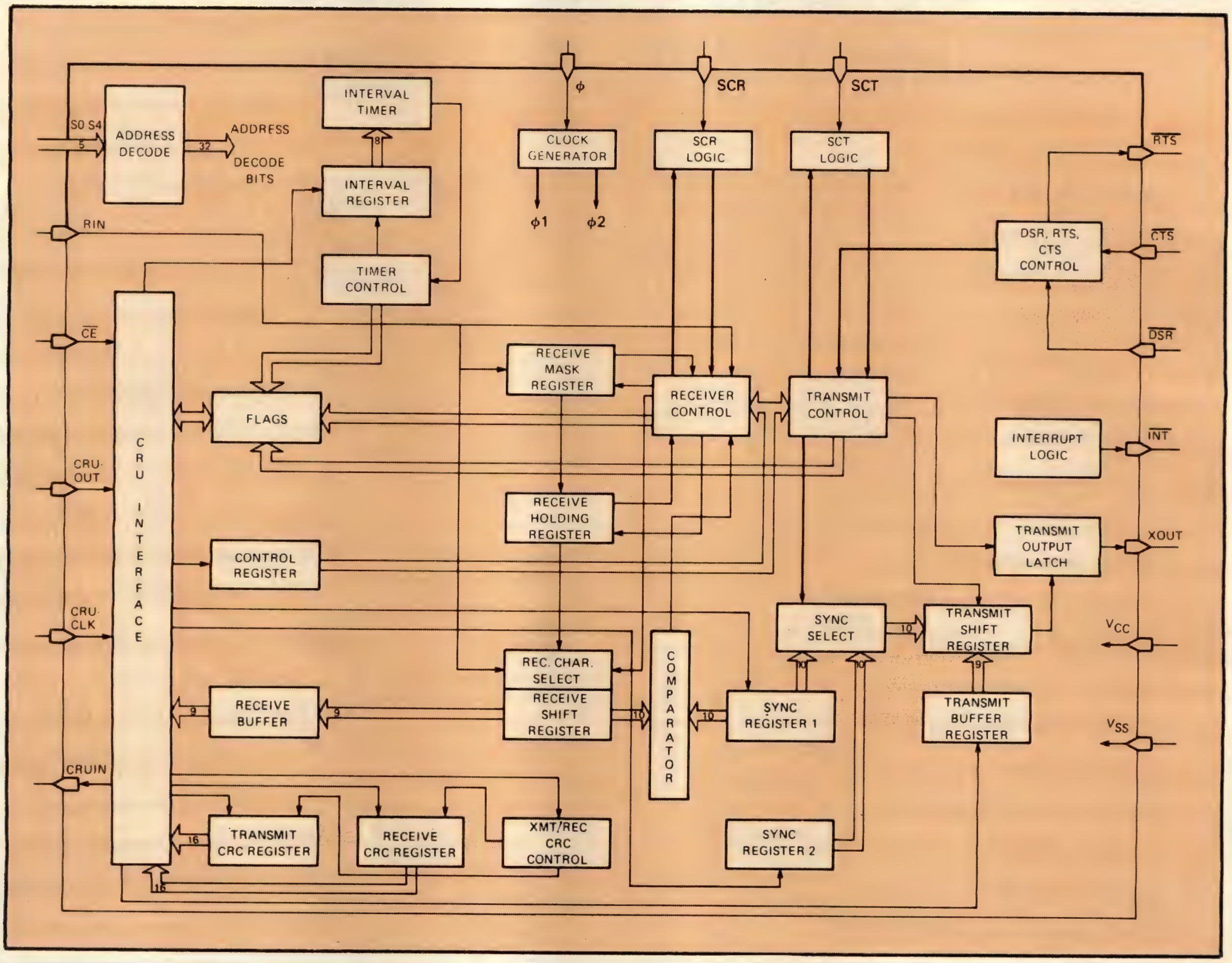
As Fig. 3 illustrates, signals sent out by the loop controller are relayed from station to station, each secondary station acting as a repeater with a 1-bit delay. Any secondary station finding its address in the A field captures the frame for action at that station (see "SDLC Basics"). If the station needs to transmit and if authority is granted by the primary station, an SDLC flag (F) is generated by inserting a binary 0 in place of the seventh binary 1 encountered in an EOP character, which originates at the primary station and is sent after the last frame. The P bit in the C field of the last frame determines whether or not a secondary station may transmit.

After changing the EOP to an F, the secondary station stops acting as a repeater and transmits one or more frames, with the F bit of the last frame set. It concludes transmission with the ending F followed by an EOP, then resumes its role as a repeater.

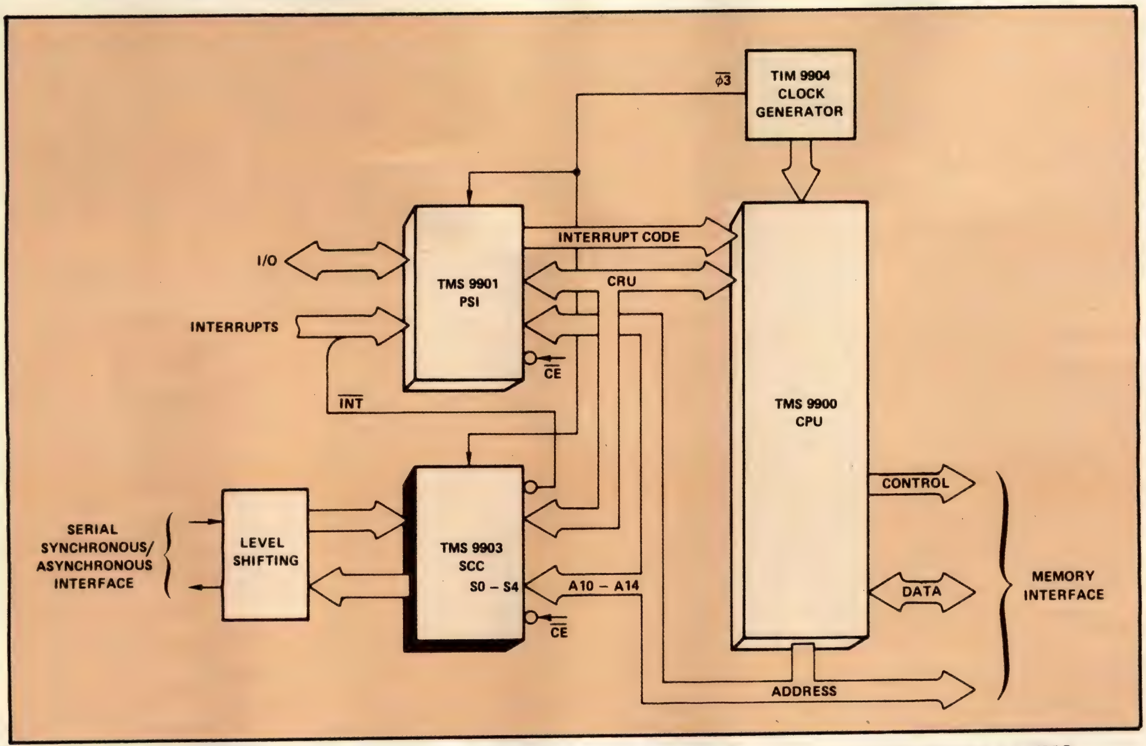
The EOP character is repeated down-loop. By the time the primary station receives the EOP character, each secondary station will have had an opportunity to transmit. The primary station may then either stop receiving and initiate another cycle, or may transmit flags to maintain bit synchronization until the CPU is ready to transmit again.

Configuring the stations

The hardware for handling frames in the loop of Fig. 3 consists of three TM990/101 CPU boards—one for each station. Each board contains 2 kbytes of read/write memory and a TIBUG ROM monitor. TIBUG loads the software into the working memory for debugging and for program execution. Each



1. This synchronous communications controller communicates with its host CPU through the communications register unit. The interface consists of five address-select, three CRU, and a chip-enable line.



2. Practically any microprocessor system in which a TMS 9903 is used to control communications for a TMS 9900 CPU may be represented by this configuration, which also uses a TMS 9901 programmable systems interface.

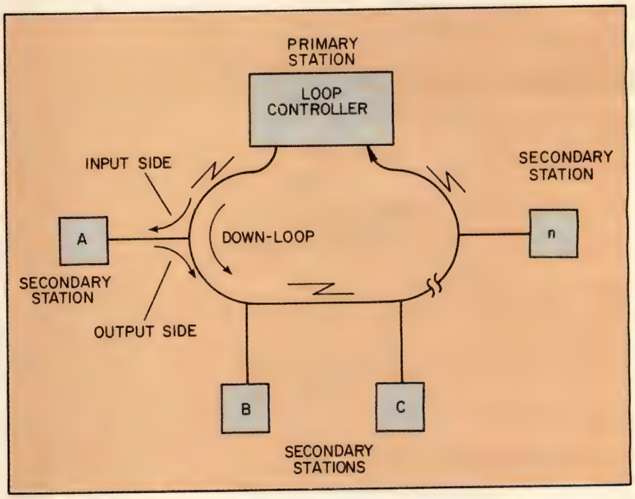
board also has two EIA ports: a TMS 9902 port for terminal I/O, and a TMS 9903 port for the SDLC loop communications.

The Table lists the pin assignments for the TMS 9903s and also presents the pin-connection list for the loop configuration. On the TM990/101 board, pin E2 is jumper-connected to pin E6 for interrupt level 4 (9903), and E5 goes to E3 for interrupt level 5 (9902).

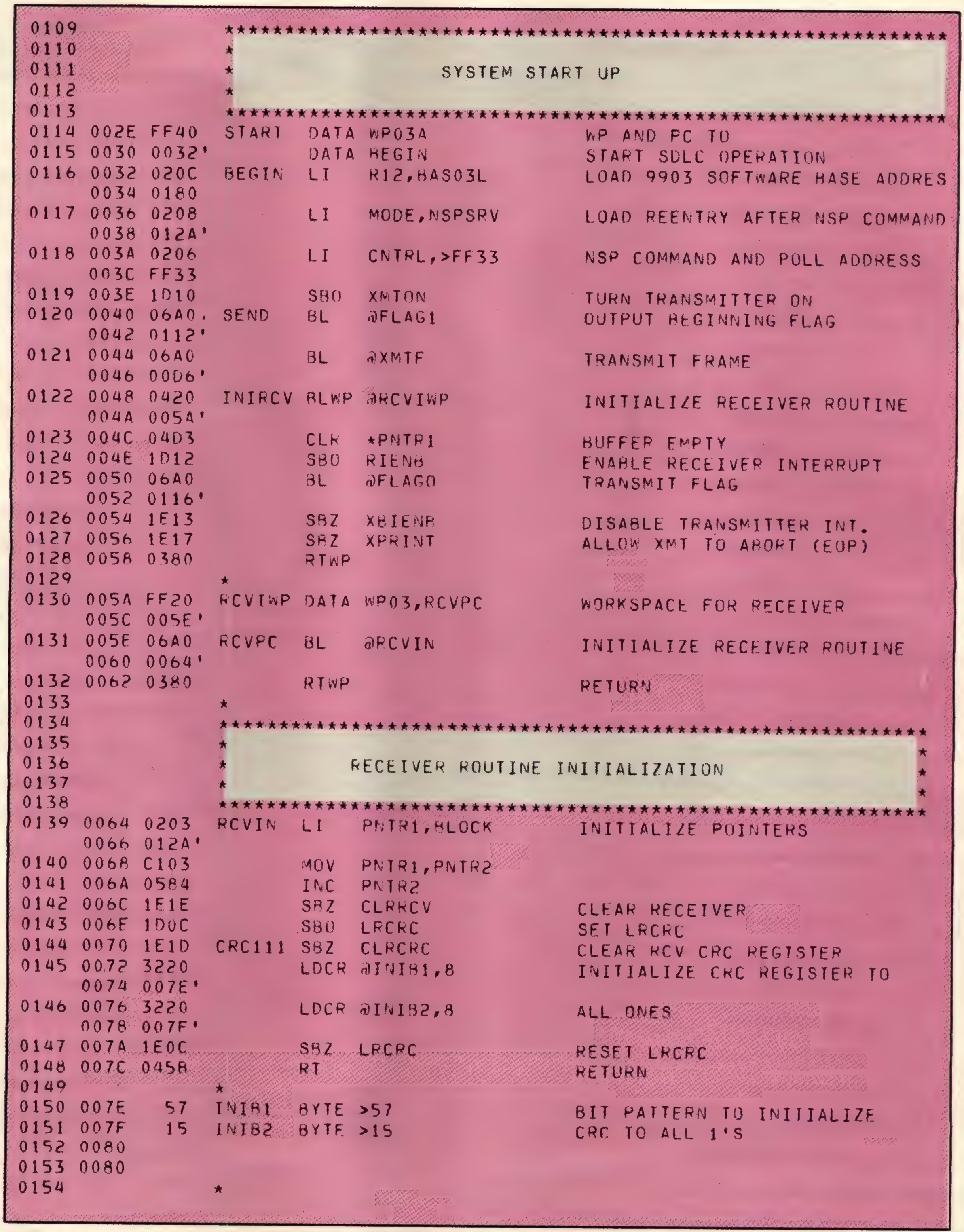
The CPU's interrupt vector locations for levels 4 and 5 are hex 10 and 14. TIBUG ROM locations 10 and 12 contain hex values FF7E and FF9E for the new WP and PC of interrupt level 4. ROM locations 14 and 16 contain hex values FF72 and FF92 for interrupt level 5. RAM locations FF9E and FF92 are loaded with a BLWP instruction followed by an RTWP instruction to branch to the service routines and return from interrupt.

Once the 9903 is initialized, interrupt levels 4 and 5 are enabled and the SDLC communication starts with a BLWP @ START instruction. The start routine (Fig. 4) enables the transmitter interrupt and transmits the first frame—a nonsequence poll (NSP). Register 8 is used to enter the SDLC routines after all frames from secondary stations are received in response to the command of the primary station. Therefore, before transmitting the NSP command, register 8 is loaded with the reentry address of routine NSPSRV.

Before transmitting each frame, the transmitter CRC register must be initialized to all ONEs. To



3. This unidirectional, half-duplex, point-to-point communications loop has a primary station, which acts as the loop controller, and any number of secondary stations.



```
0109                    ******************************************************************
0110                    *
0111                    *                         SYSTEM START UP
0112                    *
0113                    ******************************************************************
0114 002E FF40   START   DATA WP03A               WP AND PC TO
0115 0030 0032'          DATA BEGIN               START SDLC OPERATION
0116 0032 020C   BEGIN   LI   R12,BAS03L          LOAD 9903 SOFTWARE BASE ADDRES
     0034 0180
0117 0036 0208           LI   MODE,NSPSRV         LOAD REENTRY AFTER NSP COMMAND
     0038 012A'
0118 003A 0206           LI   CNTRL,>FF33         NSP COMMAND AND POLL ADDRESS
     003C FF33
0119 003E 1D10           SBO  XMTON               TURN TRANSMITTER ON
0120 0040 06A0   SEND    BL   @FLAG1              OUTPUT BEGINNING FLAG
     0042 0112'
0121 0044 06A0           BL   @XMTF               TRANSMIT FRAME
     0046 00D6'
0122 0048 0420   INIRCV  BLWP @RCVIWP             INITIALIZE RECEIVER ROUTINE
     004A 005A'
0123 004C 04D3           CLR  *PNTR1              BUFFER EMPTY
0124 004E 1D12           SBO  RIENB               ENABLE RECEIVER INTERRUPT
0125 0050 06A0           BL   @FLAG0              TRANSMIT FLAG
     0052 0116'
0126 0054 1E13           SBZ  XBIENB              DISABLE TRANSMITTER INT.
0127 0056 1E17           SBZ  XPRINT              ALLOW XMT TO ABORT (EOP)
0128 0058 0380           RTWP
0129                    *
0130 005A FF20   RCVIWP  DATA WP03,RCVPC          WORKSPACE FOR RECEIVER
     005C 005E'
0131 005E 06A0   RCVPC   BL   @RCVIN              INITIALIZE RECEIVER ROUTINE
     0060 0064'
0132 0062 0380           RTWP                     RETURN
0133                    *
0134                    ******************************************************************
0135                    *                                                                *
0136                    *              RECEIVER ROUTINE INITIALIZATION                   *
0137                    *                                                                *
0138                    ******************************************************************
0139 0064 0203   RCVIN   LI   PNTR1,BLOCK         INITIALIZE POINTERS
     0066 012A'
0140 0068 C103           MOV  PNTR1,PNTR2
0141 006A 0584           INC  PNTR2
0142 006C 1E1E           SBZ  CLRRCV              CLEAR RECEIVER
0143 006E 1D0C           SBO  LRCRC               SET LRCRC
0144 0070 1E1D   CRC111  SBZ  CLRCRC              CLEAR RCV CRC REGISTER
0145 0072 3220           LDCR @INIB1,8            INITIALIZE CRC REGISTER TO
     0074 007E'
0146 0076 3220           LDCR @INIB2,8            ALL ONES
     0078 007F'
0147 007A 1E0C           SBZ  LRCRC               RESET LRCRC
0148 007C 045B           RT                       RETURN
0149                    *
0150 007E   57   INIB1   BYTE >57                 BIT PATTERN TO INITIALIZE
0151 007F   15   INIB2   BYTE >15                 CRC TO ALL 1'S
0152 0080
0153 0080
0154                    *
```

4. The start routine enables the transmitter interrupt and transmits the first frame—a nonsequence poll (NSP).

transmit the beginning and ending flags, the zero-insertion bit must be set before loading the transmitter buffer. (Flags are not loaded into the transmitter CRC register.) The control, address and information bytes are loaded into the transmitter-buffer and the CRC register. The transmitter CRC register is read and transmitted as the FCS field of the frame.

Frames are transmitted with a beginning flag, one or more flags between frames, and an ending flag. At the end of transmission, the transmitter interrupt is disabled, XPRNT is reset to allow the transmitter to abort (EOP), and the routine is initialized. Note that because there are only two secondary stations in the loop, the receiver routine can be initialized immediately after the last frame is transmitted. Each station causes a 1-bit delay. So, if there had been more than 32 stations in the loop, the delay might have exceeded one frame, and the receiver would have had to wait until the last frame of the primary could propagate around the loop.

Synchronizing the receiver

The receiver can be cleared with a simple set of instructions. Once cleared, it goes into a wait loop and does nothing until a flag is detected marking the beginning of a frame. The receiver is then synchronized with the controller.

The first byte of the frame is not loaded into the receiver-buffer register (RBR) until 24 bits later. These 24 bits must contain no flags. An 8-bit delay occurs when RIN is shifted into the RMSK register (Fig. 5). If a flag pattern is detected in the RMSK register, the 8-bit delay is repeated. An additional

SDLC basics

There are essentially two types of data-link control for synchronous communications systems: character-oriented and bit-oriented. SDLC is a bit-oriented protocol, which means that it defines bit patterns.

Since the protocol defines bit patterns, it is essential that the protocol's control bit patterns not be contained in the message. Otherwise, they will be detected, causing message errors. To prevent this, and to detect message-transmission errors, most synchronous protocols for data-link control define the message structure. The structure consists of frames, with the structure of each frame precisely defined.

The message (frame) format for an SDLC message has five elements, or fields: flag (F), address (A), control (C), information (I) and frame-check sequence (FCS). Each frame is enclosed in flags. The first flag is a reference point for the position of the address and control fields. It also initiates transmission-error checking and bit synchronization. The flag at the end of each frame terminates the check for transmission errors.

Both flags have the binary label 01111110. Any flag can be followed by another flag, a complete frame or an idle condition, which is a succession of more than 14 consecutive ONES. To reduce the possibility of error further, SDLC procedure requires that a ZERO be inserted by the transmitter after any succession of five ONES within a frame. Therefore, no flag pattern (which contains a succession of six ONES) can ever be transmitted by chance. After testing for a flag, the receiver removes all ZEROS that follow a received succession of five ONES.

The address field consists of the eight bits following the first flag. It is dedicated to the secondary station—that is, the address always refers to such a station. The primary station is never identified. The address field of a frame sent by the primary station is the address of the secondary station to which the frame is being sent. The address field of a frame transmitted by a secondary station identifies that station to the controller (primary station).

The C (command or response) field is made up of the eight bits that follow the 8-bit address field. It carries the commands and responses required to control the link.

The next field—the I field—contains data moved from place to place in the system. Its length is a multiple of eight bits, with the least significant bit sent first.

Finally comes the FCS field, which consists of eight bits transmitted immediately after the information field and directly before the ending flag. It contains the codes needed to perform cyclic redundancy checking.

The I field is optional. Since all other fields must be present, a valid SDLC frame contains at least 32 bits.

16-bit delay occurs when data are shifted through the 16-bit receiver-holding register (RHR). Again, if a flag is detected during the 16-bit delay, the receiver returns to the 8-bit delay state.

After the 24-bit delay, the next eight bits shifted into RMSK will cause the RBR to be loaded and the RBRL flag bit to be set. The receiver continues to load characters into the RBR register until another flag is detected, indicating the end of the frame. At this point, the RHRL flag and the RBRL flags are set.

The primary receiver takes the error-free frames sent by the secondary stations and stores them in continuous blocks of memory.

Under SDLC, a secondary station that is connected to a loop does not introduce the 1-bit delay until it detects an EOP character. Therefore, in this example, when the secondary stations are initialized, they assume the slave role pending configuration. For slave pending, the control word of the 9903 has bit 4 (CSL0) equal to 0 and bit 5 (CSL1) equal to 1. Register 8 is loaded with the address of routine PENDNG, and the receiver interrupt enabled. The receiver-interrupt service routine uses the content of register 8 to branch to the appropriate location.

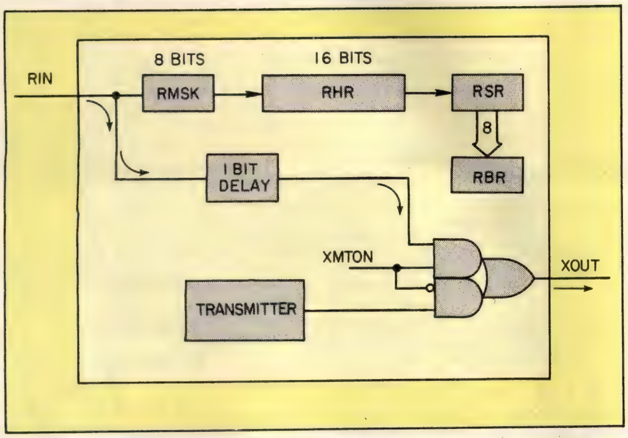
Routine PENDNG monitors the loop for an EOP (01111111) character. When an EOP is detected, the TMS 9903 automatically introduces a 1-bit delay and interrupts the CPU. The interrupt-service routine

TMS 9903 pin assignments

Label	No.	Input or output	Function
$\overline{\text{INT}}$	1	O	Interrupt. When active (low), the $\overline{\text{INT}}$ output indicates that at least one of the interrupt conditions has occurred.
XOUT	2	O	Transmitter serial-data-output line.
RIN	3	I	Receiver serial-data-input line.
CRUIN	4	O	Serial-data output line from TMS 9903 to CRUIN input line of the CPU.
$\overline{\text{RTS}}$	5	O	Request to Send output from TMS 9903 to modem. This output is enabled by the CPU and remains active (low) during data transmission from TMS 9903.
$\overline{\text{CTS}}$	6	I	Clear to Send input from modem to TMS 9903. When active (low), it enables the transmitter section of the TMS 9903.
$\overline{\text{DSR}}$	7	I	Data Set Ready input from modem to TMS 9903. This input generates an interrupt when going on or off.
CRUOUT	8	I	Serial-data-input line to TMS 9903 from CRUOUT line of the CPU.
V_{SS}	9	I	Ground reference voltage.
$\overline{\text{SCT}}$	10	I	Transmit clock—transmitter data are shifted out on one-to-zero transition of $\overline{\text{SCT}}$.
SCR	11	I	Receiver clock—receiver serial data (RIN) is sampled at zero-to-one transition of SCR.
S4(LSB)	12	I	Address bus SO-S4 is addressed by the CPU to select a particular TMS 9903 function.
S3	13	I	
S2	14	I	
S1	15	I	
S0(MSB)	16	I	
CRUCLK	17	I	CRU clock. When active (high), TMS 9903 samples the input data on CRUOUT.
$\overline{\phi}$	18	I	TTL clock.
$\overline{\text{CE}}$	19	I	Chip enable—when CE is inactive (high), the TMS 9903 address decoding is inhibited. CRUIN remains at high impedance when $\overline{\text{CE}}$ is inactive (high).
V_{CC}	20	I	Supply voltage (+5 V nominal).

For loop configuration, connect:

- CTS to $\overline{\text{RTS}}$ on each board
- XOUT of primary to RIN of secondary 1
- XOUT of secondary 1 to RIN of secondary 2
- XOUT of secondary 2 to RIN of primary
- Ground common to all TMS 9903
- SCR and $\overline{\text{SCT}}$ of all TMS 9903s, which are common, to an external pulse generator
- Select lines' CRU software base address of hex 180
- Interrupt to TMS 9901 with priority of level 4



5. An 8-bit delay occurs when RIN shifts through the RMSK register; the RHR adds a 16-bit delay. If a flag is detected in either register, the receiver returns to its previous state.

branches to routine PENDNG, which loads register 8 with the address for routine ADDRES and sets bit CSL0 of the TMS 9903 for the active-slave mode. (The transmitter must be on to introduce the 1-bit delay. It should be turned off before switching from slave pending to slave active.)

Register Frame is loaded with the address of routine ADDRES after leaving the pending mode. Routine ADDRES checks for a valid address. If not valid, the receiver is cleared and the interrupt bits are reset. After receiving a valid address, routine READF reads and stores the control byte and the I field.

Once out of the pending mode, the receiver monitors the loop for a frame with its address. Then it stores frames that are error-free and in proper sequence with its address. If the P bit is set, the receiver turns the transmitter on, and maintains a sequence of I-formatted frames. Finally, it exits the receiver routine after receiving the last frame from the primary station.

The secondary station has three SDLC modes: normal-response, normal-disconnect and command-reject. Register 7 is used for an indirect branch to the proper SDLC mode. Since Mode was initially loaded with the address of the NDM routine, the secondary station will initially enter the loop in the NDM mode.

Applications Report MP710, which provides additional information on applying the TMS 9903, may be obtained by writing to Texas Instruments, Literature Coordinator, M/S 6404, P.O. Box 1443, Houston, TX 77001. Or **Circle No. 319** □

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CIRCLE NO. 63

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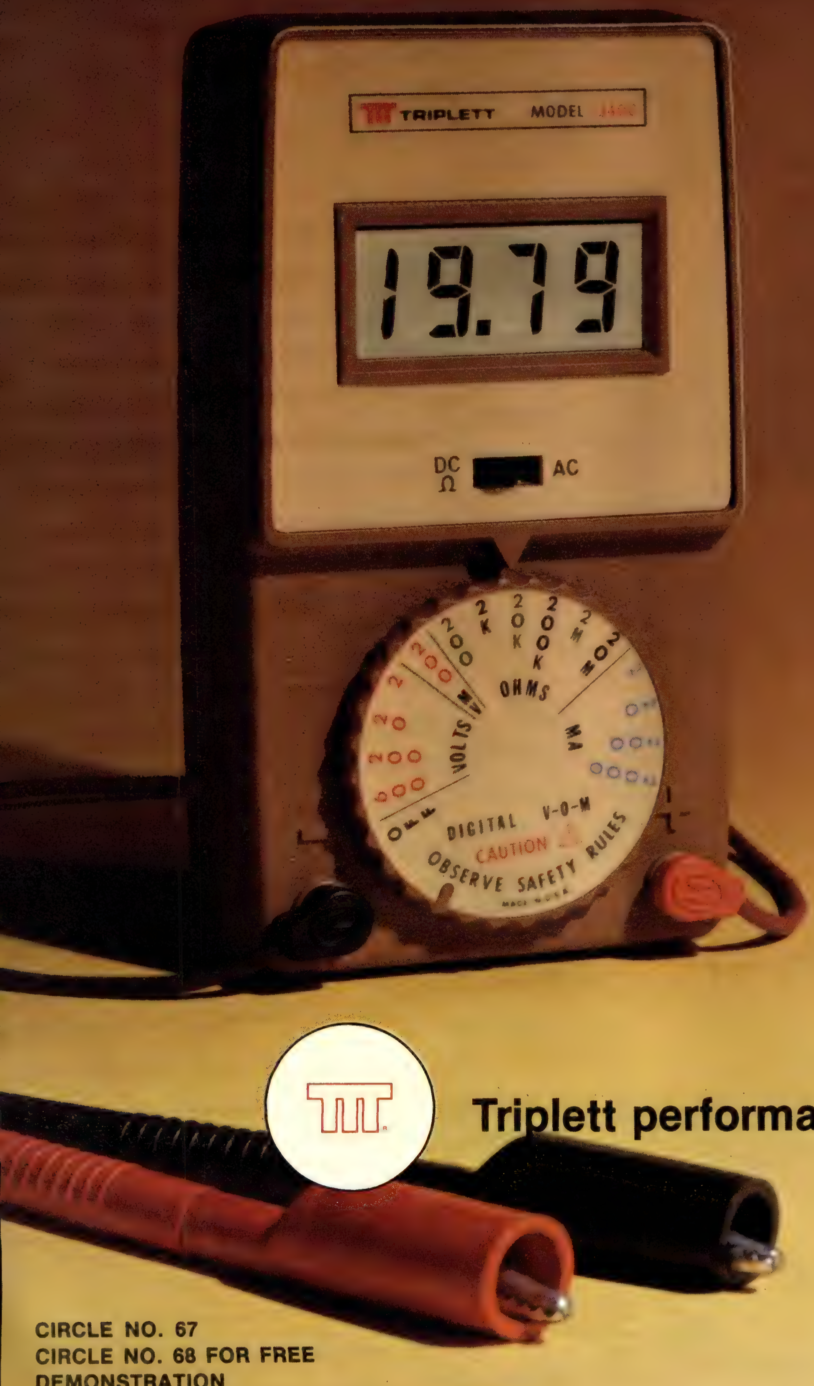

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CIRCLE NO. 67
CIRCLE NO. 68 FOR FREE DEMONSTRATION

Broadband phase-sensitive detector needs just five components

One op amp, two matched resistors and two solid-state analog switches assemble into a phase-sensitive detector for demodulating signals from ac servo components, such as synchros, resolvers and linear variable differential transformers. The detector typically operates from dc up to several tens of kilohertz.

The circuit was originally designed for detecting several modulated infrared sources with a single photodiode (Fig. 1). The amplified photodiode output is applied simultaneously to several detector circuits (connected for synchronous demodulation). Each demodulator has its own reference clock frequency to establish the relative magnitudes of the various IR sources (one level at each output).

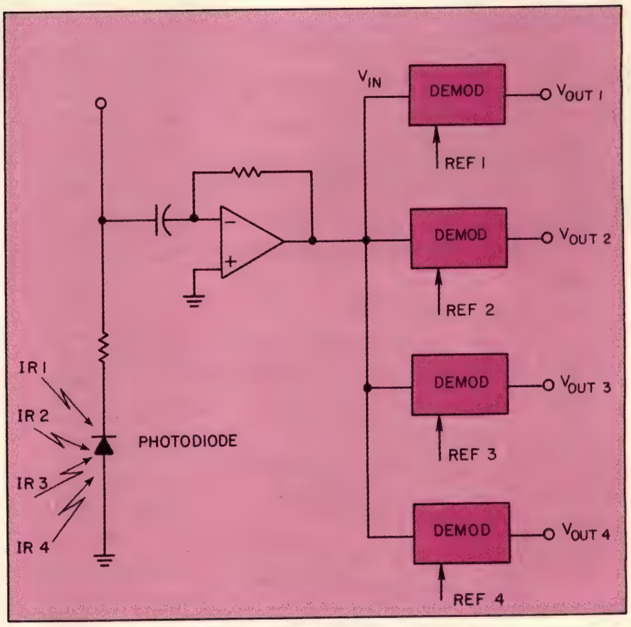
A look at the phase-sensitive detector itself (Fig. 2) shows that the Intersil IH5142 dual analog gate is controlled by a square-wave reference clock. When switch S_1 is closed and S_2 open, the amplifier is essentially a voltage inverter with a gain of $-R_1/R_2$. When S_1 is open, S_2 is closed; the overall gain is 1 irrespective of the resistors. Thus, the gain switches between $-R_1/R_2$ and 1. When $R_1 = R_2$, symmetrical synchronous detection results. It is assumed that the input signal port will be fed from a low-impedance source.

Circuit performance is insensitive to the on-resistance of the IH5142 switches. Although the level of V_{IN} is not critical, it should be about 1 V. Frequency of operation is ultimately limited by the analog switches' 80-ns minimum switching time. The op amp is noncritical and is selected to handle expected input signal amplitudes and maximum switching frequencies with a negligible slew rate.

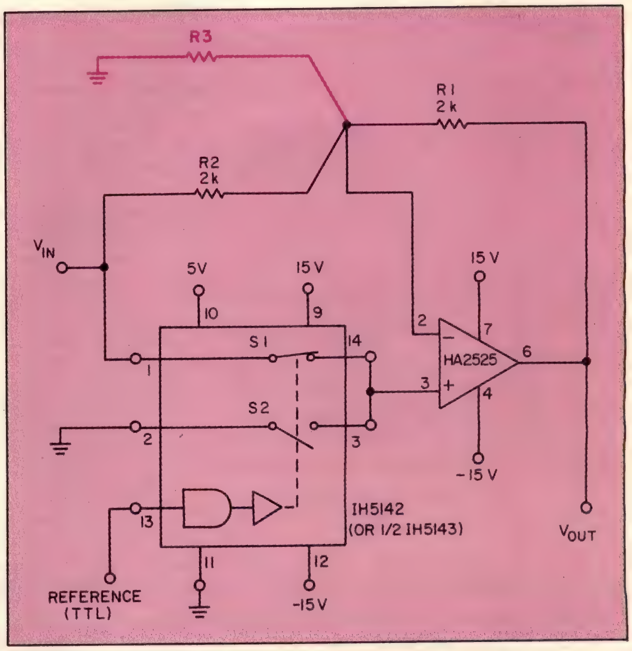
When a gain greater than unity is needed, resistor R_3 is added. Then, if $R_1 = KR_2$ and $R_3 = \frac{R_1}{K-1}$, the gain switches between K and $-K$. For the particular case where $R_1 = R_3 = 2R_2$, K is equal to 2. For $K > 2$, the necessary resistance values for R_2 and R_3 can be obtaind by series and parallel connection of single-valued resistors (preferably using a monolithic resistor network).

Yishay Netzer, Electrical Engineer, 21-A Kings Park Apt., Cherry Hill, NJ 08034.

CIRCLE NO. 311



1. Several modulated infrared sources are detected and demodulated by one photodiode and a series of synchronized demodulator circuits.



2. Since the HA2525's positive input always sees a low impedance, op amp input capacitance does not limit the detector's frequency response. Top-end performance is ultimately determined by the IH5142's switching time.

NOR gate unlatches pseudo random noise generator

Conventional seven-stage 127-period (maximum length) pseudo random noise generators implemented with CMOS logic can latch up in the all-ZERO state when power is initially applied. This problem is avoided entirely by adding a CD4078B eight-input NOR gate and one exclusive-OR gate to the conventional PN generator hookup (see Fig.). Since the conventional PN design calls for a 74C86 (a quad package of exclusive-OR gates), one of the three unused gates is simply adopted during circuit modification.

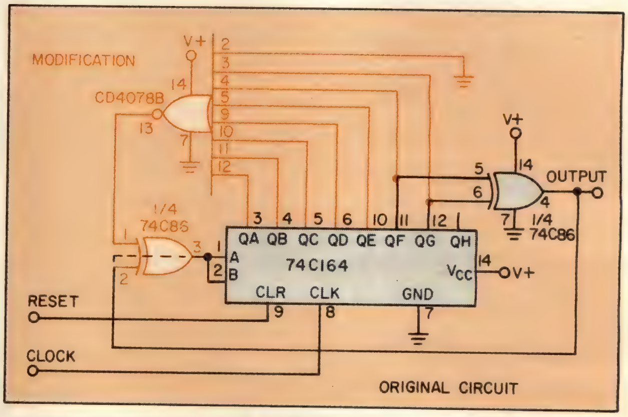
Normally, the PN generator produces a clean sequence of pulses. The parallel outputs of the 74C164 shift register repeat themselves every 127 states in sequence; thus, the "noise" is pseudo random. However, should the circuit latch up in the all-ZERO state, the shift register will continue clocking a feedback ZERO, and the output will stay in the ZERO state forever.

The CD4078B eight-input NOR gate (see schematic) decodes the state of the shift register. When an all-ZERO state is detected, the NOR gate output is a ONE. This ONE is exclusive-ORed with the feedback ZERO, producing a ONE into the shift register and initiating the desired pseudo random sequence. When the shift register is producing any of the 127 states that are not all ZERO (operating normally), the NOR-gate output is low and therefore has no effect on the feedback data.

An additional feature of this circuit is derived from the RESET line. The ongoing pseudo random sequence may be reset at any time, and the restarted from a known state (all ZEROs).

Chung M. Wong, Design Engineer, Ford Aerospace & Communications Corp., 3939 Fabian Way, MS-T97, Palo Alto, CA 94303.

CIRCLE NO. 312



The 74C164 shift register in this pseudo random noise generator can never latch up in the all-ZERO state because the CD4078B eight-input NOR gate (together with the 74C86) detects this unwanted condition whenever it occurs, and then initiates the desired pseudo random sequence.

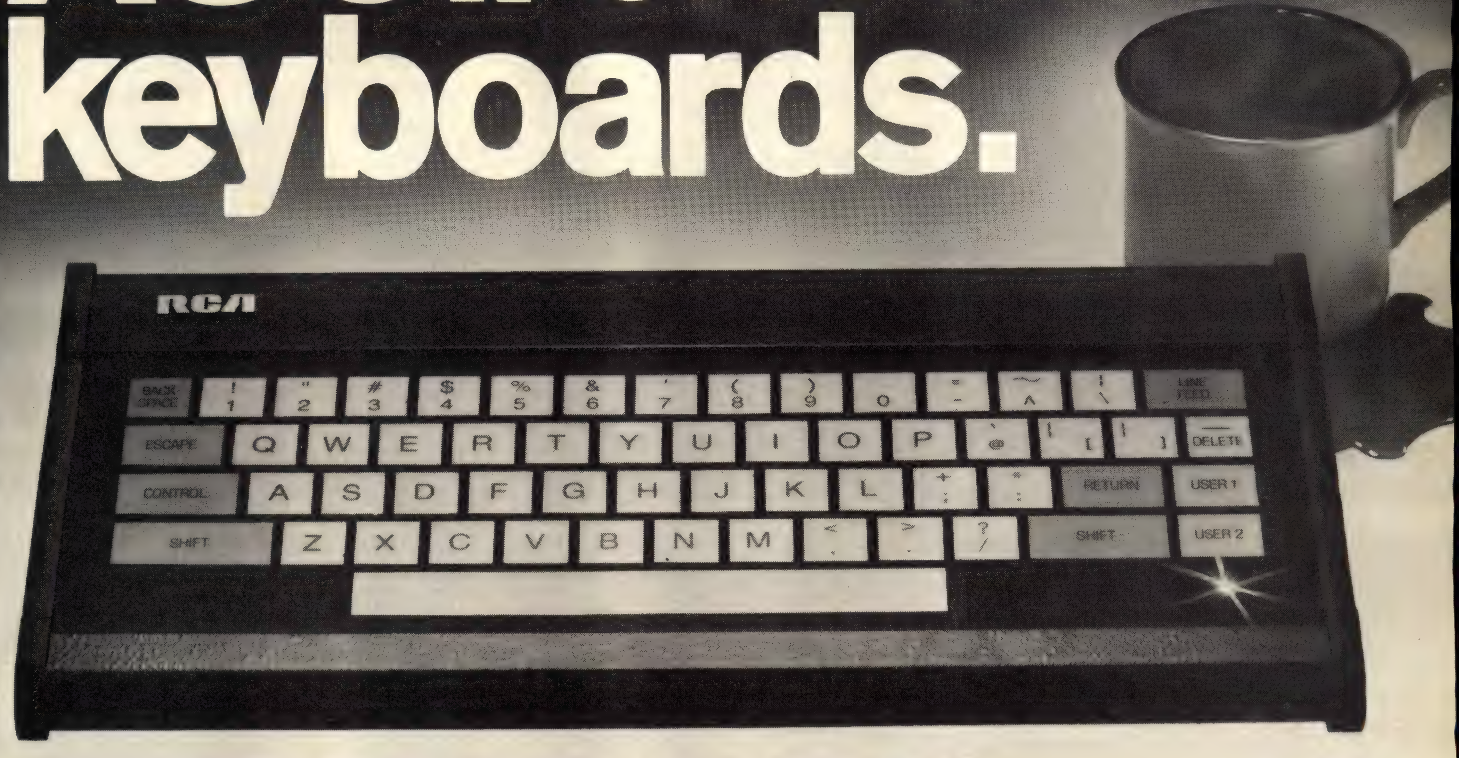
Differential amplifier design avoids op amps

A high-performance differential amplifier with zero offset can be implemented with an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). Unlike differential amplifiers made with op amps, the design maintains gain linearity and a high common mode rejection ratio (CMRR) without needing accurate closely-matched resistors or other precision components. The circuit (see Fig.) can replace standard high-performance instrumentation amplifiers in quasi-static analog applications (e.g. temperature controller) that demand long-term stability and absolutely minimal offset voltage.

The differential amplifier's input characteristics are determined by a TL500 analog-to-digital processor, which has 0.001% linearity, automatic offset zeroing, 90-dB CMRR and true differential input (with an impedance of 10^9 Ω). It draws about 50-pA bias current. A CD4040 counter, an oscillator (gates 1C-1D), a state decoder (gates 4A-4B-3A-3B-3C), a polarity flip-flop (6A) and a zero-crossing detector (1A-2A-5A)—together with the TL500—form a standard dual-slope ADC. It converts an analog signal into an 11-bit binary number (in sign and magnitude format) through a three-phase cycle (i.e., autozero, signal integrate and reference deintegrate).

The CD4040 handles 12 bits of data. The least-significant 10 bits represent data magnitude, and the most-significant 2 bits control the ADC phases: 00 for autozero, 01 for signal integration and 10 for reference deintegration. The unused portion of the

spillproof ASCII encoded keyboards.


RCA
BACK SPACE ! 1 " 2 # 3 $ 4 % 5 & 6 ' 7 (8) 9 0 = - ~ ^ | \ LINE FEED
ESCAPE Q W E R T Y U I O P ` @ { [}] DELETE
CONTROL A S D F G H J K L + ; * : RETURN USER 1
SHIFT Z X C V B N M < , > . ? / SHIFT USER 2

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Parallel output keyboard features:

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- 20-pin PC board header connector.

Serial output keyboard features:

- 3 ASCII encoded outputs: EIA RS232C compatible. 20 mA current loop. TTL.
- Switch-selectable data format.
- Six baud rates, switch-selectable.
- Power-on or "prompt" LED indicator.
- 25-pin output socket mates with male "D" cable connector.

RCA

*OEM price.

deintegrate phase is also used for auto-zero; one conversion cycle is exactly 3072 clock periods and is independent of the input voltage.

The AD7522 multiplying DAC provides a bipolar output. A floating 10-V power supply delivers the output reference signal to the DAC. Reference current direction is controlled by flip-flop 6B (drives switch SW1).

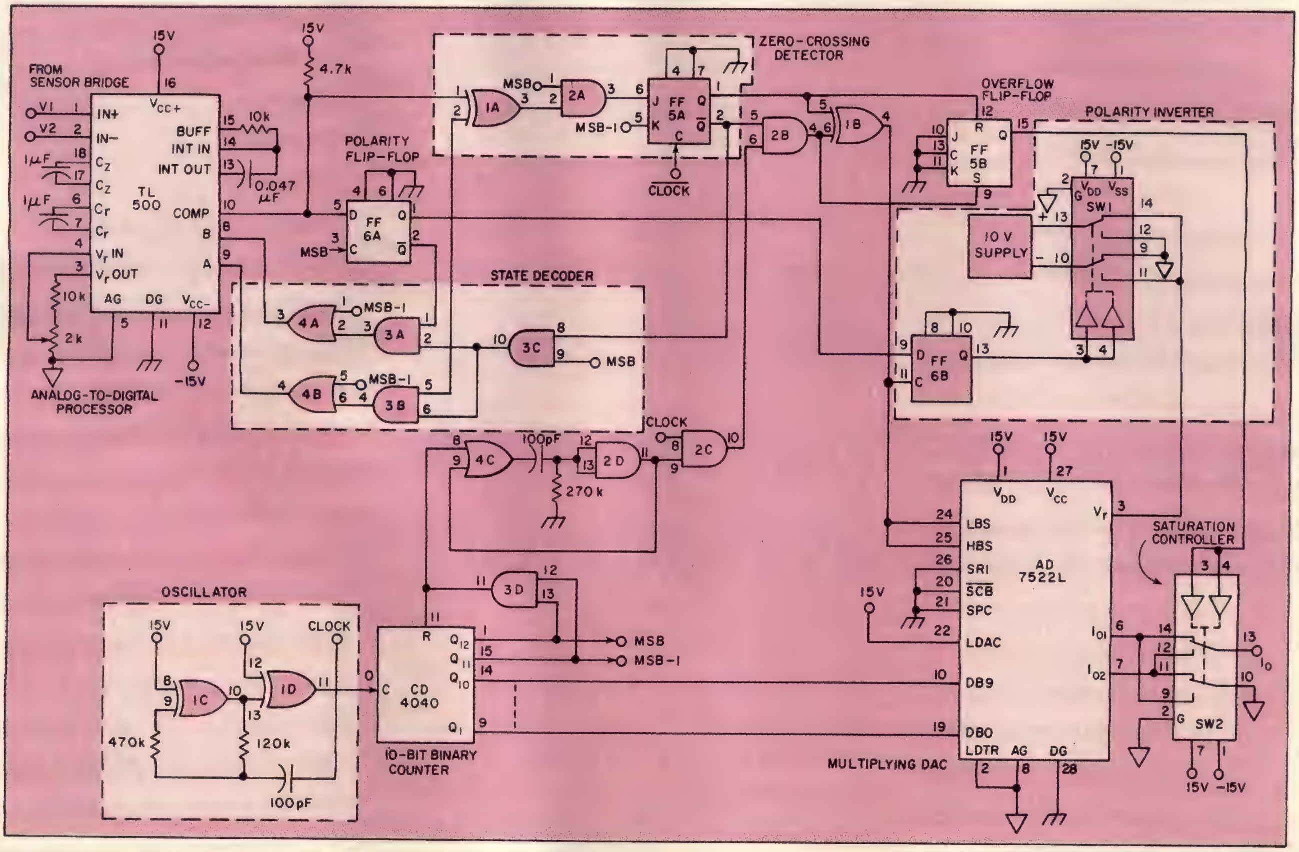
In case of overflow, flip-flop 5B causes switch SW2 to select the DAC's complementary output, giving the differential amplifier a "saturation" characteristic.

As shown, the oscillator (1C-1D) oscillates at approximately 36 kHz, so the system handles about 12 voltage samples/s internally. A higher oscillator frequency can be used for a faster data processing rate (signal integrate time should be a multiple of 60 Hz for maximum noise rejection).

Total component cost is only about $30. Where 8-bit accuracy without the bipolar output is sufficient the AD 7522 and AD7512 can be replaced by MC1408 and MC4053 (plus a few flip-flops), dropping the cost to $15.

L. Y. Hung, Consultant Engineer, 300 Tremont St., Boston, MA 02116.

CIRCLE NO. 313



This differential amplifier's offset voltage is continuously monitored and compensated for, eliminating the manual offset adjust that op-amp instrumentation amplifiers require to set their initial accuracy. The true differential input and high linearity of the TL500 eliminates the need for expensive precision resistors.

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CIRCLE NO. 74

Products

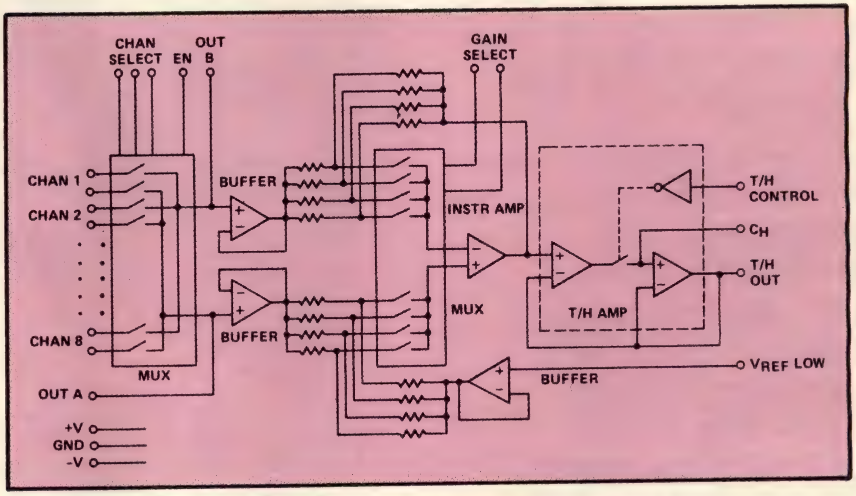
Up to now, hybrid circuits for data-acquisition systems have taken up large PC board spaces. A new hybrid system approximates DIP dimensions.

Two hybrids make hi-rel, 12-bit data-acquisition system

While hybrid packaging is an effective way to build high-performance data-acquisition systems, hybrid-circuit packages are often too big for tight PC-board layouts and, in the event of failure or test irregularity, they are not easily repaired. Now, however, a complete multichip data-acquisition system from Harris Semiconductor Products Division comes packed in two ceramic DIPs.

The system consists of the multichip HI-5900 analog data-acquisition signal processor with 50-kHz sampling rate and the multichip HI-5712 12-bit, successive-approximation a/d converter with an 8-μs conversion time. The HI-5900 includes of an eight-channel differential multiplexer, a high-impedance buffer amplifier, an instrumentation amplifier with selectable gains of 1, 2, 4 and 8, slew rate of 4 V/μs, full power bandwidth of 70 kHz, and 85 dB of common-mode rejection, a resistor network for programming the amplifier, and a track-and-hold amplifier. The HI-5900 offers a total gain error typically less than 0.17%, and is available in a 32-pin ceramic DIP with 0.100 × 0.610-in. pin spacings.

The HI-5712, in addition to 8-μs conversions, features a precision d/a converter (HI-562) with a 300-ns settling time, a precision +10-V reference (HA-1610), a comparator (HA-4950) with 100-μV overdrive and 100-ns settling time along with a clock, a successive-approximation register and three-state data latches—all in a 40-pin ceramic DIP.



The HI-5900 section of the system includes buffer amplifiers, an eight-channel differential multiplexer and a programmable gain amplifier.

Together with the successive approximation register, these chips provide a high-performance a/d converter sporting 8-μs conversion time, a nonlinearity within ± 1/2-LSB, and three-state outputs, for interface with 8, 12 or 16-bit μP systems.

All the chips in both hybrids are connected in the devices, on both the top and underside of the ceramic substrate, using low-profile leadless chip carriers. This provides easy construction, safe operation through the entire operating temperature range from −55 to +150 C, and easy chip replacement, if necessary. In addition, each chip is environmentally sealed and tested according to MIL-STD-883, Method 5004/Class B, before assembly on the substrate. The result is suitable for military hardware, space shots and other high-reliability data-acquisition systems.

Prices for the HI-5900 are in the neighborhood of $100; $200 for the HI-5712, both in lots of 100. Production quantities of both parts will be available in July.

Harris Semiconductor Products Div., P.O. Box 883, Melbourne, FL 32901. Leo Enriquez (305) 724-7549. **CIRCLE NO. 309**

Stephan Ohr, Components Editor

6800

THE 6800 STORY IN TWO GUIDES IDEAL FOR HOBBYISTS

BASIC MICROPROCESSORS AND THE 6800 by Ron Bishop. Here is the first truly complete beginner's guide to microprocessors. It starts at ground zero with the basic fundamentals of microprocessors that must be mastered before any microcomputer system is learned. Then, it goes on to describe in detail the M6800 microcomputer system. Sample flowcharts and programs are found throughout, with extensive problem sections at the end of each chapter. #0758-2, paper, $12.90.

THE 6800 MICROPROCESSOR: A Self-Study Course with Applications, by Lance A. Leventhal. This is an ideal manual for hobbyists to gain hands-on experience with the 6800. Fifteen self-paced, increasingly complex laboratory exercises emphasize the use of the microcomputer as a controller. Flowcharts and examples are used throughout. #5120-4, paper, $8.60.

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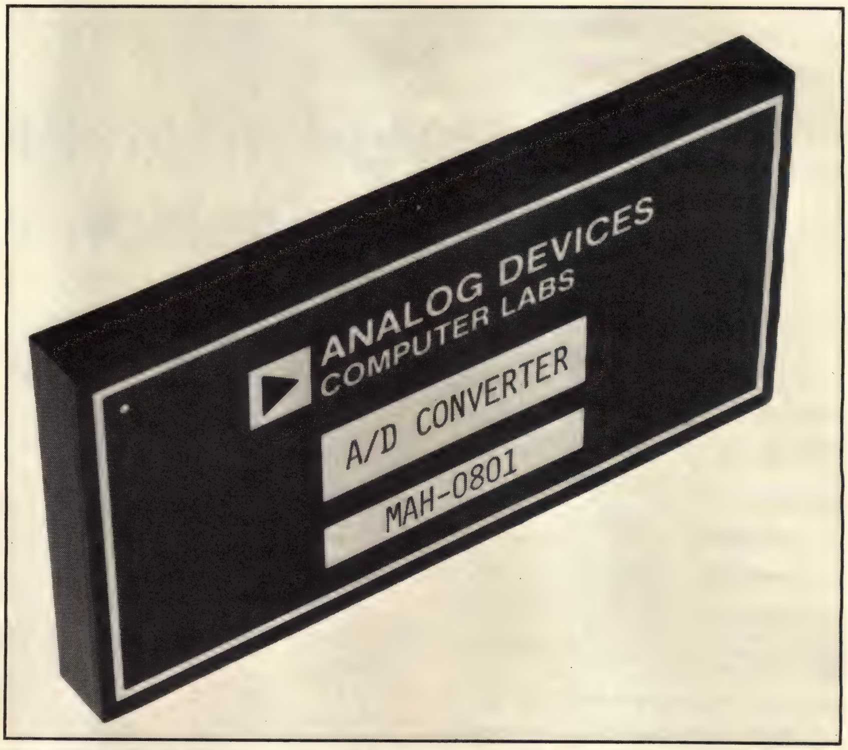


This 750-ns, 8-bit a/d converter module combines a maximum differential nonlinearity of ±1/4 LSB with a single-unit price of $195.

By using its own 12-bit precision HDS-1250 d/a converter instead of discrete components and thick-film resistor networks, the Computer Labs Division of Analog Devices offers successive-approximation a/d-converter modules that are more than just cost-effective replacements for popular Teledyne-Philbrick, Datel-Intersil and Dynamic Measurements models. The MAH-0801 8-bit, 750-ns and the MAH-1001 10-bit, 1-μs modules routinely provide superior linearity.

The 4.0 × 2.0 × 0.4-in. MAH-0801 and MAH-1001 are pin-compatible with Teledyne-Philbrick's 4130/4131 modules, Datel-Intersil's ADC-G8/G10 and Dynamic Measurements' 2800 series. The MAH-0801, however, provides a maximum differential nonlinearity of ±1/4 LSB (±1/8 LSB typical), while the MAH-1001 provides a differential nonlinearity well within ±1/2 LSB (±1/4 LSB typical). The pricing is also attractive: $195 for the MAH-0801 and $219 for the MAH-1001, both in single-lot quantities.

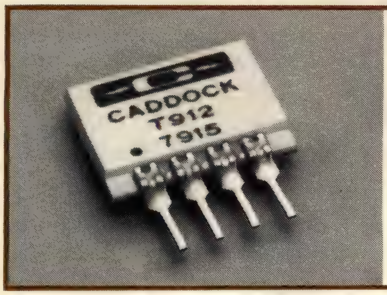
The modules require only on analog power supply (±15 V), a logic supply (+5 V), an external gain-adjustment pot or trimmer, and an external offset-adjustment trimmer. The unipolar offset drift is well within ±10 μV/°C or ±15 ppm/°C for bipolar units. The gain temperature coefficient is less than ±20 ppm/°C.

The a/d converter modules are available from stock.

Computer Labs, Div. of Analog Devices, 505 Edwardia Dr., Greensboro, NC 27409. Edward Graves (919) 292-6427.

CIRCLE NO. 305

Precision Resistance Ratios from Caddock .... and more!



Caddock's Type T912 Precision Resistor Network is the cost-effective replacement for discrete resistor sets.

The ratio characteristics of these high-stability resistor networks make them ideal for applications in precision amplifier circuits, voltage reference circuits and precision bridge circuits.

- **Ratio Tolerances from ±0.1% to ±0.01%.**
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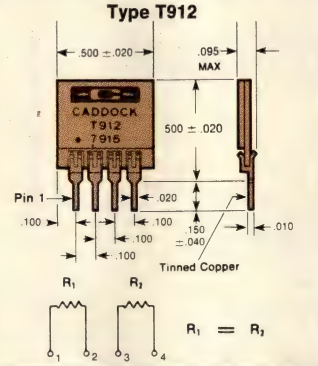
Tetrinox™ — Caddock's unique high-resistance film — provides resistance values from 5 kohm to 2 Megohms in this package size.

Custom models with unequal values can provide resistance ratios as high as 250:1 and values from 1 kohm to 2 Megohms.

Type T912



Standard Type T912 and T914 Precision Resistor Networks

Standard Resistance Values:

5K	50K	500K
10K	100K	1 Meg.
20K	200K	
25K	250K	
40K	400K	

Special or mixed resistance values *are available as custom networks.*

Ratio Tolerance:
Maximum ratio difference between any two resistors in the network.

-100 = 0.10%
-050 = 0.05%
-020 = 0.02%
-010 = 0.01%

Ratio Temperature Track:
Ratio Temperature Coefficient between any two resistors in the network from 0°C to +70°C

-10 = 10 PPM/°C
-05 = 5 PPM/°C
-02 = 2 PPM/°C

Ordering Information:

To specify any of the standard Type T912 and T914 resistor networks, use this model number.

T912 - 500K - 010 - 02

Model No.
Resistance Value *
Ratio Tolerance *
Ratio Temperature Track *

* (This information appears on the back side of the network)

The standard models of Type T912 resistor pairs and Type T914 resistor quads can be delivered in prototype and production quantities from stock to within 6 weeks ARO.

For additional technical information — and immediate confirmation of price and delivery on initial quantities — call or write directly to:

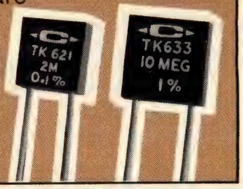
Caddock Electronics, Inc.,
3127 Chicago Ave., Riverside, Calif. 92507
Tel: (714) 683-5361

CADDOCK
HIGH PERFORMANCE FILM RESISTORS

In addition to the Type T912 and Type T914 Precision Resistor Networks shown here, Caddock Electronics is in volume production on many other types of precision discrete resistors and resistor networks:

Type TK Temp-Stable Precision Film Resistors

These .250" and .300" square discrete resistors are rated at .3 and .4 watts, and deliver TCs better than 10 PPM/°C from -55°C to +125°C.

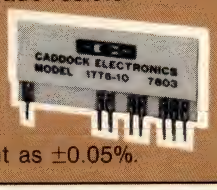


Type TF Low TC Ultra-Precision Film Resistors

Tolerances as tight as ±0.01%, values from 1 kohm to 10 Megohms and a TC better than 15 PPM/°C make the Type TF resistors the ideal replacement for expensive wire-wound resistors.

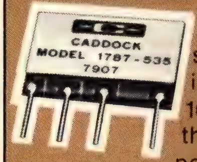
Type 1776 Precision Decade Resistor Voltage Dividers

25 standard models of these three-, four- and five-decade resistor networks provide values up to 10 Megohms and ratio tolerances as tight as ±0.05%.



Type 1787 Current Shunt Resistor Networks

For accurate current sensing in multi-range instruments, there are 16 standard models of the Type 1787 resistor networks with values between 1 ohm and 1000 ohms and tolerances as tight as ±0.02%.



To receive complete technical information on all of these high stability precision resistors, call or write directly to the applications engineering group at Caddock Electronics, Inc.

CADDOCK
HIGH PERFORMANCE FILM RESISTORS

For T912 and T914 data, Circle No. 76

For Caddock's General Catalog, Circle No. 215

6-bit DAC has voltage output

On the bipolar chip of its latest d/a converter, Precision Monolithics Inc. implants a buried zener reference—so the DAC-206 can provide pin-selectable bipolar or unipolar voltage outputs.

The 6-bit converter provides a unipolar output of 0 to 10 V, or bipolar output of ±5 or ±10 V, with a dual power supply input from ±12 to ±18 V.

The easy-to-use converter comes in a 14-pin mini-DIP, accepts TTL or DTL-level digital inputs and settles to ±1/2-LSB within 3 μs. Since the DAC provides 7-bit accuracy and a sum-node pin, the resolution can be extended to 7 bits by adding a few external resistors and diodes.

Packaging options include ceramic for industrial and MIL-spec applications (−55 to +125 C) and plastic for commercial applications (0 to 70 C). In lots of 100, industrial versions cost as little as \$10 and commercial versions cost from \$3.75. Delivery is from stock to several weeks.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, CA 95050. Russ Schroy (408) 246-9222. **CIRCLE NO. 369**

Melody IC plays two songs

Tune-playing, alarm-sounding melody ICs, Series 7910, play up to two complete, 128-note songs. The chips are available separately or installed on a circuit board with components for battery operation, tune/alarm selection and volume/tone control. Eight different versions are offered with such songs as Green Sleeves, Holidilia, two minuets, Dark Eyes, Home on the Range, Mary had a Little Lamb, Camptown Races, two Japanese children's songs and Westminster chimes. In addition to alarm sounds, a doorbell chimes is also available. Series 7910 devices are CMOS units packaged in 16-pin DIPs. A preamplifier is built-in. Series 7920 ICs play only one 64-note tune and have no preamplifier. Series 7930 devices are the same as the Series 7920, but have a built-in preamplifier.

Epson America, 23844 Hawthorne Blvd., Torrance, CA 90505. (213) 378-2220. \$5.00 (IC); \$14.00 (board). **CIRCLE NO. 320**

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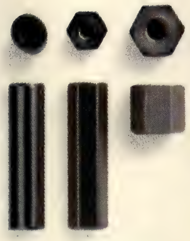
CIRCLE NO. 77



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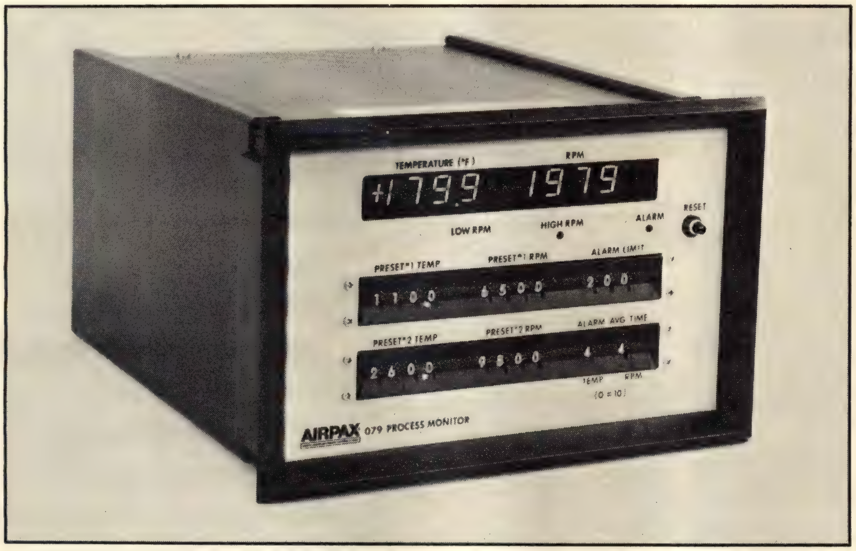
CIRCLE NO. 78

Process monitor balances complexity and cost



The Airpax 079 μP-based industrial controller comes with 8½ digits of front-panel display and thumbwheel switches for determining set points and alarm limits.

Industrial processes such as motor speeds, flow rates and temperatures can be monitored by standard equipment for a reasonable price. But calculating complex relationships between these variables and displaying the results in an easy-to-read format has been virtually impossible without expensive, specially designed process-monitoring equipment. Now, however, there is a cost-effective solution: The microprocessor-based Airpax 079.

Airpax configures and programs the 079 for each application. At the core is an Intel MCS-48 8-bit μP with up to 8 kbytes of EPROM and 2 kbytes of RAM. Data are entered through a choice of specially configured I/O cards. The information being monitored is displayed on 8 1/2 LED digits on the front panel. Additional monitoring flexibility—the ability to select information being displayed or to select process set points—is provided by front-panel thumbwheel switches. Outputs from the 079 can be used for limit-setting functions on other process-control equipment.

Configurable I/O options include two and four-channel tachometer input cards, which accept sine waves and TTL logic pulses from magnetic pickups. Analog-input cards accept up to six channels of standard 4-to-20-mA industrial signals. Relay cards with DPDT and SPDT devices, and special accumulator cards for up/down counting operations are also included. Additional I/O options include a communications card with transmit and receive channels for data in an RS-232 format, and a DIP Switch card for entering binary-coded-decimal data.

The Airpax 079 costs $3500 to $5000, depending on the application, the programming and the enclosure options selected. Delivery takes eight to 12 weeks.

Airpax Div. of North American Philips Controls Corp., 6801 W. Sunrise Blvd., Fort Lauderdale, FL 33313.

CIRCLE NO. 411

if someone beat you to the B&K-PRECISION 16 page oscilloscope selection guide

that was in this copy of Electronic Design, don't get upset!

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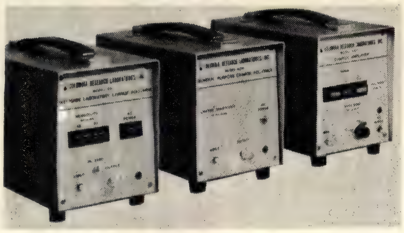
CIRCLE NO. 79

Charge amps permit sound/pressure tests



A line of charge amplifiers, 4100 series, operates with all piezoelectric sensors for dynamic pressure, vibration, shock, high-intensity sound, force and weight measurements. A charge follower, Model 4101, has a dynamic measuring capability of better than ±1 to ±10,000 pcmbs at the input. A charge amplifier, Model 4201, is equipped with a dial-gain adjustment to normalize any transducer sensitivity so that readout can be made directly in terms of full-scale output. Model 4301 is a charge follower for shock, pressure blast and sudden load work.

Columbia Research Laboratories, MacDade Blvd.& Bullens Lane, Woodlyn, PA 19094. (215) 532-9464. **CIRCLE NO. 321**

Wattmeter measures with precision

A lightweight, battery-powered wattmeter, TIF 2000, displays readings on its 3-1/2 digit LCD readout. Pointed-jaw design allows access into tight places. The clamp accepts 1-1/4 in. conductors. The unit operates on 90 to 250-V, single-phase lines. Low range measures 10 W to 20 kW with 10-W resolution. High range shows 100 W to 200 kW with a 100-W resolution. The instrument housing is ABS plastic. Two voltage probes, a battery and a carrying case are included.

TIF, 3661 N.W. 74th St., Miami, FL 33147. (305) 696-7100.
Electro: 1816 **CIRCLE NO. 322**

Meter monitors solution conductivity

A solution conductivity meter, Type 860, monitors process water, plating baths and other solutions. The unit is offered with an analog meter readout and setpoint control options. The meter accepts input from one of two, front-panel selectable, temperature-compensated probes. Solution conductivity is displayed in one of eight specifiable sensitivity ranges. Conductivity is also compared with a front-panel selectable setpoint. Drift of conductivity above or below a setpoint energizes a rear-panel accessible DPDT relay.

Thornton Associates 87 Beaver St., Waltham, MA 02154. (617) 899-1400. $315. **CIRCLE NO. 323**

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Canada: Montreal (514) 482-5520 • Toronto (416) 291-4401 • Vancouver (604) 278-7636 • **International:** Oak Brook, Illinois TELEX 206-054

CIRCLE NO. 81

Stand-alone instrument emulates the Z8000

In-circuit emulator for the Z8000 has two RS-232C ports; it can, therefore, operate with any development system that has the right software and an RS-232C port.

The first in-circuit emulator for the Z8000 is a stand-alone unit with its own monitor and debug software, which it executes on its own Z8002 microprocessor.

Because the ZSCAN emulator has two RS-232C ports, it can run on any microprocessor development system that has appropriate cross-assemblers and compilers and an RS-232C port. With its two ports, the emulator can stand between the host system and a CRT. It receives downloaded program code from the host system and supplies executed code in return.

The emulator can be configured for direct communication between the host system and CRT or for communication with the CRT alone. In the latter case, the target system would have to contain its program in PROM.

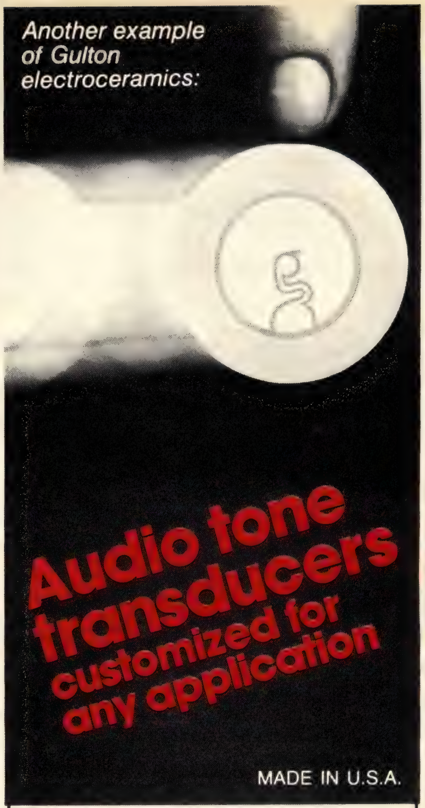
The emulator has two counters for keeping track of the number of times an event occurs and the number of operation-code fetch cycles made by the CPU. The counters facilitate the scanning of memory for n occurences of an event.

The ZSCAN also contains 4 k of static RAM, which can be mapped to any location in the target system memory, and up to 8 Mbytes of monitor memory. A software feature of the emulator makes the monitor memory a "shadow" to the target system storage space. Thus, the emulator can be controlled by a single Z8000 for both monitor and debug functions. None of the target system's memory space is needed for monitor operations.

For easing debug operations, the emulator has an unusual trace feature. It produces an address and data printout on a group of traced addresses and can then list the contents of all CPU registers for each address location collected. On other emulators, a comparable register listing requires a breakpoint operation, in addition to the trace.

Zilog, 10460 Bubb Rd., Cupertino, CA 95014. Ronald P. DeJong (408) 446-4666.

CIRCLE NO. 301



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CIRCLE NO. 83

Handheld multimeter ranges automatically

Microprocessor-controlled 3 1/2-digit multimeter measures ac and dc voltage and current plus resistance and displays the results on its 0.5-in. liquid-crystal display.

Designed to provide the convenience of autoranging without the slow "hunting" action associated with first-generation units, the B&K-Precision Model 2845 is a handheld digital multimeter with a built-in microcomputer. The 3 1/2-digit meter has a basic dc measurement uncertainty of 0.1% of reading ±1 count. It measures ac and dc voltage, ac and dc current, and resistance.

The microcomputer controls the meter's autoranging, giving the ability to skip ranges, when appropriate, for enhanced speed.

The 2845 is particularly well protected against overloads, being able to withstand +1000 and −450 V dc or 300 V ac on its resistance ranges. The ac and dc voltage ranges can take up to 1000 V dc or peak ac. A metal-oxide varistor and a fuse complete the defenses against overloads.

To save time in the making of continuity tests, the meter has an audible-tone generator that makes it necessary to look up to determine that a circuit is closed.

The 2845 complies with UL 1244 and is supplied complete with test leads, a tilt stand, an operating manual, and a spare fuse.

B&K-Precision, Dynascan Corp., 6460 w. Cortland St., Chicago, IL 60635.

CIRCLE NO. 414

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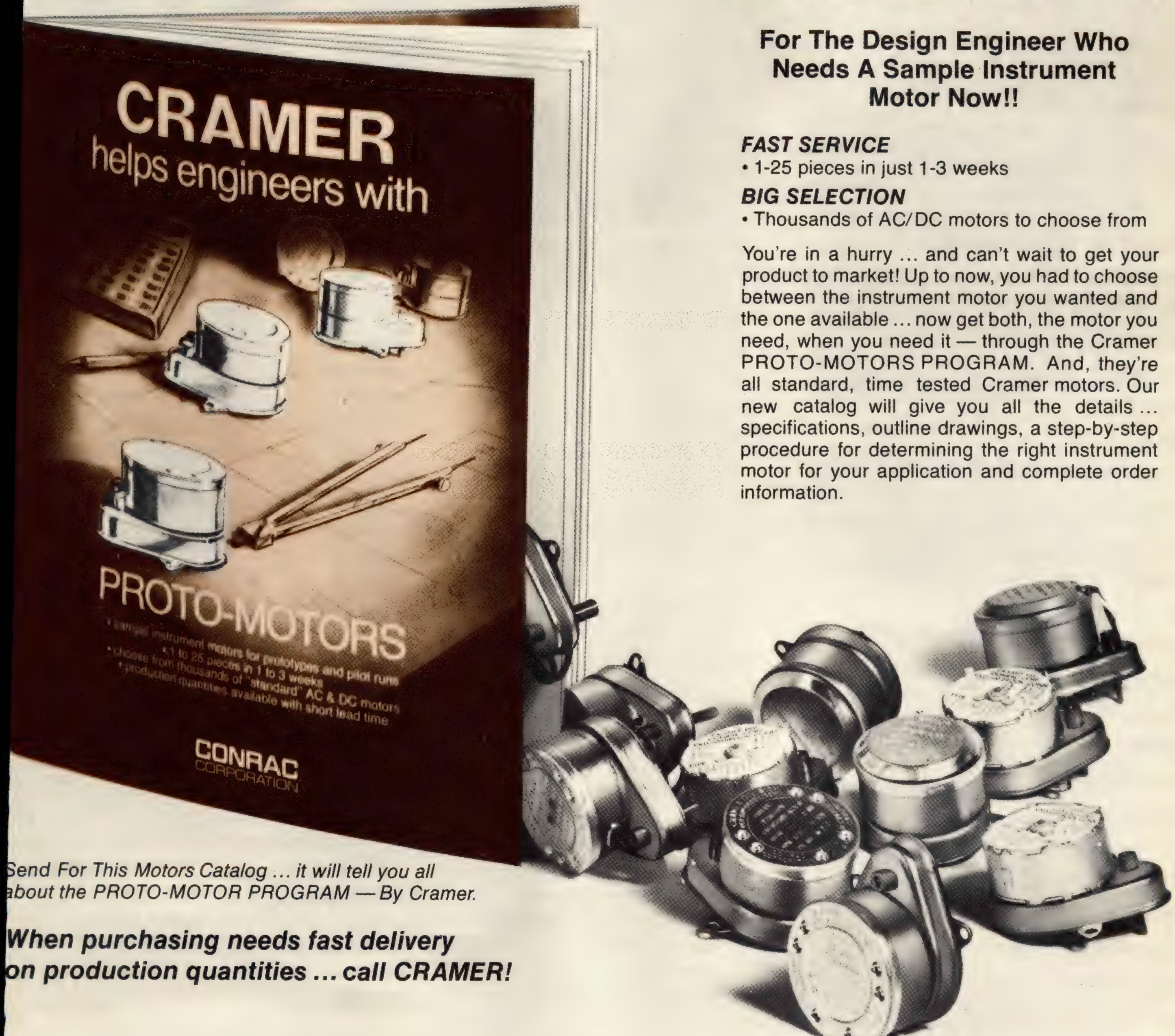

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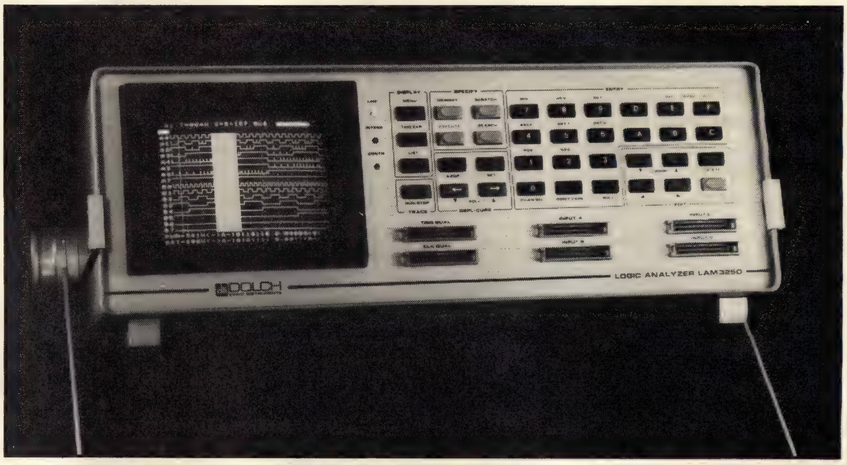
CIRCLE NO. 84

Logic analyzer premieres with 32-channel timing



Its word-search feature allows the 50-MHz LAM 3250 to count the occurrences of a user-specified keyword and to display the word in context.

As digital systems get more complex, designers need more capable instruments to monitor them. Dolch's latest, which is being marketed in this country by Kontron Electronic Inc., is the LAM 3250—the first 32-channel logic analyzer to offer 32-channel timing capability.

Another first for the 50-MHz analyzer is its word-search feature. The operator specifies a keyword for which the instrument is to search. After its trace memory fills, the analyzer counts the occurrences of the word within the memory and then displays the first occurrence of the word as the left-most vertical bits on the CRT display. (The memory can store 1024 32-bit words or 2048 16-bit words.)

The operator can then advance the display to the next occurrence of the keyword. In this way, the operator follows the sequence of events surrounding the keyword. For example, if the keyword were the starting address of a subroutine, the operator could tell which software program made each call to the subroutine and what parameters it used in order to do so.

Another plus for the unit is its programmability. The analyzer can store six independent menu procedures in nonvolatile CMOS RAM—the unit has a battery backup pack. Each menu procedure allows the operator to set up recording, triggering and comparison parameters of the logic analyzer. In addition, the menus can be accessed in string fashion, which allows for fairly complex programming.

The analyzer accepts 24 or 40-input trigger words. The 40-input trigger word contains 32 bits of trigger word and eight qualifier bits. The wide trigger word lets the analyzer easily handle 16-bit microprocessor-based systems. In addition, the user can apply four sequential triggering levels to select, dissect and isolate a faulty piece of software among several nested routines.

The LAM 3250 costs $7995; deliveries will begin in June 1980.

Kontron Electronic Inc., 700 S. Claremont St., San Mateo, CA 94402. Keith Barnes (800) 227-6854 or (415) 348-7291.

CIRCLE NO. 306

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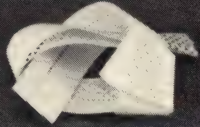

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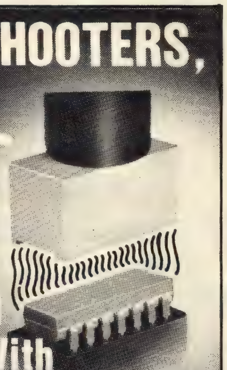

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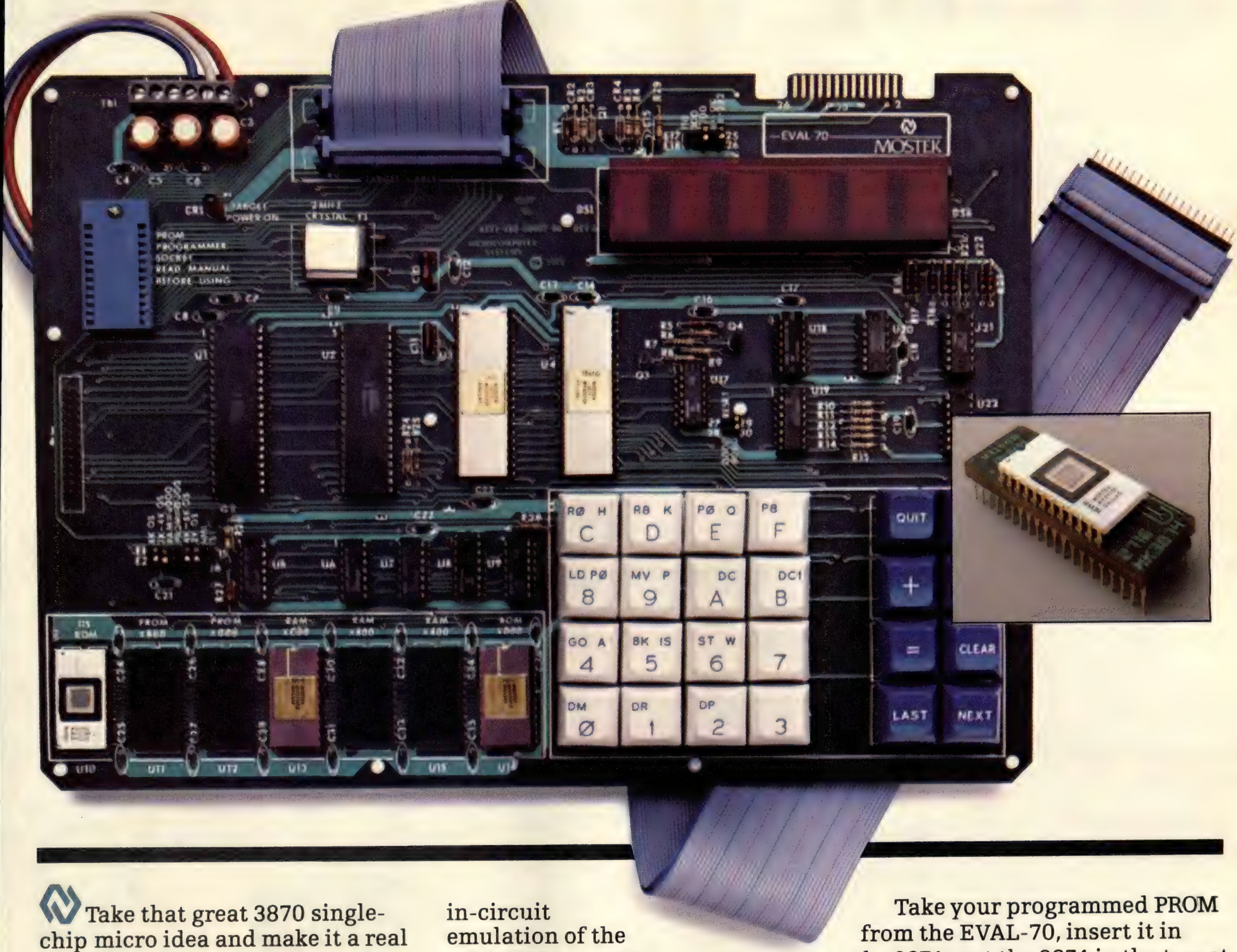
CIRCLE NO. 85

Field test your 3870 design for under $600.



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MK3874 is our piggyback EPROM single-chip microcomputer with the same architectural features, pinouts and I/O lines as other 3870 family members. Using 24-pin EPROMs, the 3874 can address 1K, 2K or 4K bytes of memory, for ideal 3870 family prototyping, testing or low volume production.

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An inexpensive yet powerful combination: the EVAL-70 is $499; an MK3874 without PROM is $92.

See both at your Mostek distributor. Or contact Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; phone 214/323-6000. In Europe, Mostek Brussels; phone 660.69.24.

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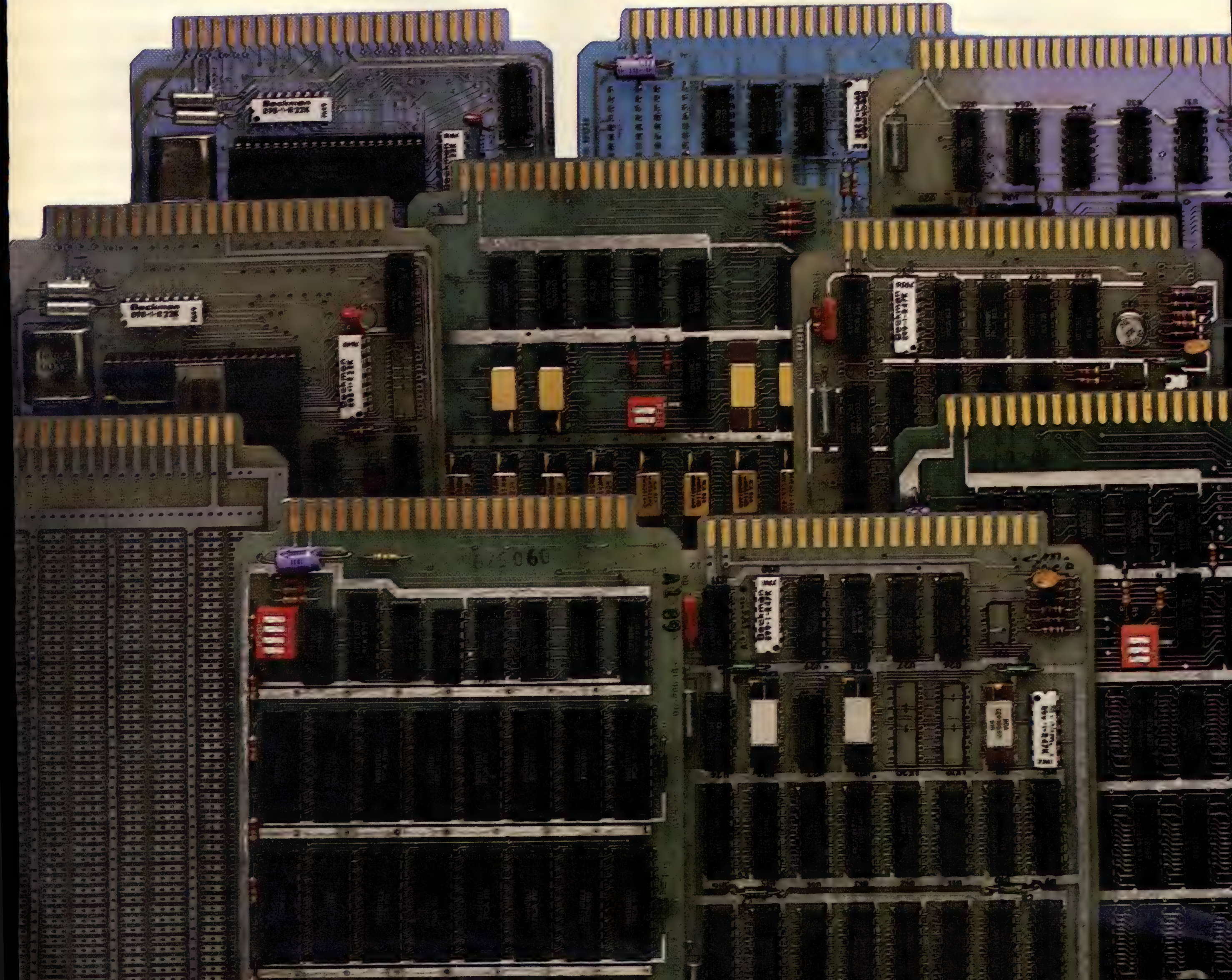
CIRCLE NO. 86

CMOS takes another giant step against NMOS.

RCA adds 12 new Microboards now, 7 more by the end of 1980.



RCA CMOS Microboards consume far less power (7.0 milliamperes), give off far less heat, and provide more functions in less space (4.5 x 7.5 inches) than any NMOS board on the market. And at competitive prices.

With 17 boards available now (24 by 4th quarter 1980) plus a range of chassis and accessories, RCA can provide a CMOS system to suit a wide variety of applications.

Microcomputer boards.

CDP18S601	Microboard Computer w/4K CMOS RAM, 4K/8K ROM/PROM sockets, serial I/O port, 20 programmable parallel I/O lines
CDP18S602*	Microboard Computer w/2K CMOS RAM, 2K/4K ROM/PROM sockets, UART, parallel I/O port
CDP18S603	Microboard Computer w/1K CMOS RAM, 4K/8K ROM/PROM sockets, serial I/O port, 20 programmable parallel I/O lines
CDP18S604*	Microboard Computer w/512 bytes CMOS RAM, 1K/2K ROM/PROM sockets, parallel I/O port

Memory boards.

CDP18S620	4K Static CMOS RAM
CDP18S621	16K Static CMOS RAM
CDP18S621V1	16K Static CMOS RAM
CDP18S622	8K Static CMOS RAM/ Battery backup
CDP18S623	8K Static CMOS RAM
CDP18S624	4K Static CMOS RAM/ Battery backup
CDP18S625	8K/16K ROM/PROM

Combination memory I/O.

CDP18S660	40 I/O Lines, 2K CMOS RAM, 4K/8K ROM/PROM sockets

I/O boards.

CDP18S640	Control/Display Module
CDP18S641	UART Interface
CDP18S642	12 Bit D/A Converter
CDP18S643	12 Bit A/D Converter
CDP18S644*	8 Bit A/D-D/A Converter
CDP18S646*	Parallel I/O
CDP18S649*	LCD Interface/Display
CDP18S661V1*	Video-Audio-Keyboard Interface
CDP18S661V3*	Video-Audio-Keyboard Interface (PAL Version)

Chassis and accessories.

CDP18S023V1	5 Volt Power Converter (100 V, 50-60 Hz)
CDP18S023V3	5 Volt Power Converter (220 V, 50-60 Hz)
CDP18S480	PROM Programmer
CDP18S502	Extender Card
CDP18S659	Breadboard w/prewired power and ground
CDP18S670*	25 Card Chassis w/power supply
CDP18S675	5 Card Naked Chassis
CDP18S676	5 Card Chassis w/Case

Prototyping systems.

CDP18S691	Microboard Prototyping System with CDP18S601 Computer Board
CDP18S692*	Microboard Prototyping System with CDP18S602 Computer Board

Full design support.

RCA Microboards are backed up by a complete line of hardware and software compatible development systems.

Plus 38 RCA "Systems Appointed Distributors" offer technical assistance, systems demonstrations, and off-the-shelf delivery.

A complete list of RCA Systems Appointed Distributors appears on the following page.

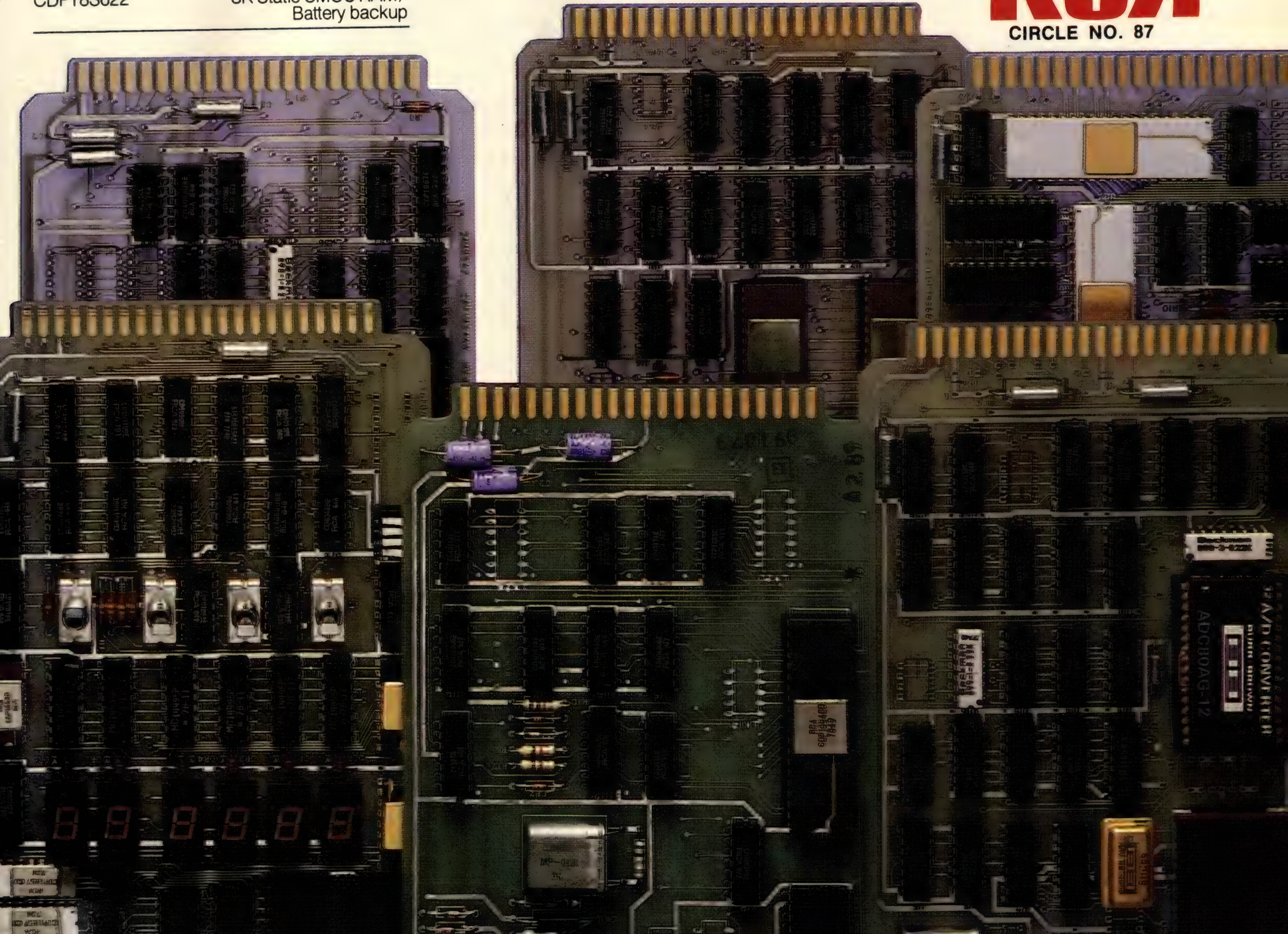
For more information and a free brochure on RCA Microboard Computer Systems, contact your local RCA Distributor.

Or contact RCA Solid State headquarters in Somerville, New Jersey. Brussels, Belgium. Tokyo, Japan.

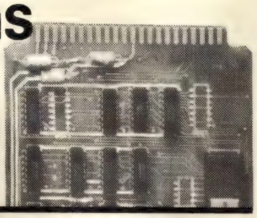
*Coming in 1980

RCA

CIRCLE NO. 87



RCA Systems Appointed Distributors.



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Gerate GmbH
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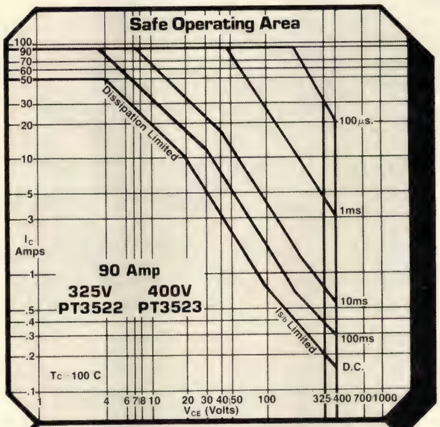

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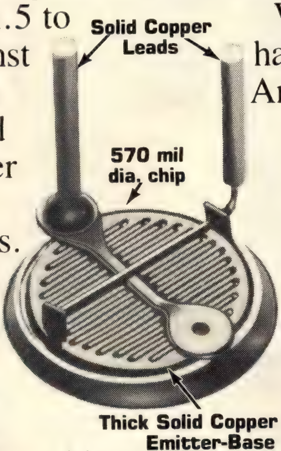

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9-1085

CIRCLE NO. 89

Control unit changes data acquisition

Couple Hewlett-Packard's new data-acquisition and control instrument (the 3497A) with HP's 85A personal computer or other desktop computer, add a fast DVM like HP's 3437A or brand-new 3456A (ELECTRONIC DESIGN, June 7, 1980, p. 149), and enjoy quick, accurate data collection and analysis—all at an attractive price.

For example, voltage reading rates can soar to 5000 per second, and accuracy can reach ±0.0008% +2 counts over a 24-h period at 23 C ±1 C. The 3497A multiplexes up to 4800 channels/s.

The 3497A mainframe consists of a clock-timer, front-panel keyboard and LED display, which shows analog channels, digital slots or dc-voltage measurements. Up to 1000 analog channels and 1360 digital lines are available, using HP 3498A extenders.

The system includes software for instrument driver routines, data analyses and presentations, verification routines and application programs.

Timing in the 3497A comes from a quartz reference, and runs from seconds to months with 1-s resolution. Elapsed time can be monitored or an interrupt can be preset. Programmable pulse trains stemming from the clock can pace measurements or select channels.

Optional plug-ins bring multiplexing, digital monitoring and control functions. For instance, a 20-channel multiplexer contains low-thermal-offset reed relays for low-level transducer measurements.

The 3054A sells for $7000 to $25,000, depending on options and the computer selected. Deliveries start in July.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 857-1501.

CIRCLE NO. 412

Temperature indicator measures up to 3200 F

A digital temperature indicator, Model 5200, offers seven standard ranges for measuring temperatures up to 3200 F. A four-digit display features 0.4-in. high LEDs. Overrange is indicated by a separate front-panel LED. A pushbutton selector switch module, Model 5290, chooses thermocouple or three-wire RTD inputs. The selected input is shown by a lighted red LED over the appropriate pushbutton.

Syscon International, 1239 S. Bend Ave., South Bend, IN 46617. (219) 287-5916.

CIRCLE NO. 324

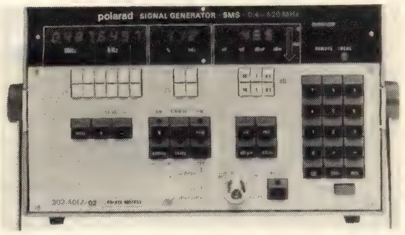
Portable instrument checks transducers

A portable readout, Model 304, has excitation power for up to four 350-bridge transducers. The instrument displays transducer output on its LCD readout and operates from 115 V ac or 12 V dc to facilitate field testing. Three readings are taken each second. Digital display range is 0 to ±1999. A front-panel offset control can be switched in or out. An internal switch selects decimal position. Model 304 operates over a 0 to 115-F range.

Acrotech, 1160 E. Ash Ave., Fullerton, CA 92631. (714) 879-8470. $325; stock.

CIRCLE NO. 325

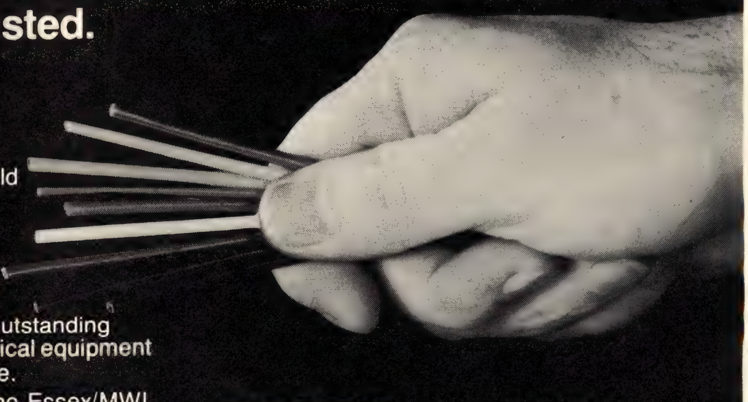
Signal generator works under bus control



A synthesized signal generator, Model SMS, operates under IEEE 488 bus control for measurements from 0.4 to 520 MHz. An option extends instrument range to 1040 MHz. The microprocessor-controlled unit offers a frequency resolution of 100 Hz on an 8-digit display and an amplitude resolution of 0.1 dB on a 3-1/2 digit display in μV, mV, dBμV or dBm. Other options include a high-stability reference oscillator.

Polarad Electronics, 5 Delaware Dr., Lake Success, NY 11042. (516) 328-1100.

CIRCLE NO. 326



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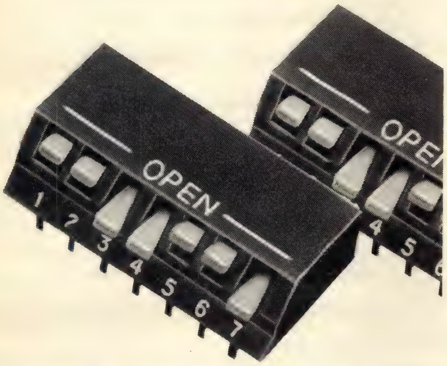
9-1088

CIRCLE NO. 90

Grayhill Side-Actuated Piano-Dip™ Switches Now Totally Sealed



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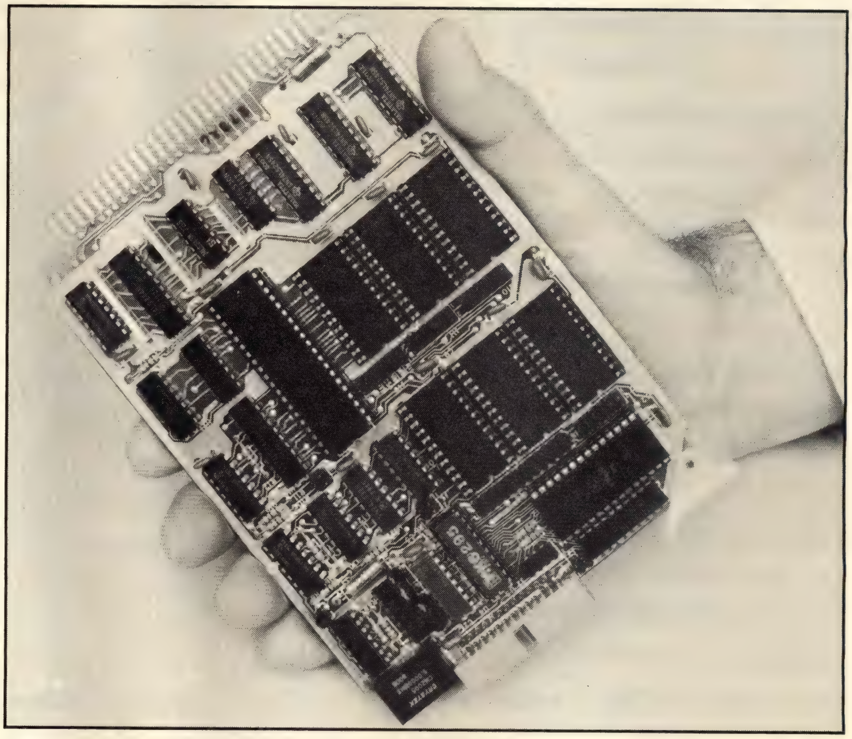
CIRCLE NO. 91

STD-Z80 board handles many memory combinations



Computer board based on Z80 microprocessor has six 24-pin sockets which can accept any combination of seven designated memories.

Designed to satisfy a need for inexpensive microcomputer modules, the Z80-based MDX-CPU2 and CPU-4 boards contain six 24-pin sockets which may be strapped to accept any combination of seven designated EPROMs, RAMs and ROMs. The 4.5 × 6.5-in. microcomputer boards can decode memory on any 1-k boundary of the 64-k memory map; hold bidirectional address, data and control buses for external DMA; and are STD-Z80 bus compatible.

The boards also feature a counter-timer circuit (the MK3882) with four cascadable channels; automatic, transparent dynamic memory refresh; fully buffered signals for system expansion; a selectable reset address to either 0000H or E000H; and a selectable wait-state generator. The six 24-pin sockets will accept the following memory devices: 2758 (1 k × 8), 2716 (2 k × 8) and 2732 (4 k × 8) EPROMs; MK4118 (1 k × 8), MK4801 (1 k × 8) and MK4802 (2 k × 8) static RAMs; and the MK34000 (2 k × 8) ROM.

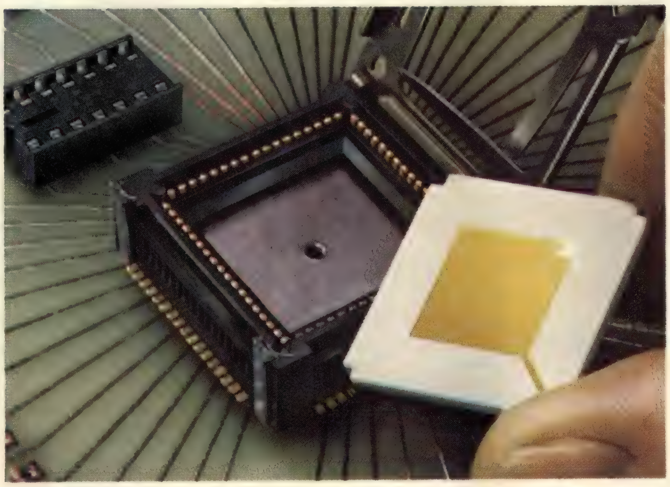
The boards are supplied with a PROM decoder that allows users to choose one of four preselected memory configurations; or, by programming a decoder PROM, the user can assign any of the six sockets to memory addresses, as the application under consideration requires.

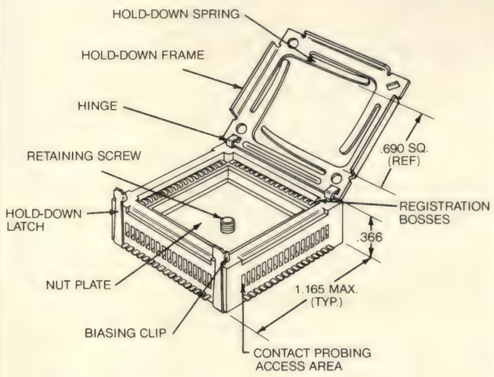
In quantities of 1 to 9, the MDX-CPU2 will sell for $299 and the MDX-CPU4 will sell for $388. Delivery time ranges from 6 to 8 weeks.

Mostek, 1215 W. Crosby Rd., Carrollton, TX 75006. (214) 323-6000.

CIRCLE NO. 303

"We can take advantage of the latest in JEDEC packaging because AMP can deliver the connectors."





More AMP ADS facts worth knowing.

- Mounting flexibility. Solder Tail type in 52, 68, 100 and 124 positions. Surface-to-surface type in 68, 100 and 124 positions incorporates screw installation.
- Built-in alignment guides.
- Integrated datum registration.
- Optional contact probing capability.

The new leadless substrates have a lot of benefits for you—real estate savings, shorter, equalized traces, enhanced speed, and greater accuracy. But first you have to get them to the board. That's why we've made it our business to design and produce—in quantity—the connectors these new substrates require. And that means you can start taking advantage of them right now.

What's more, our Active Device Substrate (ADS) connectors have advantages of their own. Like two low-profile mounting styles—solder tail and Surface-to-surface—and a wide range of positions in each, up to 124. Both styles have a hinged frame design that exerts more than 50 grams normal force per contact on the ceramic package pads. So you get a reliable interface and compatibility with substrates incorporating cooling fins.

For more information on how you can put the performance of JEDEC packaging into production now, call the ADS Information Desk at (717) 780-8400. Or write us. AMP Incorporated, Harrisburg, PA 17105.

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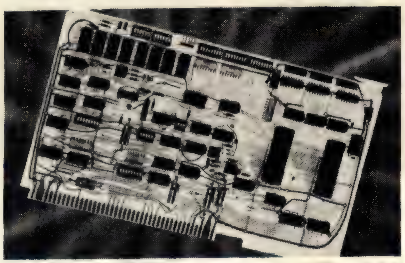
CIRCLE NO. 93

Supervisory board resets Multibus system



A supervisory board, SB-1004, provides the features necessary to reset a Multibus system after a system malfunction. A watchdog time-out circuit detects malfunctions. Should the system fail to resume normal operation after the reset, an on-board relay activates to trip failure alarms. In addition to reset, the SB-1004 provides a reset on power-up, power brown-out and manual reset. Interrupt intervals are user-selectable from 100 μs to 10 s.

Morrow Computer & Electronic Design, 315 Wilhagan Rd., Nashville, TN 37217. (615) 329-1979. $395. **CIRCLE NO. 327**

Board packs 512 kbytes for DEC minicomputer

A high-speed, high-density memory board, NS780, packs 512 kbytes on a single hex-wide card. The board is compatible with DEC's VAX 11/780, 32-bit minicomputer. The card is a direct replacement for DEC's M8210 memory. The NS780 features a partitioned power plane to minimize drain by powering only the memory elements and refresh circuits during battery backup conditions. An on-line/off-line switch allows the memory to be electrically removed from the system to assist reconfiguration or troubleshooting.

National Semiconductor, 2900 Semiconductor Dr., M/S 7C-265, Santa Clara, CA 95051. (800) 538-8510. $6995.

CIRCLE NO. 328

Bubble memory braves hot climates

A 1-Mbit magnetic bubble memory device, 7110-1, tolerates the extremely hot environments which limit the use of disk or tape memories. The device is specified for operation at 70 C. Microcomputer systems need no longer be limited by the temperature tolerance of memory systems. The 7110-1 is available individually or as part of an improved version of the BPK71 prototype kit. The kit contains one 7110-1 and includes a blank PC board.

Intel Magnetics, 3000 Oakmead Village Dr., Santa Clara, CA 95051. (408) 987-6046. $1985 (7110-1); $2280 (BPK71).

CIRCLE NO. 329

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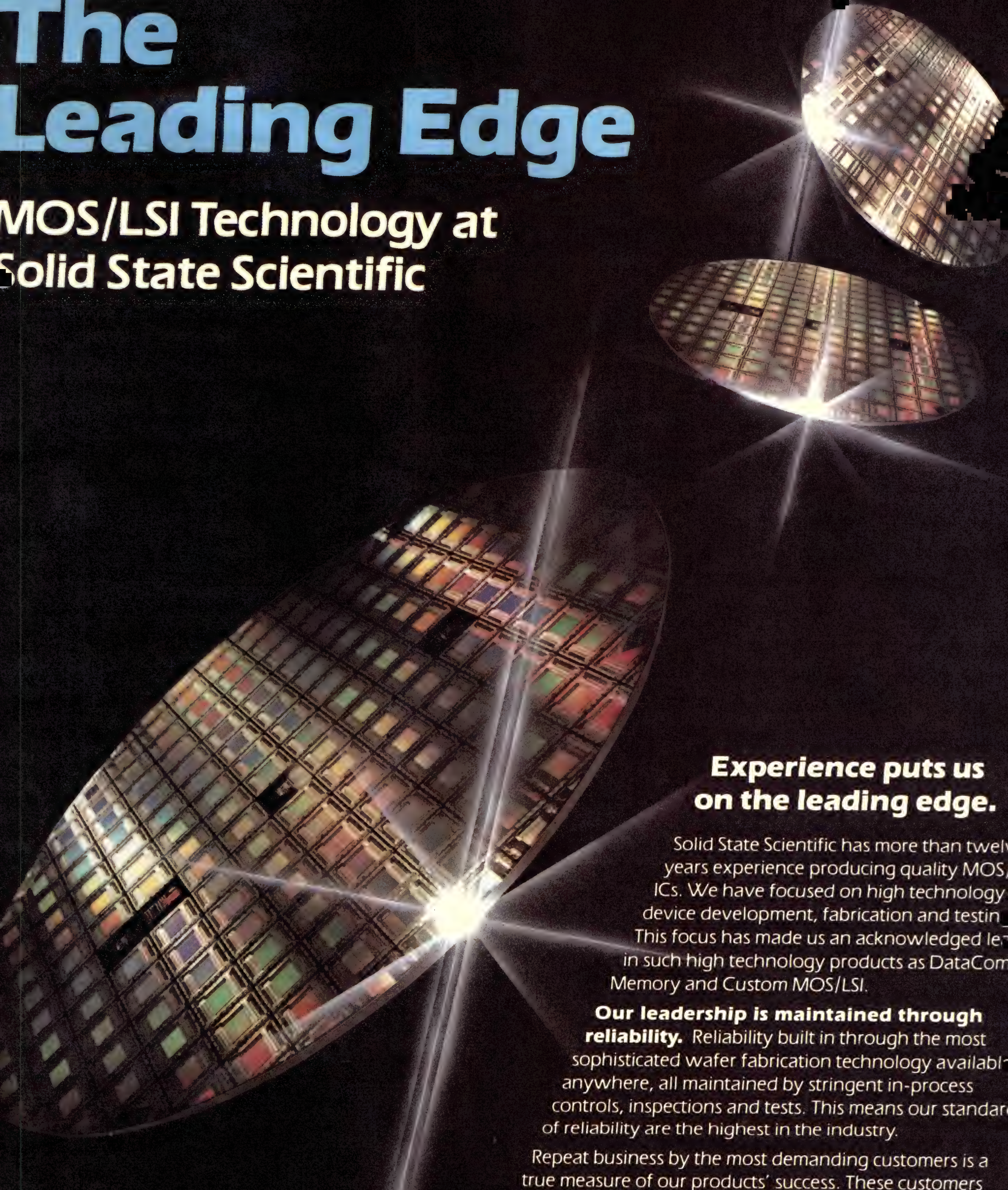
CIRCLE NO. 94

The Leading Edge

MOS/LSI Technology at Solid State Scientific



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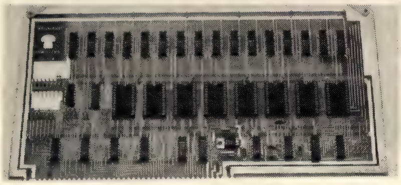
Solid State Scientifi

RAM/PROM module ups one-board μC storage



A Multibus-compatible RAM/PROM card, PAM-1/ES, expands the memory capacity of single-board or development system computers. The board is available in 4 or 8 kbyte versions using 2114 devices. Eight sockets are provided for 24-pin ROMs or PROMs. The module supports 8 kbytes of 2708 PROMs or 16-kbytes of 2716 PROMs or equivalent ROMs. RAM and PROM are fully address selectable. Power supply requirement is 5 and ±12 V.

MegaLogic, 9659 National Rd., Brookville, OH 45309. (513) 833-5222. $295; stock to 6 wks.

CIRCLE NO. 330

Interface connects PDP-11 to IEEE-488 bus

A high-speed DMA interface, GPIB11-2, provides the hardware link between DEC's PDP-11 computer and the IEEE-488 instrumentation bus (also referred to as the GPIB). The single SPC hex card provides decoding of GPIB commands for implementing talker, listener and controller functions. Transfer rates of up to 500 kbytes/s are provided for three-state operation and up to 250 kbytes/s for open collector. Three-state or open-collector operation is switch-selectable. The interface card works in either a single or multiple controller environment. Software supports includes drivers, utilities and an interactive control program. A 4-m cable with a GPIB connector on the outboard end allows connection of as many as 14 instruments on a single interface.

National Instruments, 8900 Shoal Creek Blvd., Austin, TX 78758. (512) 454-3526. $1995; stock.

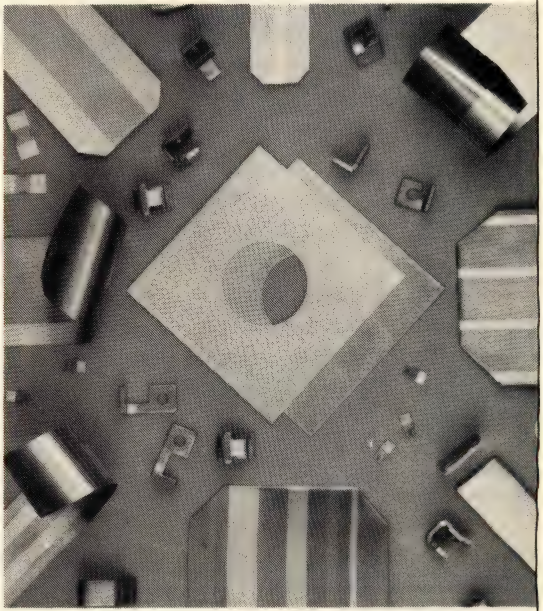
CIRCLE NO. 331

Single board expands PDP-8 memory

A single memory board, VM832, expands memory storage of PDP-8 microcomputers by up to 32-k. The board's memory is fully static; stalls in the memory timing, due to refresh logic, are eliminated. On-board DIP switches allow each 4-k memory field to be individually assigned to any field of 0 to 31 when operating with the KT8A memory management option. Power requirement is 4.2 A at 5 V dc.

Computer Extension Systems, 17511 El Camino Real, Houston, TX 77058. (713) 488-8830. $1850.

CIRCLE NO. 332



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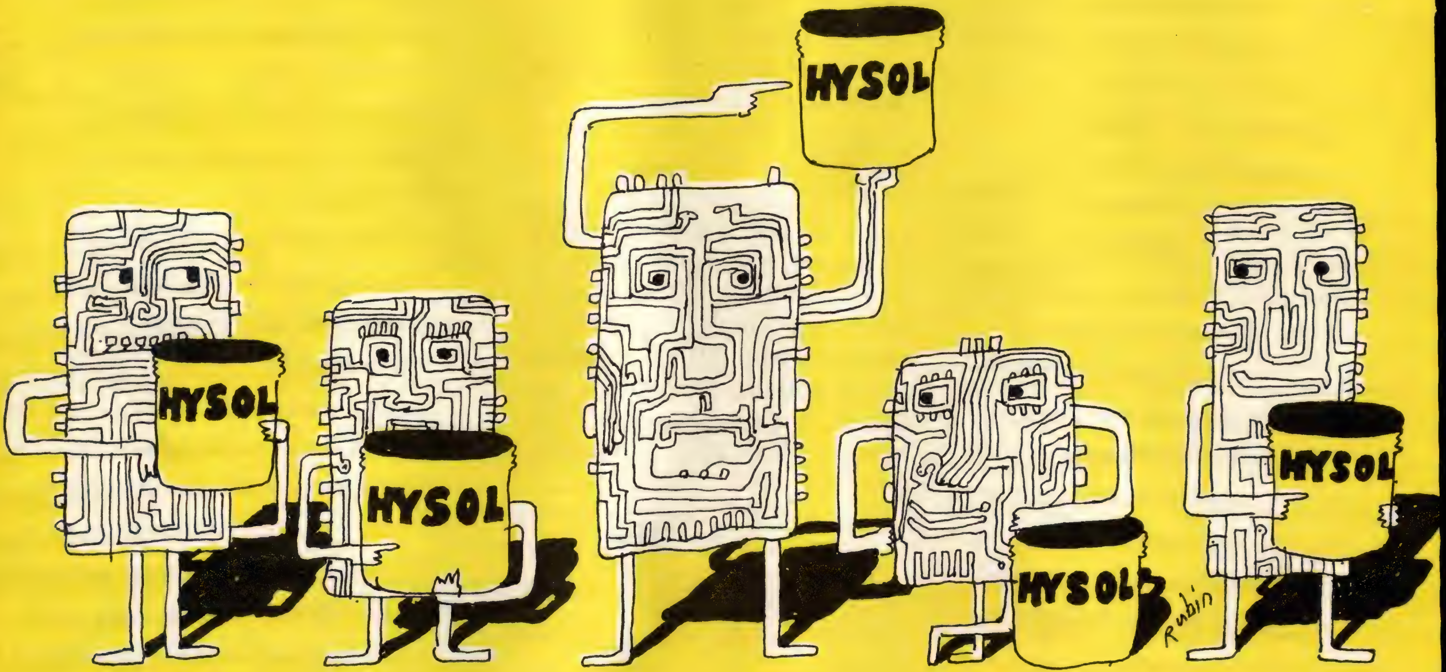

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The experts agree, Hysol's remarkable SR1000 Solder Resist is really different. In performance. And *productivity.*

Sure, Hysol SR1000 is a PC 401 spec equivalent.

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First, our SR1000 has only one component. No time lost weighing, mixing or measuring. Just open the can and it's ready to go. That's productivity.

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As good as it is for PCB, Hysol SR1000 is even better for your production environment. In fact, SR1000 releases just 5 percent volatiles during cure. And SR1000 volatiles are actually *exempt* from air pollution regulations.

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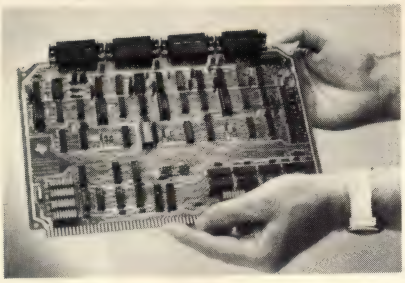
Telephone (213) 968-6511.

CIRCLE NO. 97

Data-comm board links TM990 μC to modems

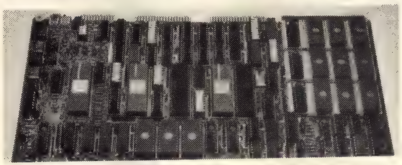


An addition to the TM990 family of microcomputer modules, the TM990/307 communications expander allows exchange of serial data with up to four asynchronous or synchronous modems or terminals through RS-232 interfaces. The board provides parallel interfacing to an autodialer, such as the Bell 801 Automatic Calling Unit. Individual channels are selected via communications register unit (CRU) addresses. Features include a loopback mode, which allows self-testing with a demonstration software package. Baud rates are software programmable and switch-selectable interrupt levels are offered for each of the four channels. One of the four channels also provides an RS-422 interface. The board, which measures 11 × 7.5 in., is characterized for operation from 0 to 70 C.

Texas Instruments, P.O. Box 1443, M/S 6404, Houston, TX 77001. (713) 494-5115. $650; stock.

CIRCLE NO. 333

All-CMOS one-board μC plugs into Multibus cage



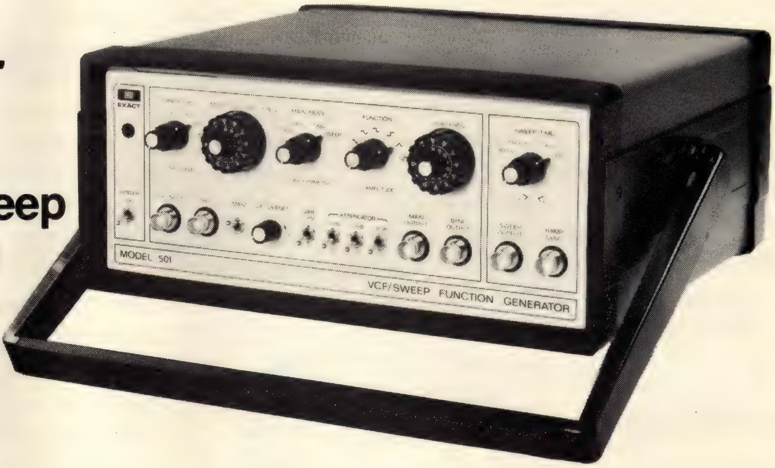
An all-CMOS single-board microcomputer, Model PPS-1201, plugs directly into a Multibus card cage. The board uses a CMOS 6100 microprocessor, 4 kwords of memory (any combination of CMOS RAM and EPROM), a programmable real-time clock, a memory expansion controller, three 12-bit wide parallel ports and a single serial port (either RS-232 or 20 mA). Also included is a transparent 1-kword "control-panel" memory contain a monitor and debugger which performs all commonly required system-development functions. A binary bootstrap is available for loading on-board RAM through the serial port. Power requirement is 5 V at less than 60 mA. The 6100 microprocessor uses a binary instruction set identical to that of DEC's PDP-8 and VT-78 minicomputers, so software development can be carried out on these systems.

Pacific Cyber/Metrix, 6800 Sierra Ct., Dublin, CA 94566. (415) 829-8700. $995; 4 wks.

CIRCLE NO. 334

The Exact Model 501...

A $595.00* 5 MHz VCF/Sweep Function Generator with a proven militarized design.



The Model 501 possesses all of the performance characteristics of its military counterpart the Exact Model 566 — currently doing duty with the Marines. Dressed up in a new lightweight aluminum package, the Model 501 offers features found only in function generators costing much more. Precision Start/Stop frequency controls, 5 MHz top frequency, gate and trigger modes, and 30 Volts P-P output are perhaps the most important items you look for in a function generator. Add to those a wide range auxiliary ramp generator, variable symmetry, adjustable lockout level, and fixed step attenuators, and you soon realize that the Model 501 may be the most affordable test instrument available today.

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CIRCLE NO. 98 FOR MODEL 501

CIRCLE NO. 221 for 1980 CATALOG

Wafer-trim system speeds things up with YAG laser

Controlled by a PDP-11 computer, the MicroLase Model 80 wafer trim station can provide laser pulses of 30 to 40 ns, using a Q-switched Nd:YAG laser.

To speed up wafer-level IC processing, the Model 80 MicroLase system relies on a Q-switched Nd:YAG laser that handles resistor trimming, selective annealing and link cutting for both analog and digital circuits. The special laser has a short-pulse capability (30 to 40 ns), first-pulse control and high pulse-to-pulse stability for consistent trimming over long production runs.

Other system features include kerf widths of 4 to 8 μm and automatic beam-to-work alignment within 2.5 μm (submicrometer resolution is optional).

The probe fixture can accommodate a variety of test components and an inker for marking chips. The fixture accepts a 4.5-in. probe card and larger functional boards. A laser power detector is mounted on the wafer nest of the step-and-repeat table.

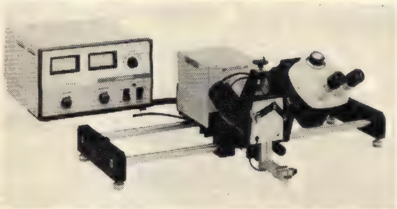
Since the system is intended for trimming products at the wafer level, the laser-beam positioning subsystem is kept within the boundaries of a 0.75 × 0.75-in. area. Positioning is based on two recoilless linear motors. An optics arm coupled to the motors carries the focusing (objective) lens for the laser. The lens produces a beam with a waist diameter of less than 6 μm and with a field depth of ± 50 μm. The same lens also magnifies the image of the trimmed region up to 500 times for the system's closed-circuit TV.

The entire system requires a floor area of about 150 sq ft, as well as deionized water for the cooling unit and tap water for cooling the deionized water. The system costs from $200,000 for a bare-bones package to about $250,000 for a system with most of the options available. Delivery is six to nine months, depending on options.

Electro Scientific Industries, 13900 Science Park Dr., Portland, OR 97229. Tom Freeman (503) 641-4141.

CIRCLE NO. 310

Rework center repairs damaged PC boards



A complete rework center, the Circuit Saver, repairs damaged PC board circuit traces, including those on double-sided and multilayer boards. A parallel-gap welding technique welds a gold-plated kovar, gold, copper or nickel ribbon over a broken or defective trace on boards up to 36-in. wide. Circuit Saver produces repairs to traces between 0.005 and 0.02-in. wide without damage to surrounding trace geometry. The system also provides the capability of welding flat packs to circuit boards.

Unitek, 1820 S. Myrtle Ave., Monrovia, CA 91016. (213) 574-7800. **CIRCLE NO. 335**

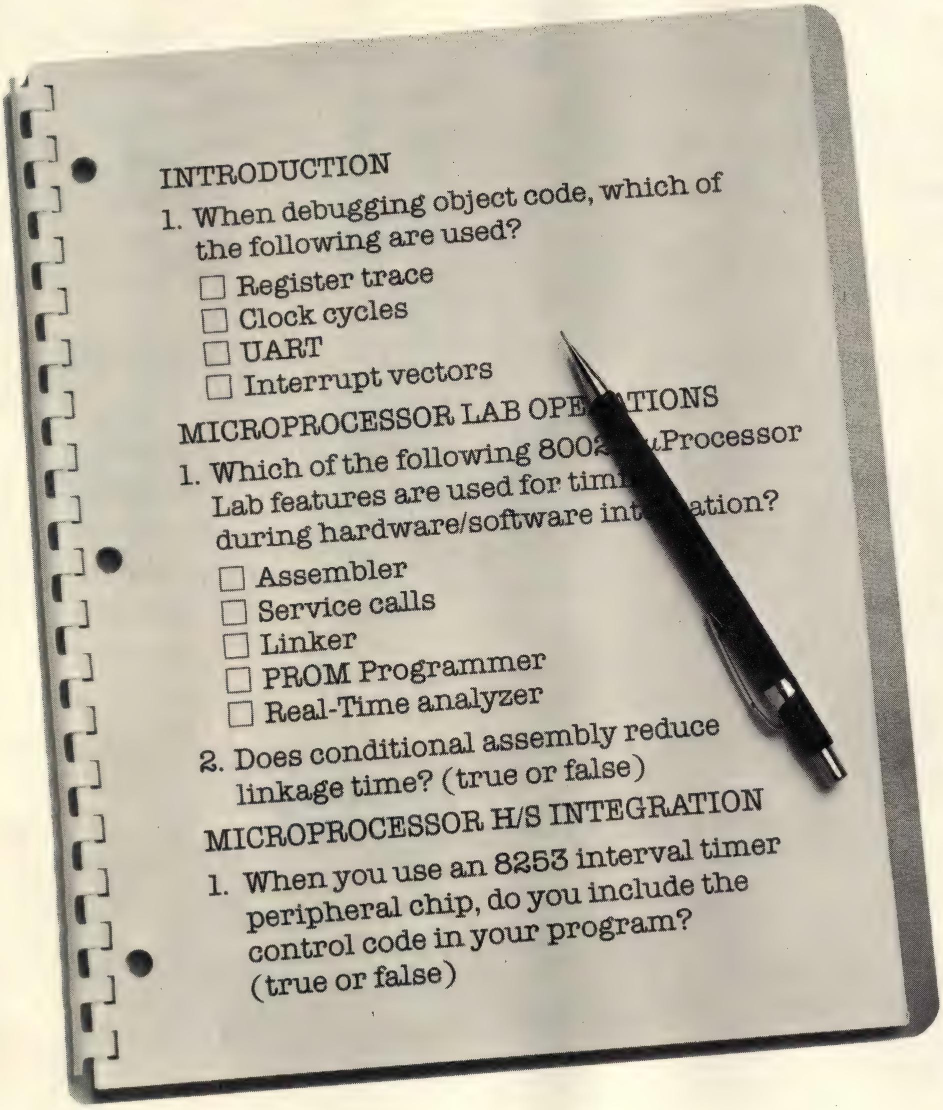
Wafer processor needs little outside help

A wafer processing system, the Micronet Autofab, operates under microprocessor control to minimize handling and operator involvement. The system uses various processing modules, configured to suit different processes or fabrication area layouts. The system sends, scrubs, coats, develops, bakes, receives and stores 3 to 6-in. wafers. Displays, status reports and commands appear on a CRT in simple English. A diagnostics system reduces troubleshooting time and can be used in line. Process parameter alarms assure consistent wafer processing.

Computervision Cobilt, 2727 Augustine Dr., Santa Clara, CA 95051. (408) 727-2300.

CIRCLE NO. 336

Test your microprocessor design IQ.



INTRODUCTION

1. When debugging object code, which of the following are used?
   - ☐ Register trace
   - ☐ Clock cycles
   - ☐ UART
   - ☐ Interrupt vectors

MICROPROCESSOR LAB OPE ATIONS

1. Which of the following 8002 μProcessor Lab features are used for timi during hardware/software int ation?
   - ☐ Assembler
   - ☐ Service calls
   - ☐ Linker
   - ☐ PROM Programmer
   - ☐ Real-Time analyzer
2. Does conditional assembly reduce linkage time? (true or false)

MICROPROCESSOR H/S INTEGRATION

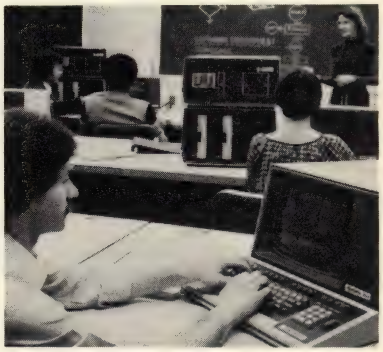
1. When you use an 8253 interval timer peripheral chip, do you include the control code in your program? (true or false)

How many questions did you miss? One? Two? Three or more? Well, no matter how you did, this little test proves one thing: The field of microprocessor design is changing so rapidly, it's a real challenge just to stay on top.

That's why we invite you to attend one of our three Microprocessor Development Workshops.

Each workshop is an intensive, week-long course that provides hands-on training in three different areas of microprocessor design.

And each gives you the kind of practical, results-oriented instruction you need to meet your unique design challenges...



Whether you're an engineer who'd like to learn more about designing with microprocessors; a software programmer who wants to know more about writing and interfacing software for microprocessors; or an engineer/manager who needs to find out more about the microprocessor development cycle. The fee? Only $650 per workshop.

But hurry. Enrollment is limited to 12 students per workshop. To find out more — or to reserve your space — call MDL Training at 503 644-0161 x6091. Or fill out the coupon below. And put yourself to the test.

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1101 Boston, MA June 16-20
1102 Chicago, IL June 23-27
1103 Washington, DC August 4-8
1104 Chicago, IL August 25-29

Microprocessor Hardware/Software Integration Techniques

1400 Washington, DC June 23-27
1401 Boston, MA July 14-18
1402 Santa Clara, CA July 28-August 1
1403 Chicago, IL August 11-15
1404 Boston, MA August 25-29

Microprocessor Lab Operations

1200 Boston, MA June 2-6
1201 Chicago, IL June 9-13
1202 Washington, DC June 16-20
1203 Santa Clara, CA June 23-27
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1206 Boston, MA August 11-15
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CIRCLE NO. 101

New conductive plastic element now available in the MOD POT®... the original modular potentiometer.

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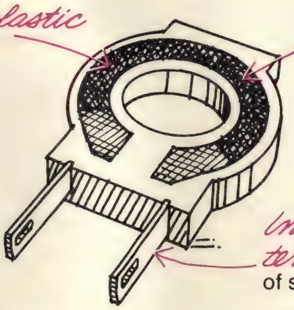

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EC214

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A 40-W soldering iron, the "Slide-Away" safely packs away into a tool box immediately after use. A sliding tip retracts into the iron's handle, simultaneously disconnecting power. The iron uses replaceable thread-on tips.

Electronic Tool Claremont Ave., Thornwood, NY 10594. (914) 769-8070. **CIRCLE NO. 337**

Laser system trims and cuts on wafer level

A laser trimming and processing system, Model 80 MicroLase, cuts and trims VLSI products on the wafer level. A Q-switched Nd:YAG laser develops a short-pulse capability (30 to 40 ns), first-pulse control and pulse-to-pulse stability in producing consistent trimming kerfs over long production runs. Kerf widths range from 4 to 8 microns. Other features include automatic beam-to-work alignment within 2.5 microns; under 1-micron resolution is optional. A PDP-11 process control computer uses a DEC RL-01 5-Mbyte disk drive and Pascal software.

Electro Scientific Industries, 13900 N.W. Science Park Dr., Portland, OR 97229. (503) 641-4141. **CIRCLE NO. 338**

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High-friction flexible mats, StopSlip, hold small components and circuit boards right where you want them—on the workbench. The elastomeric pads have a high coefficient of friction; flat objects, placed on the mats, stay in place. The mats are useful as a scratch-preventitive surface for board assembly and soldering. Since it snags small components, the mats act like a third hand. Tackiness of the mats is inherent and will not gradually decrease. The elastomer does not leach plasticizers.

S.A.T., 357 Cottage St., Springfield, MA 01104. (413) 788-6191. **CIRCLE NO. 339**

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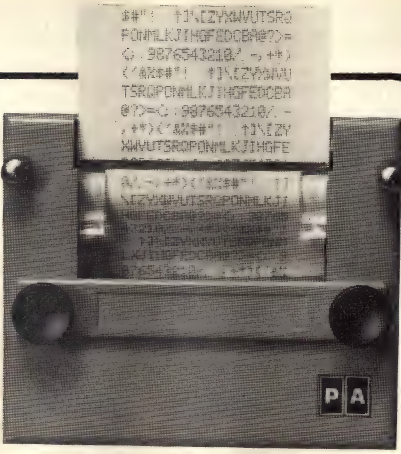
CIRCLE NO. 103



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CIRCLE NO. 104

THE GANG PROGRAMMER THAT GIVES YOU MORE FOR LESS...

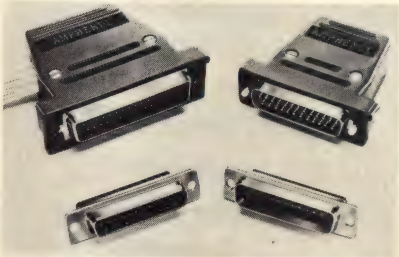
The PkW-8000 handles up to eight EPROM's simultaneously without extra options utilizing built-in power supply and four standard selection units. Almost every type of EPROM can be programmed. Yet, it weighs just over ten pounds, is compact and efficiently portable. Extra automatic functions include a voltage margin check, incorrect EPROM insertion check, data bus check and a level limiter. Compare reliability, performance and low cost and you'll agree that the PKW-8000 does give you more for less.

For complete information, price and delivery, write or phone.

WES-CON PRODUCTS, INC.
525 University Ave., Suite 705, Palo Alto, CA 94301, Telephone (415) 327-4051 TELEX 345549

CIRCLE NO. 105

D-type connectors meet flammability tests



A family of rectangular, rear-release, miniature D-type connectors meet stringent flammability requirements. Min-Rac 17 Series rack and panel connectors use 94V-O rated materials. The connectors conform to performance requirements of EIA standards RS-232C and RS-449 for data transmission. Completely intermateable and intermountable with existing D-type rack and panel designs, the new connectors are offered in five standard contact configurations—9, 15, 25, 37 and 50. Current rating is 5 A maximum per contact

Amphenol Bunker Ramo, 2122 York Rd., Oak Brook, IL 60521. (312) 986-2322. $3.34 (1000 qty); 2 to 4 wks. **CIRCLE NO. 340**

Hand presser assembles telecomm connectors

A hand pressing tool, the MS² 4254, aids field splicing of Pre-Con telecomm connector modules. The plier-like tool securely closes a module in three crimping strokes, assuring positive action each time with an audible snap. The tool can be set for use on male or female Pre-Con modules, for base/body/cover closure after re-entry in any Super-Mini module or for adding a bridge module to a Super-Mini module. A holster is supplied for easy carrying and convenient access.

3M, Dept. TL80-14, Box 33600, St. Paul, MN 55133. (612) 733-3351. **CIRCLE NO. 341**

It's spillproof.

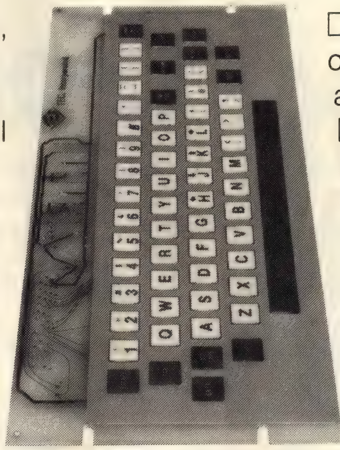
New from TEC
Low cost, low profile
Tactile Feel Keyboard

The front surface of the Keyboard is sealed with a Polycarbonate Material making it impervious to most accidental spills.

For areas where harsh chemical environments exist other overlay materials are available.

Features

☐ Tactile feel ☐ Custom design, unlimited colors optional ☐ Embossed keys on velvet surface ☐ Positive mechanical contacts ☐ LED indicators in keys for specific key functions, optional ☐ All versions sealed from front, environmental back sealing optional ☐ Enclosure optional ☐ Mounting on .093″ (.236 cm) PCB for rigidity.



Less than .125″ (.317 cm) thick

☐ Contact life in excess of 5,000,000 cycles ☐ ASC II or EBCDIC encoding available ☐ Parallel output standard ☐ Serial output optional ☐ 3 or 4 modes of operation available on intelligent models ☐ "ALL CAPS" key electronically latched on intelligent models ☐ CMOS optional ☐ Direct soldering, terminals, PCB tab, Flex tail, or Connector interface available. Standard model has a 34 pin header.

Major Applications

1. **Process Control**
   Machine shop environments; paper mills; textile industries; Oil and associated drilling rigs.
2. **Home Computers**
   Low cost applications where fast data entry is not required.
3. Any application where severe environmental conditions exist.

Ask about our other Keyboards too!

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TEC International, Inc.
European Sales Office:
Avenue Louise 148—Box 6, 1050 Brussels, Belgium
(02) 649 81 54/Telex 846-63553

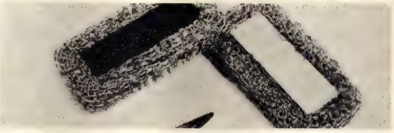
CIRCLE NO. 106

Coax stripper does it all in one step

A hand-held coaxial cable stripper, Model CX-1, prepares most cables in a single operation. Precision screw adjustments determine the depth of each cutter's cut. Cable holders for various size cables are interchangeable. Built-in length adjustment allows any desired center conductor length to be cut. Spacers permit proper cutter spacing for all commonly used connectors. Model CX-1 handles cables within a 0.075 to 0.485-in. range. The tool is fabricated from anodized aluminum and uses hardened tool steel cutter blades.

Western Electronic Products, 107 Los Molinos, San Clemente, CA 92672. (714) 492-4677. $49.50; stock. **CIRCLE NO. 342**

Static discharge pads make snug retrofit



Static discharge contact pads, made with sponge rubber centers, provide a snug retrofit into performed pockets or ridges in cabinets and metal housings. Knitted wire mesh is bonded to rectangular or square centers of sponge rubber. The pads provide electrical continuity between mating edges of metalized plastic enclosures or metal cabinets. A variety of metals are available to suit operational requirements, such as galvanic compatibility, high current capacity, resistance to corrosive atmospheres and similar specialized needs.

Metex Electronic Shielding Group, 970 New Durham Rd., Edison, NJ 08817. (201) 287-0800. **CIRCLE NO. 343**

Tool kit suits the rf engineer

A kit with more than 90 tools for the rf or communications engineer comes in a convenient, two-pallet, all-weather case. Included are alignment tools, fastening tools, pliers, cutters, strippers, test equipment, wrenches, a hole saw kit, soldering and desoldering equipment, solderless terminals and a 3/8-in. electrical drill.

Jensen Tools, 1230 S. Priest Dr., Tempe, AZ 85281. (602) 968-6231. **CIRCLE NO. 344**

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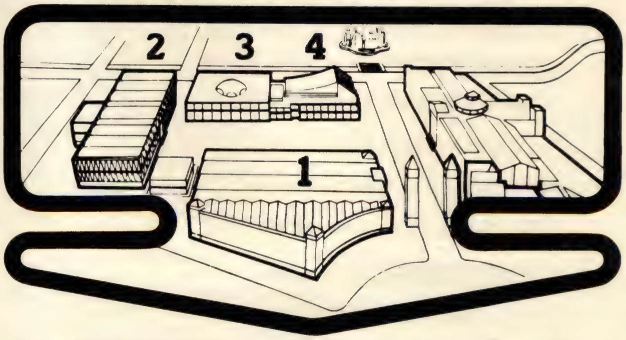

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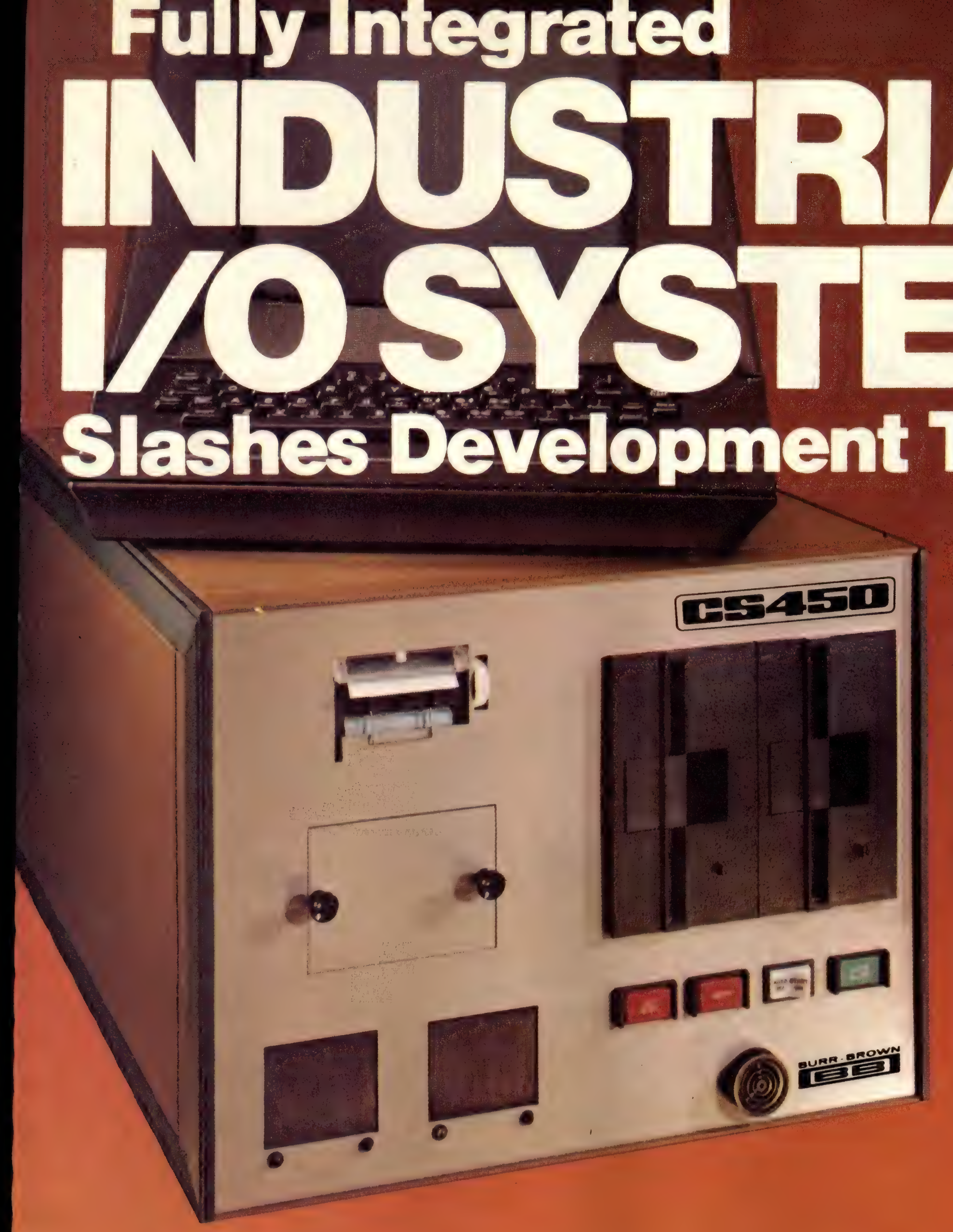
4 Symposiums, Conventions, Meetings. Hi-Fi and Video demonstrations.

FAIR GROUNDS: BARCELONA (SPAIN) 29th september, 5th october, 1980
Trade visitors: 29th, 30th september and 1st october - General Public: 2nd, 3rd, 4th and 5th october
INFORMATION: Avda. M.ª Cristina, s/n. - BARCELONA-4 (Spain) Tel. 223 31 01
Telex 50458 FOIMB-E
CIRCLE NO. 108

Fully Integrated INDUSTRIAL I/O SYSTEM Slashes Development Time



CS450...A Stand-Alone Measurement and Control System

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- **Complete I/O family**
- **Intel Multibus™**
- **12″ CRT terminal**

If you've avoided programmable I/O systems because you think they're confusing, mysterious and expensive...

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But now you can computerize your operations simply, at low installed cost!

CS450 is a complete data acquisition and control system that's really easy to install and use. It includes microcomputer, memory, peripherals, real world I/O, human interface and software tools. Its' AUTOSTART feature will even load and run your programs without an operator. Depressing a single "function" key can send a multistep, preprogrammed instruction to CS450.

You communicate with CS450 in straightforward, plain-talk Burr-Brown BASIC-400. Write your application program using this powerful, easy-to-debug interpreter language. Communicate with the real world with analog and discrete I/O boards that plug into CS450's Multibus.

Program and data storage is provided by dual minifloppies (standard) and dual minicassette options. An internal 40-column printer is an option. A Centronics printer port is standard. Optional 12″ CRT with full ASCII keyboard provides operator interface. Other features include audible alarm, real time clock and system battery backup option.

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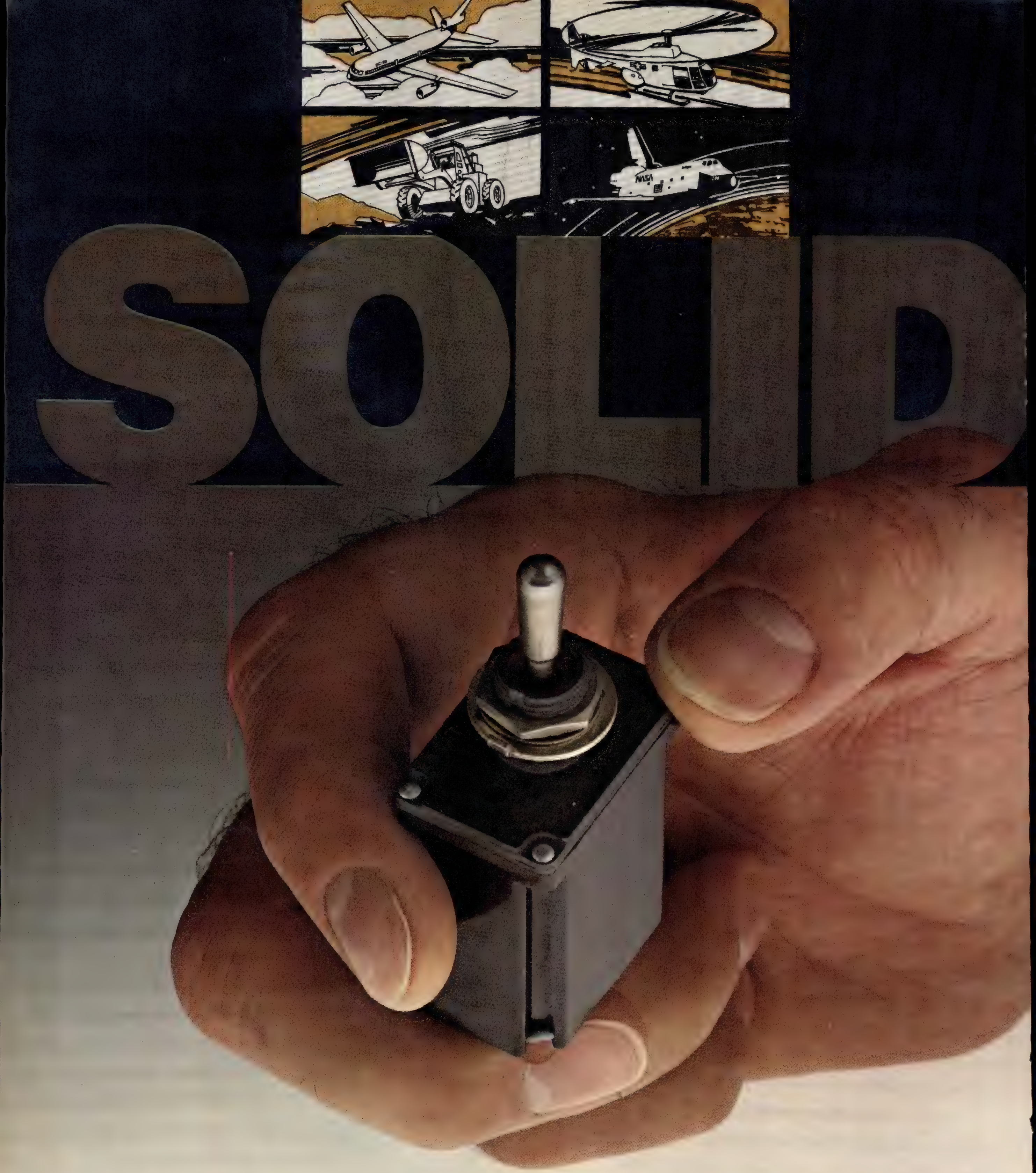
Multibus™ Intel Corp.

CIRCLE NO. 109



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For more information on any product in our full line, contact your Cutler-Hammer Aerospace Products Specialist or distributor—they know your business. And, write for our free catalog. Eaton Corporation, Aerospace Control/Systems Division, 4201 N. 27th St., Milwaukee, WI 53216.

EATON Electrical/Electronic Control

CIRCLE NO. 110

Adapters couple Type N plugs/jacks to GR-900

Coaxial-cable adapters connect GenRad GR-900 (14-mm) connectors and Type N male and female types. No. 2099-2-14 is for Type N jacks while No. 2099-1-14 suits Type N plugs. Both adapters have a VSWR of 1.004 from dc to 8.5 GHz. Chrome-plated coupling mechanisms are used on the GR-900 side along with gold-plated silver contacts. On the Type N side, No. 2099-2-14 (jack) has a gold-plated outer body and inner conductor. No. 2099-1-14 (plug) has a Kings TR-5 bright alloy coupling nut and gold-plated body and contacts. Both adapters measure 2.35 × 1 in.

Kings Electronics, 40 Marbledale Rd., Tuckahoe, NY 10707. (914) 793-5000.

CIRCLE NO. 345

Microscope inspects IC wafers and masks

An IC inspection microscope, the BHMJL, accommodates wafers up to 5-in. in diameter and masks of up to 6-in.^{2}. The unit was created especially for inspection of microelectronics and incorporates features designed to ease that task. A mechanical stage moves smoothly and with driftless motion on independent ball races. Observation is possible with brightfield, bright and darkfield, Nomarski differential interference contrast, as well as through the techniques of photomicrography and microprojection. A revolving nosepiece is interchangeable. A full range of objectives is available, as are light sources and other modifications. A variety of wafer and mask holders is offered.

Olympus, 4 Nevada Dr., New Hyde Park, NY 11042. (516) 488-3880.

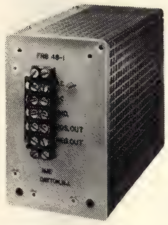
CIRCLE NO. 346

A POWERFUL STATEMENT FROM NJE

"NJE Power Supplies and Systems are THE BEST INVESTMENT in terms of watt hours per dollar of any available anywhere!"

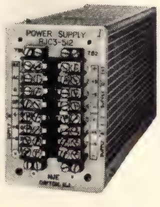
ASK US-WE CAN PROVE IT!

● FERRORESONANT ●



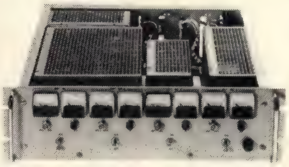
The same model can handle both 50Hz and 60Hz inputs. MTBF's in excess of 100,000 hrs. and efficiencies from 70% to 85%. Output power to 1000 watts. Densities up to 0.9 watts per cubic inch.

● SERIES-REGULATED ●



High reliability, excellent line and load regulation, very low output ripple and noise, fast transient response, and remote control capability. Outputs available to 500 volts.

● POWER SYSTEMS ●



Incorporate up to eight modular supplies in one rack assembly. Systems may be tailored to your custom requirements by incorporating options from the extensive list available including panel metering, individual controls, test jacks, redundancy and load sharing. Combinations of ferroresonant and series regulated supplies may be accommodated.

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CIRCLE NO. 111

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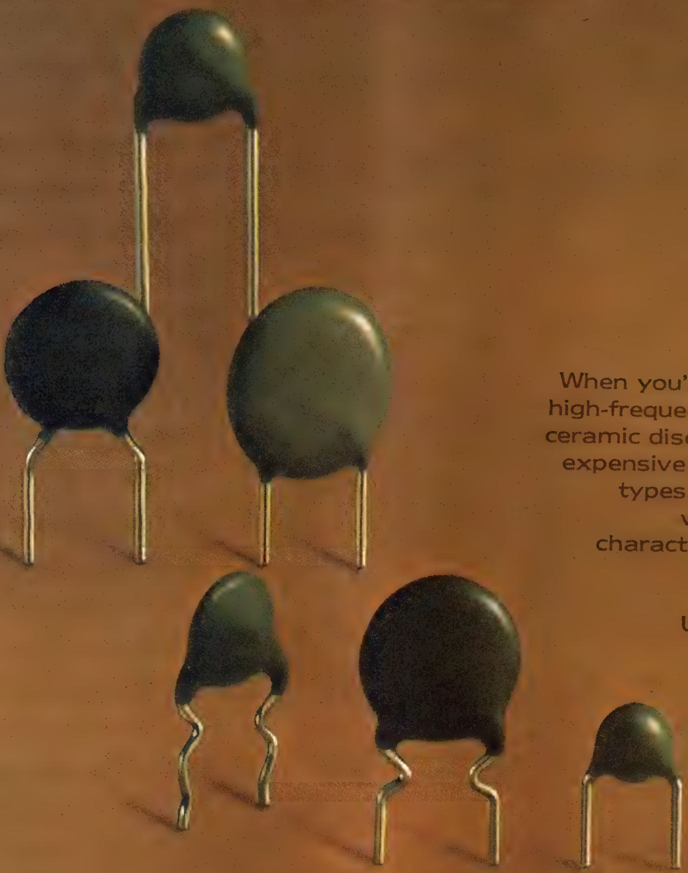

When you're selecting capacitors for low-voltage, high-frequency applications, Centralab's Ultra-Kap ceramic disc is the economical alternative to more expensive film, tantalum and multi-layer ceramic types. Look at the specs and you'll find that when you can't afford the performance characteristics of an X7R monolithic, but your circuit demands better stability than a hi-K dielectric ceramic disc, the Ultra-Kap is the answer. It will provide the stability and ceramic reliability you need at a reasonable price.

With Ultra-Kap, you get a non-polarized, temperature-stable capacitor with excellent high frequency characteristics and a small package size. You get the kind of ceramic reliability that's been proven in many types of severe environmental and other demanding applications.

They're available in a wide variety of lead configurations and are offered with your choice of tape and reel packaging for automatic insertion. Standard sizes and values are stocked for off-the-shelf delivery by over 200 Centralab Industrial Distributors.

Discover the foremost source for your ceramic capacitor requirements. Call your Centralab Representative or write Centralab, Inc., a North American Philips Company, 5855 N. Glen Park Road, P.O. Box 2032, Milwaukee, Wisconsin 53201.

CIRCLE NO. 231

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Nonvolatile RAM needs just two supplies

Instead of the exotic programming voltages required by other MNOS devices, the MN9410 electrically alterable random-access memory operates from +5 and −12-V supplies. With a nonvolatile storage capacity of 64 × 4 bits, the read/write memory permits independent reprogramming of each of its 64 words, via a common I/O data bus and two control inputs.

Housed in an 18-pin DIP, the MN9410 has latching data and address inputs and three-state data outputs. To generate all the programming voltages on-chip, the memory must have an external capacitor connected from the −12-V supply to a special voltage-generator pin. Data can be retained for a year over a 0 to 70 C temperature range, if write pulses are kept to 10 ms. (The unit will function for shorter periods over a −40 to +80 C ambient operating range.)

A minimum of 10^7 write operations are guaranteed, with a minimum recommended pulsewidth of 1 ms for a write, an address setup time of 1 μs and a data setup time of 2 μs. Memory read times equal the chip select time (2 μs) plus the propagation delay time (1 μs). A 1-ms pulse can erase any selected word.

All outputs and inputs are TTL or CMOS compatible and can handle up to one TTL load. The memory has six address inputs, four data I/O lines, a read/write control line, a strobe control line and two chip-select control lines, in addition to the three power supply pins and the external capacitor connection. Power dissipation for the memory is typically about 300 mW.

The MN9410 costs $28.69 in 100-unit quantities; delivery is from stock for small quantities.

Plessey Semiconductors, 1641 Kaiser Ave., Irvine, CA 92714. (714) 540-9979.

CIRCLE NO. 302

Transceiver couples to the 1553 bus

A hybrid transceiver, BUS-8553, works in modular remote terminals receiving and transmitting 1-MHz serial data along the military's 1553 bus. The device operates between the bus and Manchester II encoder/decoder. No adjustments for coupling to the data bus are required. BUS-1553 is TTL compatible and operates from ±15 and +5 V supplies. Internal filtering provides an improved s/n ratio.

ILC Data Device, 105 Wilbur Pl., Bohemia, NY 11716. $295; stock to 13 wks.

CIRCLE NO. 347

16-k CMOS ROM draws only 7 mA

A low-power replacement for 2316 ROMs and 2716 EPROMs, the 16-k SCM5316 CMOS ROM draws only 7 mA when operating. The device incorporates a storage cell, with control circuitry, to automatically reduce current drain to 0.1 mA on chip deselection for a CMOS interface or only 1 mA for a TTL interface. A low-power option is offered to drop current drain to 0.1 mA when operating with a TTL interface.

Solid State Scientific, Inc., Commerce St., Montgomeryville, PA 18936. (215) 855-8400.

CIRCLE NO. 348

THE UNTOUCHABLES

DmC 4003

DATAMETRICS CORPORATION PRESENTS THE DmC 4003 ALPHANUMERIC, HIGH-SPEED, NON-IMPACT, MILITARY HALF-PAGE PRINTER.

The DmC 4003 is a proven 33-column, 2000 line per minute, non-impact Military specification half-page printer. Small size, light weight and high speed combine to make this unit suitable for critical space and aviation requirements. Freedom from adjustments, fewer moving parts, quieter operation and improved reliability under environmental extremes are some of the advantages of the 4003.

The DmC 4003. The only printer you may ever need.

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CIRCLE NO. 228

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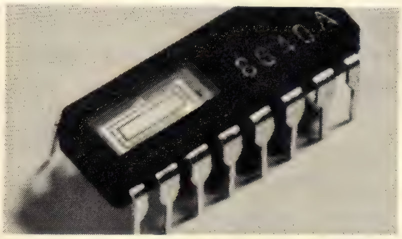
CIRCLE NO. 113

Clock-pulse IC generates 64 frequencies



A programmable clock-pulse generator IC, the Series 8640, generates 64 (57 unique) frequencies from the original frequency of its built-in crystal oscillator. The oscillator in the hybrid CMOS IC provides an original frequency with a wide range from 500 kHz to 1 MHz, which is programmed through a divider. Power consumption is only 1 mA. The device is TTL compatible and operates from a 5-V supply. Versions with original frequencies of 600 kHz, 768 kHz and 1 MHz are offered. Model 8640P supplies an output of 50 or 600 Hz only. The dividing IC is also available.

Epson America, 23844 Hawthorne Blvd., Torrance, CA 90505. (213) 378-2220. $8; stock to 12 wks.

CIRCLE NO. 349

Static 4-k RAMs need no clock or refresh

A series of 4096-bit RAMs, MSM 2114L, use fully static circuitry which requires no clocks or refreshing operation. The devices are directly interchangeable with all standard 2114L parts and feature TTL-compatible I/O and operation from a single 5-V power supply. The devices are organized as 1024 words × 4 bits. Maximum access time is 200 ns for the 2114L-2, 300 ns for the 2114L-3 and 450 ns for the 2114L.

OKI Semiconductor, 1333 Lawrence Expy., Suite 401, Santa Clara, CA 95051. (408) 984-4840. $5.45 to $6.75 (100 qty); stock.

CIRCLE NO. 354

Long-period IC timer drives relays

A long-period IC timer, AN6780, directly drives low-power relays. The timer provides delays between one second and one week. The device comes in a 7-pin SIP and operates from any voltage between 4.5 to 12 V dc. Maximum current draw is only 10 mA. AN6780 contains an oscillator, a 15-stage frequency divider, an output circuit and a power stage. For extra flexibility in circuit design, the user can select the oscillation frequency via an external resistor and capacitor. In addition to its use as a timer, the IC can be used as an ultra-low frequency oscillator or an accumulative timer.

Panasonic, One Panasonic Way, Secaucus, NJ 07094. (201) 348-7269. $1.05 (1000 qty); stock to 8 wks.

CIRCLE NO. 355

8-k PROMs offer time and power savings

Two fast 8-k bipolar PROMs and two 8-k SPROMs offer a choice of fast access time and low power consumption. The 29631A (1024 × 8) and 29651A (2048 × 4) are three-state PROMs with a maximum access time of 50 ns and an enable access time of 35 ns over a commercial temperature range. The 29633A (1024 × 8) and 29653A (2048 × 4) are three-state SPROMs with a maximum access time of 55 ns and an enable access time of 50 ns over a commercial temperature range. Power consumption in the SPROMs is accomplished through built-in power switches which turn off unselected devices.

Raytheon Semiconductor, 350 Ellis St., Mountain View, CA 94040. (415) 968-9211. $89.90 (100 qty).

CIRCLE NO. 356

HMOS-II transceiver drives the GPIB

An HMOS-II transceiver, the 8293, provides the high current drive and interface required by an IEEE-488 bus. Together with the 8291 talker/listener and the 8292 controller, the 8293 provides a complete IEEE-488 interface, replacing what previously was accomplished by an entire board of electronics. The 8293 chip contains nine line drivers and nine receivers. Each of the drivers and receivers contains the bus line terminations required to meet IEEE-488-1978 specifications, the receiver components needed to meet hysteresis requirements and power-up and power-down protection. Each driver can sink 48 mA.

Intel, 3065 Bowers Ave., Santa Clara, CA 95051. (408) 987-5020. $11.50 (100 qty).

CIRCLE NO. 357

Knobs for Anything you can Think of

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CIRCLE NO. 114

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THE EPROM PROGRAMMER DESIGNED
EXCLUSIVELY FOR THE AIM-65

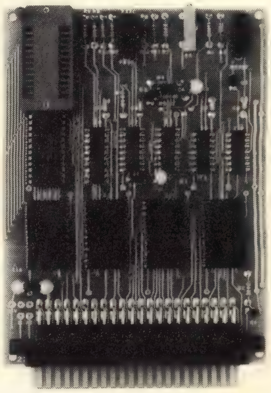
'Zero Insertion Force Socket' for EPROM programming

'Powerful Monitor' contains all programming routines.

'EPROM Expansion' for 8K of user programmed EPROM.

'Female Connector plugs directly onto the AIM-65 expansion bus. Male connector plugs into motherboards.

For more information on AIM-65 programming power call or write:



(415) 962-8237
CUBIT
2267 Old Middlefield Way
Mountain View, CA 94043

AIM-65 is a trademark of Rockwell International Corporation

CIRCLE NO. 115

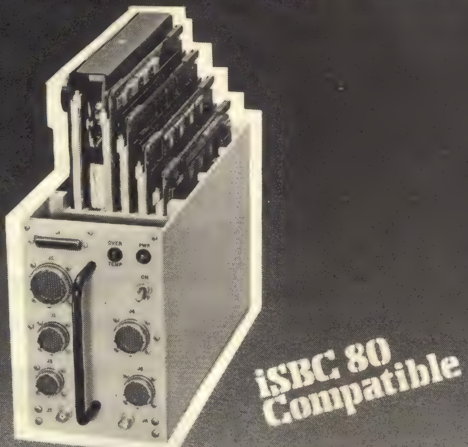
Void-free ferrite makes tape heads

A dense, fine-grain ferrite material, MND5100, makes tape heads for applications requiring good high-frequency and good bit-density performance. The Mn-Zn material is void-free. Density is 5.09 gm/cm^3. The extremely fine grain (mean grain size is 10 μm) and low porosity inhibit gap erosion and assure good wear characteristics. High permeability and saturation density give Mn-Zn ferrites an advantage for use in recording heads. Flux density is 5000 G maximum.

Ceramic Magnetics, 87 Fairfield Rd., Fairfield, NJ 07006. (201) 227-4222. Stock.

CIRCLE NO. 358

Ruggedized Microcomputer



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SECS 80 is a ruggedized version of Intel's iSBC* single-board computer. Even uses the same development system software.

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CIRCLE NO. 116

Test kit solves solder flux problems

A problem-solving chemical test kit contains 24 of the most-used soldering fluxes and chemicals. By consulting the kit's solderability chart, an engineer can determine the proper flux to use with any of 23 metals. The kit contains 10 different rosin fluxes, as well as inorganic fluxes, water-soluble organic fluxes, residue removers and metal surface activators.

Kester Solder, 4201 Wrightwood Ave., Chicago, IL 60639. (312) 235-1600. $30.

CIRCLE NO. 359

Conductive coat sticks to problem substrates

X-Coat 210-X conductive coating exhibits good adhesion to such problem substrates as injection-molded polycarbonate, polystyrene and ABS without "crazing" or degrading the plastic. The material can be applied and cured at room temperature. Cured resistance is 0.5 Ω/sq at a thickness of 2 to 3 mils. X-Coat 210-X contains no silver or other precious metals and is thus economical for rf shielding on plastic cabinets.

Electro-Kinetic Systems, 1000 Herald Sq., Aston, PA 19014. (215) 358-3440. $75/gal.

CIRCLE NO. 360

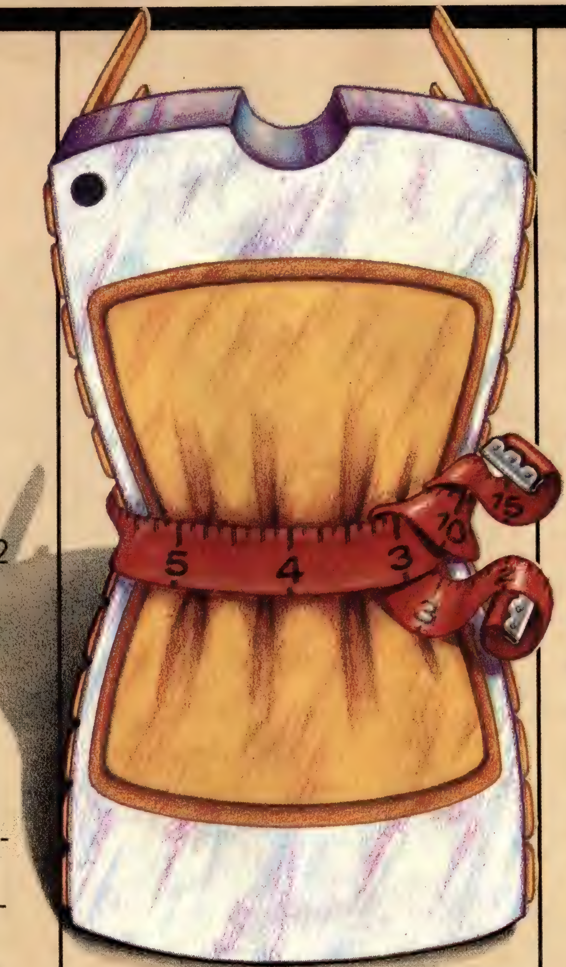
12-BITS, 16 PINS. THE END OF THE FAT DAC.

HE 12-BIT DAC FOR IGHT LAYOUTS.

ur compact new AD7542 s the world's first and only 2-bit D/A converter in a 16 in DIP. It needs only ⅓ the oard space of the usual 4 pin DIP, and since data is rought in as three 4-bit vords, only 4 data lines are equired rather than 12, vhich saves lots of PC board rack. This makes the AD7542 deal for applications requiring several DAC's per board.

DIRECT AND EASY μP INTERFACE.

Our slim, new DAC is designed specifically to interface directly to the data and control buses of 4, 8, and 16-bit microprocessors. The AD7542 interfaces to a μP as static RAM, with data loaded into it in three 4-bit words, using simple memory WRITE instructions. It even has a separate asynchronous clear input to simplify initialization during power up.



AND IT'S AN HONEST 12-BITS.

The AD7542 is a *real* 12 bit DAC, offering *true* 12 bit performance. Its monolithic CMOS construction gives you guaranteed 12 bit linearity over temperature (±½ LSB from T_{min} to T_{max}), and a low gain TC (typically ±2ppm/°C).

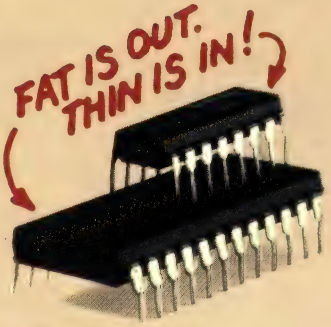
It operates on a +5V supply and features latch-up free operation. It also has all the analog versatility of CMOS DAC's, including 4-quadrant multiplication, and a low 40 mW power consumption.

ALL FOR AN INCREDIBLE PRICE.

You might think the world's smallest 12-bit DAC comes with a big price tag. It doesn't.

Our AD7542KN has a maximum linearity error of ±½ LSB. And our AD7542JN, with a maximum linearity error of ±1 LSB, costs less.

For the full story on this lean, new DAC, contact the local Analog Devices sales office listed below.



ANALOG DEVICES

WAY OUT IN FRONT.

Analog Devices, Inc., Box 280, Norwood, MA 02062; East Coast: (617) 329-4700; Midwest: (312) 894-3300; West Coast: (714) 842-1717; Texas: (214) 231-5094; Belgium: 031/37 48 03; Denmark: (02) 84 58 00; England: 01/94 10 46 6; France: 687-3411; Germany: 089/53 03 19; Japan: 03/26 36 82 6; Netherlands: 076/879 251; Switzerland: 022/315760; and representatives around the world.

CIRCLE NO. 166

Are you really into "SYSTEM"

System drafting means selecting the components used in your drafting technique for compatiblity and precision performance. It is counting on single-source responsiblity for these components. And it is knowing assistance is available for areas of your technique that may need improvement.

With "System" drafting, changes within your present technique are easy. Even easier are transitions from one system to another when you decide "there is a better way".

If the components and quality of your company's drafting products are your responsiblity, you should know more about the quality and performance value of the Koh-I-Noor products featured in the following drafting systems.

Black India Drawing Inks formulated to meet specific requirements for drawing on paper or film. The largest single-source selection includes Koh-I-Noor and Pelikan inks for film: Koh-I-Noor Rapid-O-Ink 3072, Koh-I-Noor Rapidraw 3084, and Pelikan "T" 9085 are special formulations to satisfy requirements for drying time, flow, opacity, and adhesion.

Special Ink-On-Film Erasers for removal of even the oldest ink lines when drawings need updating. A complete line of Koh-I-Noor and Pelikan erasers — liquid and dry — are available individually and in kit form.

Rapidraw Drafting Film with fine-toothed surface for maximum line definition. Virtually indestructible, optimum dimensional stability, unsurpassed storage life.

The KOH-I-NOOR "RAPIDRAW" System

Direct ink-on-film drafting for precision-perfect engineering drawings and microfilm blowbacks.

Koh-I-Noor Technical Pens and precision drawing points for exact line widths. Rapidograph 3065 and Rapidograph SL 3076 Series feature eighteen precision point sizes. Rapidometric 3095 Series features nine metric point sizes in a geometric progression based on the $\sqrt{2}$ (1.414): matching line widths on microfilm blowbacks is easy. All point sizes for all Technical Pen Series are available in stainless steel, jewel, or tungsten carbide.

The KOH-I-NOOR "KOH-I-LAR" System

Drafting on film with polymer leads. System components include:

- Koh-I-Lar Lead 2200-M; Koh-I-Lar wood-cased Drawing Pencils 1500-M. Each in six degrees, 6H through 3B.
- Koh-I-Noor Lead Holders 5612, 5613 and others.
- Koh-I-Noor Lead Pointers and Sharpeners 992-WC, 25960, 25961, 981, and 983.
- Koh-I-Noor Erasers, including Film Eraser 286 and Eraser Strip 289 with Holder 48.
- Rapidraw Drafting Film, the same virtually indestructible film used for the "Rapidraw" System.

RAFTING?

The KOH-I-NOOR Graphite System

Still the finest quality graphite vailable anywhere, and it has been ince 1790. Matched components for this opular system include:

- Koh-I-Noor Leads 2200 and 2200-I, Koh-I-Noor wood-cased Drawing Pencils 1500 and 1500-T, each in seventeen precision degrees.
- Koh-I-Noor Lead Holders 5611, 5616, 5619-N (0.5mm), 5623 (0.5mm), 5624 (0.3mm) and others.
- Koh-I-Noor and Pelikan Erasers, including Gum Cleaner 204 and Pelikan Special Green 9606-SP2.
- Koh-I-Noor Lead Pointers and Sharpeners including 992-WC, 25960, 25961, 981, and 983.
- Koh-I-Noor Drawing Papers — transparentized vellum and natural tracing bond, both 100% rag.

The KOH-I-NOOR "RAPIDRAW" Liquid-Ink Plotting System

The right pen points and the right inks add up to the optimum plotting efficiency for which your plotter was designed.

Koh-I-Noor Plotting Points, Pens, and Adaptors. Ten line widths available. Custom sizes on request. In stainless steel, jewel, and tungsten carbide.

Koh-I-Noor and Pelikan Inks for use on film and paper — among them, Koh-I-Noor "Universal" 3080, Koh-I-Noor 3000-F, 3000-PF and 3084 for film. And Koh-I-Noor 3089 and Pelikan 9065 for paper.

Koh-I-Noor Drafting Film and Drawing Papers in standard and special size sheets, pads, and rolls. Also gridded pads with blue dropout. On request, prepunched holes for drum plotters.

KOH-I-NOOR®

For in-depth information about Koh-I-Noor matched components for "System" drafting, fill in and return the coupon: Koh-I-Noor Rapidograph, Inc., 100 North Street, Bloomsbury, NJ 08804. In Canada: 1815 Meyerside Drive, Mississuaga, Ont. L5T 1B4

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☐ Koh-I-Noor & Pelikan Drawing Inks and Selection Chart, K-1072
☐ Faster and Easier Ink-on-Film Erasures, K-1043
☐ The "Rapidraw" System for direct ink-on-film drafting, K-913
☐ Koh-I-Noor Leads, Lead Holders, Pencils, Pointers, and Sharpeners, K-1073
☐ Koh-I-Noor Drawing Instruments and Sets, K-1075
☐ Koh-I-Noor "Rapidraw" Liquid-Ink Plotting System, K-1066
☐ Koh-I-Noor Templates, Scales, Triangles and Other Drawing Aids, K-1074
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CIRCLE NO. 118

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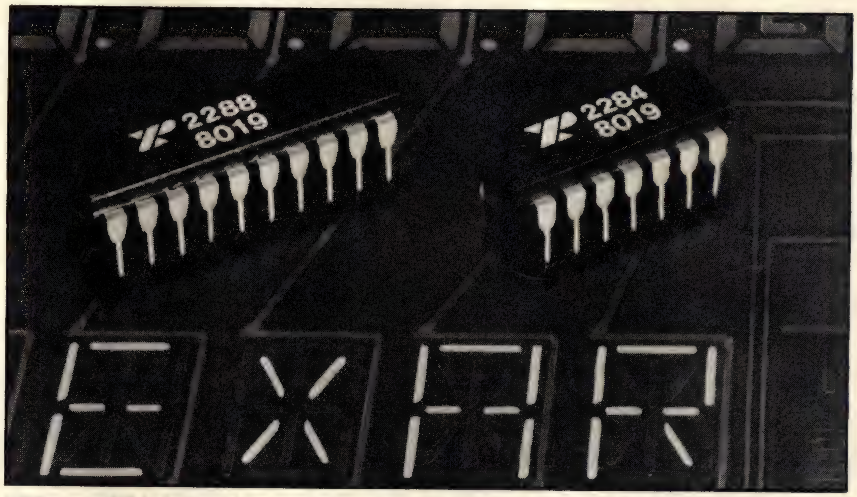
CIRCLE NO. 119

Mini-DIP ICs drive ac plasma displays



With monolithic integration, ac plasma display drivers handle 200-V systems at a reasonable cost.

For bright, reliable ac plasma displays, the existing driver circuitry made up of discrete or hybrid components exacts a heavy cost penalty. Now, simplified IC devices packaged in 14 or 20-pin DIPs handle the 200-V and 200-kHz requirements of ac plasma displays at a savings in board space, components and design effort.

The XR-2284 from Exar Integration Systems is a four-channel display driver; the XR-2288 is an eight-channel unit. Both can be used for either the segment or the column (digit) of an ac plasma display.

The driver for an ac plasma display must normally apply a trigger voltage exceeding 200 V across the display to light it. However, in actual practice, the trigger voltage is the sum of two quadrature voltages—one for the segment and one for the digit of the display. Each toggle voltage is one-half the trigger voltage, making it possible to reduce the driver to monolithic form without too much difficulty.

The driver outputs of the XR-2284 and XR-2288 are miniature SCRs triggered by TTL or even CMOS logic-level signals. A low-state control input applied to the integrated circuit causes the toggle voltage to be connected to the display.

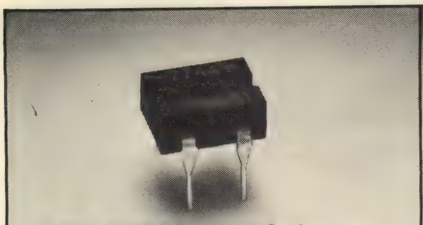
Both the XR-2284 and XR-2288 operate with toggle frequencies up to 200 kHz. Two other versions (XR-2284-P and XR-2288-P) work in 360-V ac plasma systems that require a minimum sustaining drive of 180-V for each driver output. For 240-V systems, requiring 120 V ac from each segment, Exar offers the XR-2284-CP and XR-2288-CP units. Power dissipation, in all versions, is about 50 mW per channel. The plastic-packaged devices operate over the temperature range from 0 to 75 C.

The price is reasonable: An XR-2284-CP costs $2.40 in lots of 100; an XR-2288-CP costs $5.80 for the same quantity.

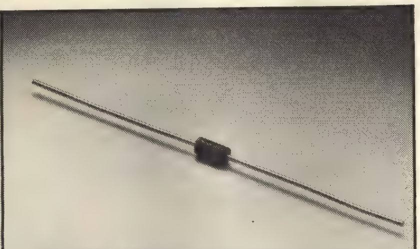
Exar Integrated Systems, Inc., 750 Palomar Ave., P.O. Box 62229, Sunnyvale, CA 94088. Steve Pass (408) 732-7970.

CIRCLE NO. 419

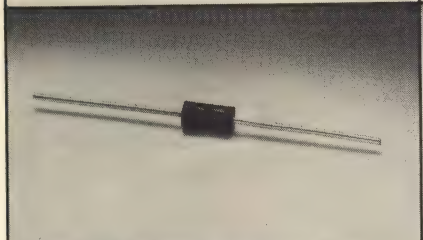
Which Schottky do you need?



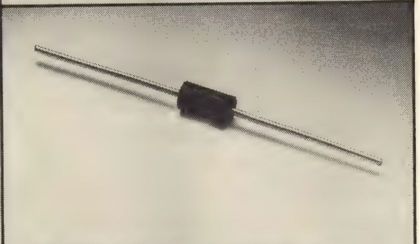
0.75A BRIDGE VSB51 Series: 10/20/30/40 V_{RRM} 0.65 V_F @ 0.75 mA I_F



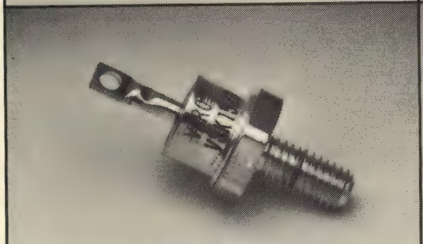
1A VSK 1 Series: 20/30/40 V_{RRM} 0.55 V_F @ 1.0 A I_F



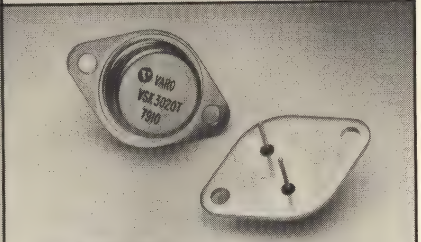
3A VSK 3 Series: 20/30/40 V_{RRM} 0.475 V_F @ 3.0 A I_F



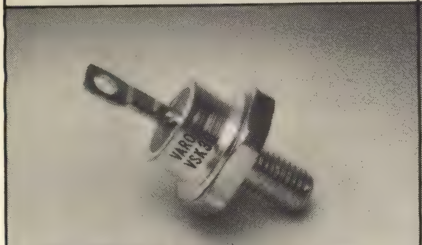
5A VSK 5 Series: 20/30/40 V_{RRM} 0.450 V_F @ A I_F



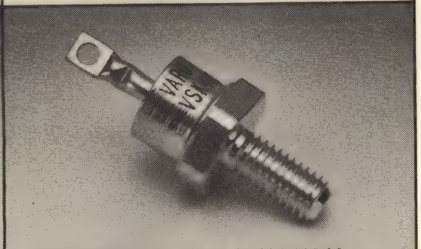
15A VSK15 Series: 20/30/40 V_{RRM} 0.60 V_F @15.0 A I_F



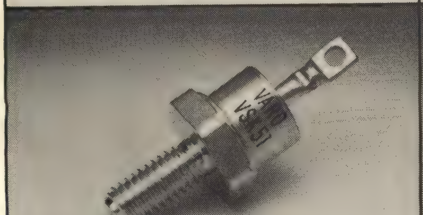
30A VSK30T Series: 20/30/40 V_{RRM} 0.64 V_F @ 15.0 A I_F



30A VSK30S Series: 20/45 V_{RRM} 0.64 V_F @ 30 A I_F



40A VSK40 Series: 20/30/40 V_{RRM} 0.62 V_F @ 40.0 A I_F



60A VSK51 Series: 45 V_{RRM} 0.60 V_F @ 60 A I_F

60A VSK51B Series: 45 V_{RRM} 0.63 V_F @ 60 A I_F

Look to Varo for the widest choice of Schottky devices for power supplies.

Efficiency is today's basic design criteria, and energy-saving begins in the power supply. That's why Varo has developed the most comprehensive line of Schottky devices around today. From a practical, dual in-line bridge family to a tough, 60 amp braided lead rectifier, we've got your requirements covered. Devices are available now; ready to meet your prototype or production schedules.

For application info, specs or a sample device, call: (214) 271-8511. Varo Semiconductor, Inc. Box 40676 Garland, Texas 75040.

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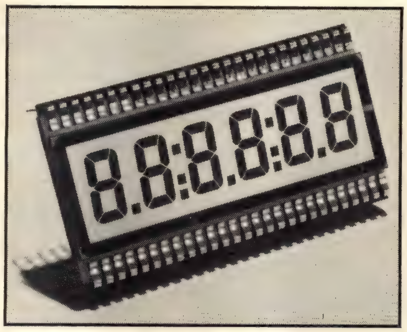
CIRCLE NO. 120

LCD provides big display with low power

While miniature liquid-crystal displays for wristwatches and pocket calculators are common, few feature 0.5-in. digits in large, multidigit packages. With the introduction of the 740-56 and 742-58 0.5-in. LCDs from Beckman Instruments, six and eight 7-segment digits are available in one package.



Intended for frequency counters, instrument panels, clocks and appliances, the LCD displays boast the low power consumption of their miniature counterparts, making them compatible with battery-powered CMOS drive circuitry. The displays will operate from supply voltages of 3 to 20 V and consume about 5 μW. The LCD digits respond in a reasonable time: 85 ms turn-on and 95 ms turn-off, both at 25 C. (Cold weather slows down response time, to about 125 ms at 0 C.)

The 6-digit 740-56 package is 2.75 × 1.4 in.; the 8-digit package is 3.7 × 1.4 in. Consult factory for prices. Delivery is from stock to six weeks.

Beckman Instruments Inc., Display System Div., 350 N. Hayden Rd., P.O. Box 3579, Scottsdale, AZ 85257. (602) 947-8371.

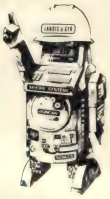
CIRCLE NO. 308

Lithium batteries give long-life power

Lithium batteries, designed to meet user requirements, give long-lasting performance in equipment requiring a dependable supply with closely predictable operation. Lithium anodes are used with such depolarizers as sulfur-dioxide and/or thionyl-chloride and any modifications of those elements. Open-circuit voltage is 3.67 V maximum, with capacity and rating depending on the size and interior design.

Battery Engineering, 80 Oak St., Newton, MA 02164. (617) 965-4449.

CIRCLE NO. 410



Our Little Printers Solve Big Problems

If your system requires a reliable printer but you're short on space, our PR series microprinters are the logical choice. Although we occupy a volume of only 2.3" H x 5.5" W x 6.0" D, we are not short on capability. Consider the features:

- 15 or 21 columns
- Full Alphanumeric
- Impact bar matrix print technique
- Two-color snap-in ribbon cartridge
- Plain paper
- Multiple copies
- Rugged construction
- Microprocessor compatible
- Optional DC operation

One thing we *are* short on, however----*price*.

Sodeco manufactures tape and ticket printers, microprocessor-based printer controllers, and printer accessories to suit a variety of applications for the OEM.

For more information on how our little printer can solve your problems call
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write Sodeco, Div. of
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Elmsford, N.Y. 10523.

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CIRCLE NO. 121

You don't have to be an IBM to cash in on custom IC's.

Item: Of course, all the big guys are heavy users of custom IC's, but most of our clients have sales volumes from $10 million to $100 million per year.

Item: SSi can provide you with cost-effective custom circuits even when your annual usage is only $100,000 per year.

Item: SSi does it all—from circuit concept through design and on-going production.

If you want it your way, call SSi, Director of Marketing, or send for our capability brochure today.

Silicon Systems incorporated, 14351 Myford Road, Tustin, California 92680. Phone: (714) 731-7110 or TWX 910-595-2809.

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CIRCLE NO. 122

Neon lamps snap into mounting holes

A series of neon indicators, 760/761 Series, snap-fit into mounting holes without additional hardware. The lamps require a 5/16-in. diameter hold with a minimum panel thickness of 0.03 in. The assembly consists of a neon C2A (NE2H) lamp with a 30-kΩ resistor. The 760 lens is flush while the 761 lens is a stovepipe type. Lenses come in white, green, red and amber. A chrome bezel is standard on the 761.

Wilbrecht Ledco, 240 Plato Blvd., St. Paul, MN 55107. (612) 222-2791.

CIRCLE NO. 361

LED indicators snap into panel holes

Subminiature 5210 series LED indicators snap-fit into a 3/16-in. diameter panel opening. The solid-state lamps use high-intensity red, green or yellow LEDs in a housing that provides 180°, wide-angle viewing. The parts fit securely into panels from 0.02 to 0.097-in. thick. No additional mounting hardware is needed. The indicators are supplied with 4-1/2-in. long wire leads with ends stripped and for soldering.

Industrial Devices, 7 Hudson Ave, Edgewater, NJ 07020. (201) 224-4700. $0.70 (1000 qty); stock.

CIRCLE NO. 362

Sealed switches ward off solvents and fluxes

Axial-travel switches withstand cleaning solvents, acid atmospheres, fluxes and salt spray. Silver contacts allow the switches to withstand higher current and inductive loads than standard reed switches. Normally-open and normally-closed contacts are available with the option of gold, tungsten or silver contacts. Spring clips or welded-on leads can be attached to the switches' end caps.

Electronic Applications, 4918 Santa Anita Ave., El Monte, CA 91734. (213) 442-3212.

CIRCLE NO. 363

Axial-Lead Schottky Rectifiers

25¢ in quantity

(for 20 volt, 3 amp unit)

Now! Reliable axial-lead Schottky rectifiers with extended performance characteristics; 20, 40, 60, and 80 volts—1, 3, and 5 amps—as low as 25¢ each in quantity. Use the coupon below for ***Free Evaluation Samples,*** judge the quality for yourself.

Send my Free Schottky samples.

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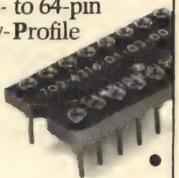
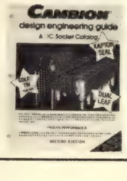
Current ________ Annual Usage ________
Name ________ Title ________
Company ________
Address ________
City ________ State ________ Zip ________
Phone ________

CIRCLE NO. 123





CAMBION V-L-P* IC SOCKETS

Now available in 2 different styles and in 8- to 64-pin positions, are Cambion's new, * Very-Low-Profile (.093") *Series 703-43XX* IC Sockets:

- **ROUND-PIN, SOLDER TAB VERSION** for mounting flush to PC boards. Use also as PROM carriers. Adhesive fit.
- **SQUARE-EDGE, WIRE-WRAPPABLE VERSION** orients each leaf of the 4-leaf Beryllium Copper spring contact to engage the *sides* and *edges* of IC leads for increased reliability! Press mount.

Machined body provides rigidity for pin alignment and for IC insertion/extraction. Ask for evaluation samples and the new IC Socket Catalog! Cambridge Thermionic Corp., 445 Concord Avenue, Cambridge, MA 02238, Tel: (617) 491-5400, Telex: 92-1480, TWX: (710) 320-6399.

CAMBION
The Right Connection.

CIRCLE NO. 125

SYSTEM 19 NOW PROGRAMS MORE THAN 200 DIFFERENT PROMS WITH ONLY ONE SOFTWARE SELECTABLE MODULE.

Our new System 19/UniPak lets you program most MOS and bipolar PROM'S from AMD, Fairchild, Harris, Intel, MMI, Motorola, National, Raytheon, Signetics and Texas Instruments. UniPak's software assembles the programming algorithm and selects the correct socket for 16, 18, 20, 24 and 28-pin PROMS.

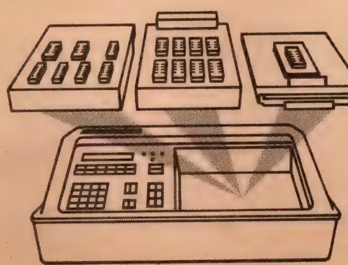
System 19/UniPak gives you design and purchasing freedom. This means you can select the best PROM for each application, and you can second-source for the best price and availability.

Semi-house approvals and easy calibration help maintain higher device yields. UniPak has earned written approval from device manufacturers. And easy calibration lets you keep performance within PROM manufacturers' specifications.

UniPak algorithms shorten programming time enhancing System 19's use as a production tool. UniPak is the first module to use a newly developed algorithm which makes it possible to program a 64K EPROM in less than half the time it takes to program a 16K EPROM using standard methods.

And the System 19/UniPak is easy to operate, with a minimum of operator training.

New System 19 concept is open ended to keep it state of the art. The System 19 is designed around a standard main frame and plug-in modules.

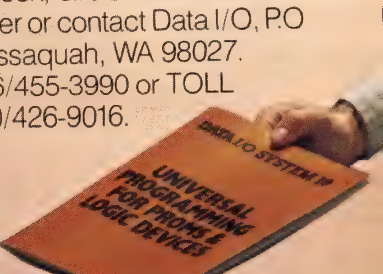


CIRCLE NO. 126

Modules available now include the UniPak, a gang programming pak for MOS devices, and a series of programming paks for logic devices and individual PROM families.

23 communication formats including six for development systems. Development systems, computers, teletypes and CRT terminals interface easily with the System 19. The System 19 accepts micro-processor instruction codes from Motorola, Intel, Tektronix, Fairchild, FutureData and other development systems without intermediary equipment.

Let us show you the future. The new Data I/O System 19/UniPak is available now. To make arrangements for a demonstration or to get your free copy of this valuable 32-page book, circle reader service number or contact Data I/O, P.O Box 308, Issaquah, WA 98027. Phone 206/455-3990 or TOLL FREE: 800/426-9016.



DATA I/O

Mil-spec transformers sit close to the board

PP Series power transformers, built to the environmental requirements of MIL-T-27, work well in PC-board applications where above-the-board space is minimal. Type PP11A, for example, measures only slightly more than 1 in. from the board-base to its top. Output range is 1 to 12 VA; dielectric strength, 1500 V rms for one minute; insulation resistance, 10,000 MΩ at 500 V dc. The supplies are suited for logic, operational amplifier and power supply applications where reliable performance under severe conditions is a vital consideration.

Pan-Magnetics, 137 Eucalyptus Dr., El Segundo, CA 90245. (213) 322-1075. 6 to 12 wks.

CIRCLE NO. 364

Position transducers conform to user specs

High Gain Inductosyn linear and rotary position transducers meet the size, accuracy and environmental requirements of manufacturers of measuring equipment, computer disk drives and other precision mechanisms. Units with accuracies of ±50 μin. and repeatability to ±20 μin. can be supplied. Pitch or cycle length are designed to custom specifications with typical units in current production offering pitches of 0.01, 0.0202125, 0.2 in. and 1 mm. Auxiliary control signals, such as End of Travel or Track Location, can be included. Any substrate material, from cast aluminum to fiberglass tape, can be used. The thermal time constant of the substrate can be adjusted to match a user's structure, thus eliminating inaccuracies during warmup. The transducers operate in strong magnetic fields without pickup or loss of accuracy.

Farrand Controls, 99 Wall St., Valhalla, NY 10595. (914) 761-2600. From $10 (OEM qty).

CIRCLE NO. 365

Bit - Slice

NIGHTMARES

Microprogramming Nightmares . . . That STEP-2 Has Banished

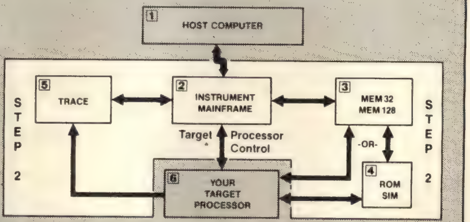
NIGHTMARE #		NIGHTMARE COST*
#1	We only used up $50,000 worth of PROM's during development. What do you mean, Production is short of them?	$50,000 + Late Product
#2	Our bit-slice system almost works.	Bankruptcy?
#3	Real-time testing wasn't important. Of course Charlie's still "tightening" code.	Maintainability + $100,000?
#4	Charlie's home built simulator didn't break down until after he left for Germany.	Project Delay + $32,000?
#5	How can they scrap the project? We have only been debugging for six months.	Market Share + $250,000?
#6	It is just another 2 hour assembly	Frustation

Get Rid Of Your Nightmare . . . Wake Up To STEP-2

Not just another bit-slice development system . . . a complete solution to your microcoding problems:

- Microcode development in-circuit
- Real-time memory simulation
- Fast word-oriented microcode editing
- Real-time trace of processor activity

STEP-2 surrounds your processor, giving you the flexibility needed to turn your nightmare into a sweet dream. With STEP-2, you spot a bug, track it, recode, kill it . . . and sleep nights.



1 Use **any** computer to develop microcode: STEP will provide the meta assembler if you need one. Advantages: less startup time — no new operating system to learn — faster code development — quicker assemblies, simultaneous hardware and software development — less cost using existing computer. No computer? In many cases STEP-2 *plus* a computer costs less than our nearest competitor!

2 STEP-2 is a standalone interactive development instrument with: integral CRT, keyboard, word oriented microcode editor, communications facility with upload/download routines, control port for target processor, reconfigurable memory, and simple, fast-learn command routines. All in the base price.

3 Real-time reconfigurable memory simulation from 8 to 192 bits. You configure STEP-2 array size for each new project. Choose from both memory families:

- MEM 32 for fast controller applications: depth to 2k, worst case access time to **36ns**
- MEM 128 for processing applications: depths to 48k, worst case access time to **50ns**

Bonus: STEP-2 handles one memory array or several, pipelined or not.

4 ROM simulation cable family allows you to plug into existing PROM sockets on any target processor.

5 Real-time Trace for synchronous capture of processor states at cycle times to 90ns. A selection of triggering equations and modes from self-teaching menus simplify complex setups.

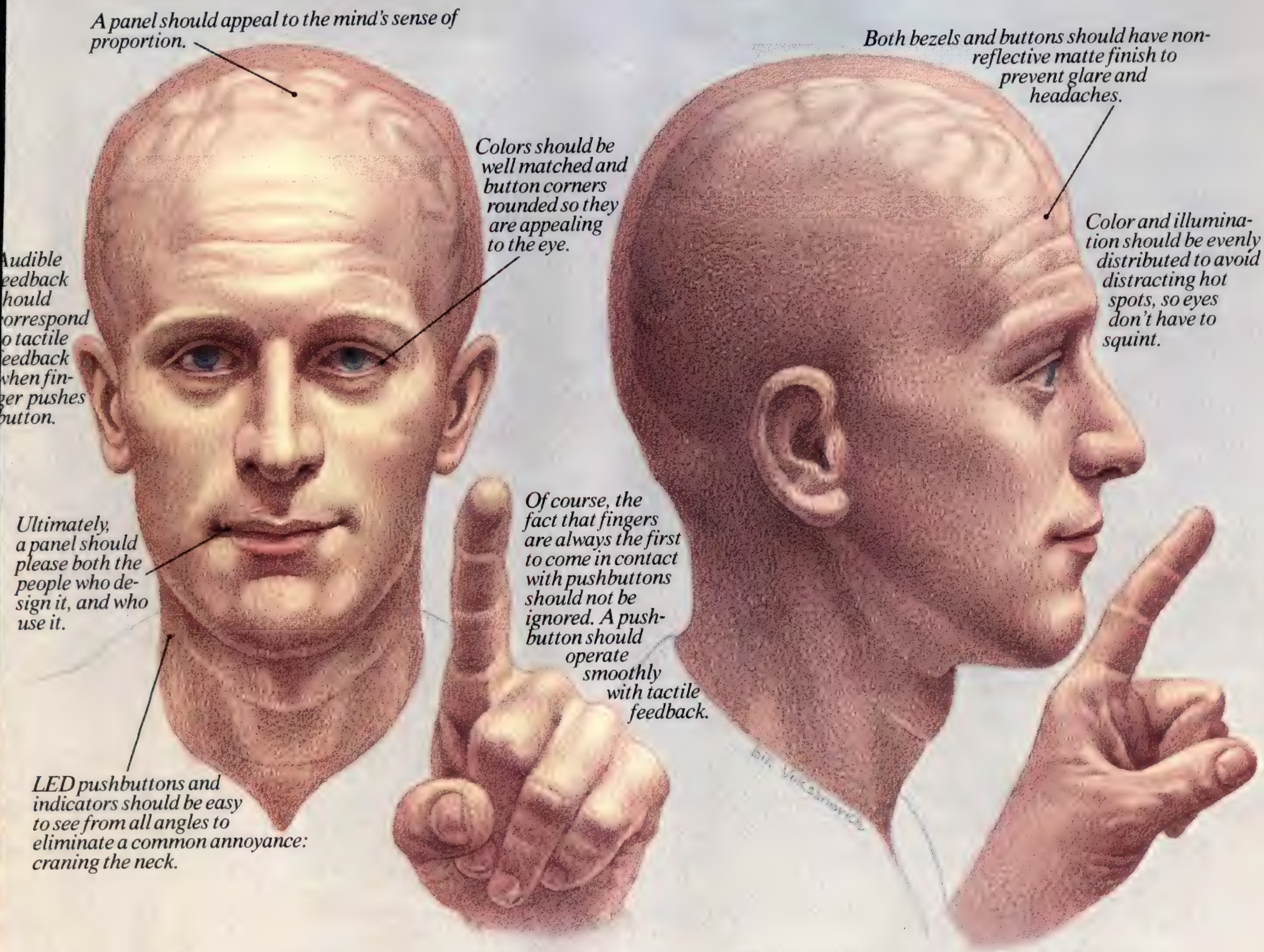
6 Your processor/controller under development is supported by STEP-2 *regardless* of configuration. Doubt it? Call Curtis at (408) 733-7837.

***Good equipment pays for itself. STEP-2 is priced from $4,950 to $49,500. Call STEP today for a quote.**

STEP
ENGINEERING
P.O. Box 61166, 757 Pastoria Ave.
Sunnyvale, CA 94088 • (408) 733-7837

CIRCLE NO. 127

A pushbutton panel should be designed for parts of the body besides fingers.



A panel should appeal to the mind's sense of proportion.

Both bezels and buttons should have non-reflective matte finish to prevent glare and headaches.

Colors should be well matched and button corners rounded so they are appealing to the eye.

Color and illumination should be evenly distributed to avoid distracting hot spots, so eyes don't have to squint.

Audible eedback hould correspond o tactile eedback when finger pushes utton.

Ultimately, a panel should please both the people who design it, and who use it.

Of course, the fact that fingers are always the first to come in contact with pushbuttons should not be ignored. A pushbutton should operate smoothly with tactile feedback.

LED pushbuttons and indicators should be easy to see from all angles to eliminate a common annoyance: craning the neck.

When we designed the Advanced Manual Line (AML), we included everything a designer could want.

Like a broad selection of pushbuttons, indicators, paddles and rockers. In a variety of shapes, sizes and colors. With LED, incandescent or neon illumination.

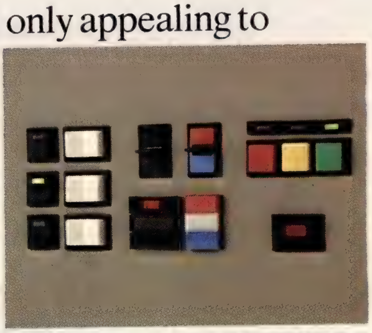
But what really makes AML unique is a small detail that others seem to have overlooked.

The people who use them. Which is why they're not only appealing to fingers, but other parts of the body as well.

That isn't to say we've neglected the person who puts the panel together. Because AML has single level termination for easy wiring and low installation cost. And electrical flexibility that ranges from solid state to electronic and power duty control.

With AML, you clearly design panels around people who use them, and not just their fingers.

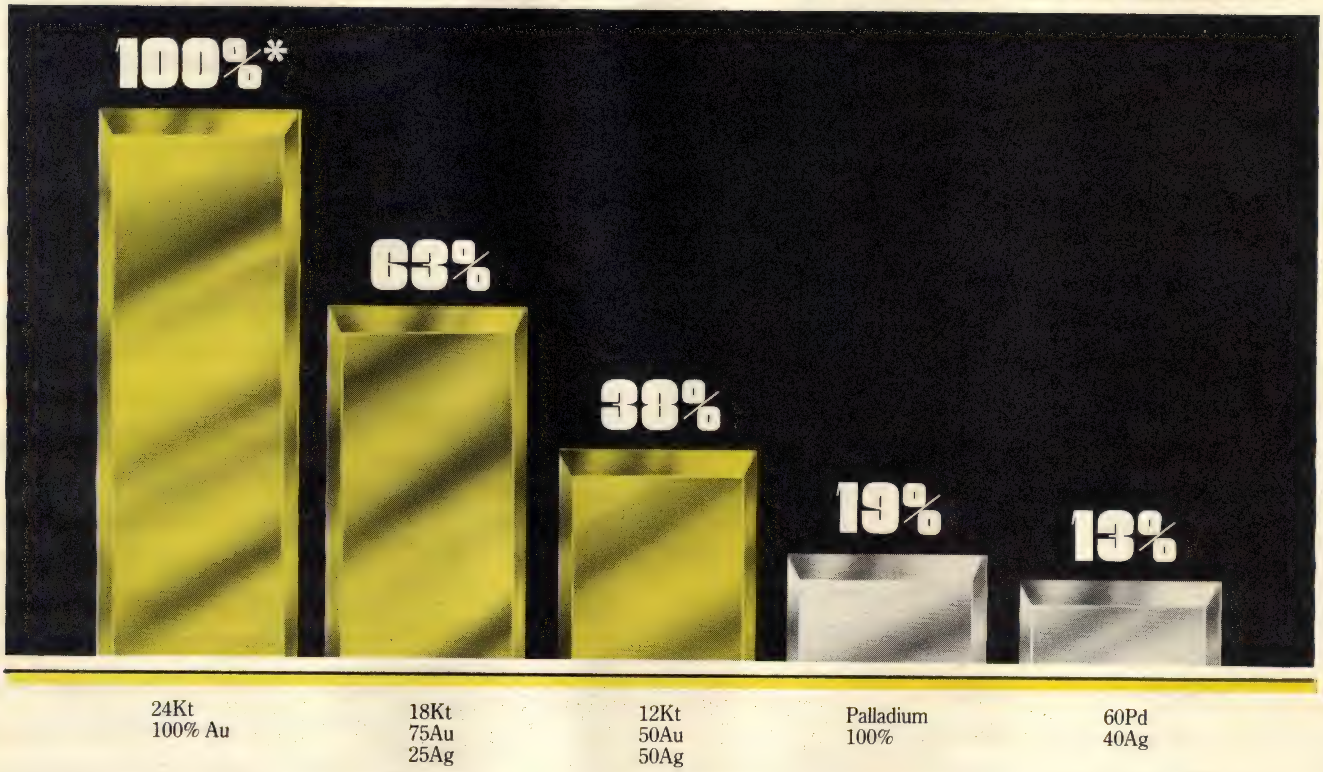
For details, and the location of our sales offices and distributors around the world, write MICRO SWITCH, Freeport, Illinois 61032. Or call 815-235-6600.



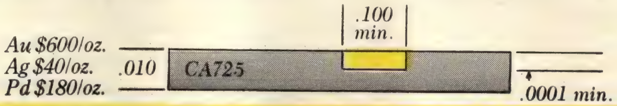
MICRO SWITCH
a Honeywell Division

CIRCLE NO. 128 FOR DATA

HOW INLAY–CLAD CONTACT ALLOYS CAN SAVE YOU MONEY



** Calculations based on precious metal content and appropriate density plus market price as shown.*



As this chart illustrates, you can now select palladium and Pd alloys in addition to gold alloys which offer dramatic cost reductions over pure gold while providing the performance criteria needed in the design and production of electronic contacts. TMI offers these alloys in selective stripes ranging down to .000010″ thickness and as narrow as .055″. In addition to the alloys shown on the chart, many other combinations of dollar-saving gold and palladium alloys, which cannot be electroplated, are available for specific requirements. Contact applications which are successfully using 12Kt gold alloy and palladium are currently in production.

Some of the technical advantages of wrought contact alloys are:

- Excellent Formability
- Low Porosity
- More Dense Structure
- More Consistent Properties
- Wide Range of Hardness

TMI inlays of pure palladium and its alloys provide an economical replacement for gold while still retaining a noble alloy's advantages. *60 Pd/40 Ag is an optimum alloy for minimizing tarnish film and reducing polymer formation.*

Ask for TMI reports on "Properties of Inlay Gold Wrought Alloys" and "Properties of Palladium in Contacts and Connectors" or ask TMI to help you make the most effective use of clad inlay metals.

TMI

TECHNICAL MATERIALS, INC.
5 Wellington Rd., Lincoln
Rhode Island 02865
Telephone: (401) 333-1700

TECHNICAL MATERIALS INC. (UK) LTD.
C2, Stafford Park 11
Telford, Shropshire TF3 3BJ
TX No. 35359 (TELDEV)
Tel. (0952) 615991/2

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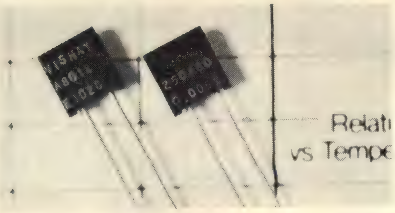
CIRCLE NO. 129

Precision resistor comes in values to 250 k



A precision resistor, Model E102C, comes in values from 100 kΩ to 250 kΩ with resistance tolerances from ±0.005% to ±1%. The part uses wrap-around "paddle lead" construction for a low thermal EMF of only 0.5 μV/°C maximum. Each lead has only a single weld connection, located away from the lead's point of entry into the case, eliminating ribbon interconnections. Nominal tempco is 0.6 ppm/°C from 0 to 25 C and −0.6 ppm/°C from 25 to 60 C. Standard tempco spread from nominal is only ±1.5 ppm/°C from 0 to 25 C and 25 C to 60 C. Selected tempco tracking can be as close as 0.5 ppm/°C throughout the full temperature range. Current noise is less than 0.025 μV rms/V of applied voltage. Nominal dimensions of the molded case are 0.302 × 0.326 × 0.105 in.

Vishay Resistive Systems Group, 63 Lincoln Hwy., Malvern, PA 19355. (215) 644-1300. stock to 8 wks.

CIRCLE NO. 366

Tiny bead thermistors monitor temperature

Glass-coated bead thermistors, Series B35, meet or exceed the performance requirements of MIL-T-23648. The parts are available with adjacent or opposite leads in standard resistance values from 30 Ω to 30 MΩ. The thermistors consists of a small ellipsoid of metal oxides, sintered about a pair of 0.004-in. diameter platinum alloy wires. The bead is hermetically sealed with a shock-resistant glass coating.

Thermometrics, 808 U.S. Hwy. 1, Edison, NJ 08817. (201) 287-2870. Typical $1.40 (100 qty); stock to 4 wks.

CIRCLE NO. 367

Lithium cells power watch circuits

A line of lithium cells provide additional power source options for battery-powered watches. The line includes 1.5-V cells with iron-sulfide cathodes and 3-V cells with manganese-dioxide cathodes. Both types offer high resistance to electrolyte leakage and long shelf life.

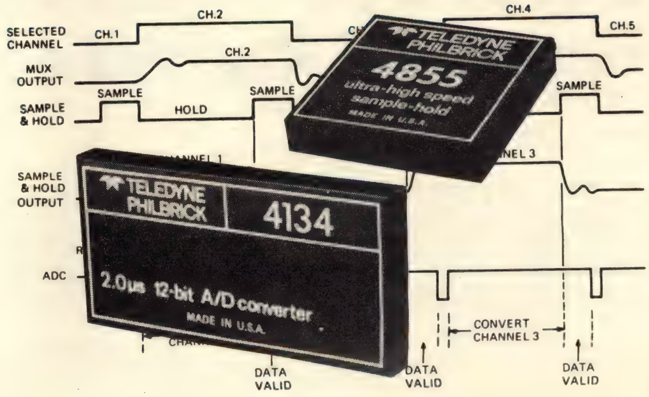
Union Carbide, 270 Park Ave., New York, NY 10017. (212) 551-3763.

CIRCLE NO. 368

DATA ACQUISITION: THRU-PUT AT 488 kHz

You can obtain true 12-bit performance . . . by combining Teledyne Philbrick's 4855 high-speed sample-hold with our new 4134 12-bit, progressive approximation A-to-D converter. Data acquisition thru-put rates of 488 kHz are achieved without the sacrifice of accuracy. With these and our other data conversion products, combinations of thru-put/resolution trade offs can be attained to solve your design problems.

For additional information and special OEM pricing, contact Ted Serafin, Product Marketing Manager at (617) 329-1600, ext. 354.



TELEDYNE PHILBRICK

Data Converters, V/F/V Converters, Linears, Nonlinears, Power Supplies
Allied Drive at Route 128, Dedham, MA 02026
Tel: (617) 329-1600 TWX: (710) 348-6726 Telex: 92-4439

CIRCLE NO. 133

16-Pin DIPS:
Log/Anti Log Amp,
Peak Sense/Holds

WIDE BAND LOG AMP
DC to 10MHz freq response
80dB min dynamic range
V or I input mode—bipolar
−65°C to +125°C operation
±15V supply voltage
Model 2910 $61.50 (3-9)

LOW COST SENSE/HOLD
100ns max acq time/10V pulse
30ns max acq time /1V pulse
100mV/ms decay, Cx=100pF
TTL, CMOS logic compatible
50ns max reset/gate turn-on
Model 5902 $51.00 (3-9)

HIGH SPEED SENSE/HOLD
20ns max acq time, for 5V pulse
+5V max input voltage
150mV/ms decay, Cx=100pF
TTL, CMOS logic compatible
50ns max reset/gate turn-on
Model 5905 $64.50 (3-9)

MIL Packages also available
Request 72-page Op Amp,
Function Module Catalog.

oei Box11140 • Tucson, AZ 85734 • (602)624-8358 • TWX:910-952-1283

CIRCLE NO. 134

Best Source
For
Microprocessor
Quartz Crystals

We offer top quality, low price, a wide choice of frequencies and **fast** delivery. Write or phone for complete information including quantity discounts. You can depend on us. **We deliver!**

WES-CON

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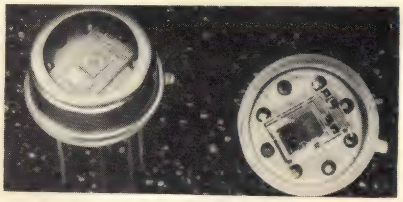
525 University Ave., Suite 705 Palo Alto, CA 94301
Telephone (415) 327-4051 • TELEX 345549

CIRCLE NO. 135

Substrate improves optical receiver



Optical receivers for through-the-air or fiber optic reception, R-1900 and R-1000, contain all their circuitry on a single substrate for improved performance. A receiver, consisting of a p-i-n diode and a thin-film, hybrid transimpedance amplifier—all on one substrate—minimizes cost and improves shock and vibration resistance. All circuitry is contained within a TO-5 package with four active pins. Receiver bandwidth is 100 MHz with spectral response from 400 to 1100 nm. A family member, R-1000, has a dc to 0.25-MHz bandwidth.

Meret, 1815 24th St., Santa Monica, CA 90404. (213) 828-7496. $99 (R-1900); $71 (R-1000) (10 qty); stock.

CIRCLE NO. 370

Image intensifier tube offers large active area

A proximity-focused image intensifier tube, F-4110, offers an active diameter of 75 mm. The device can be supplied with a selection of input windows and photocathode combinations for applications within a UV to near IR region. A typical output window is a plano-plano fiber optic with an aluminized P-20 phosphor screen. Since the tube is proximity focused, its size is small and there is minimal distortion over its active image area. A separate power supply can be furnished.

ITT Electro-Optical, 3700 E. Pontiac St., Fort Wayne, IN 46803. $7600; 12 to 24 wks.

CIRCLE NO. 371

TYPE 287P STYRACON® CAPACITORS

LOW COST, TIGHT CAPACITANCE TOLERANCE

- Polystyrene film dielectric . . . rugged epoxy coating.
- Capacitance tolerances . . . ±1%, ±2%, ±3%.
- Extended foil construction avoids reliability and inductance problems of laid-in-lead imports.
- Short lead times . . . unlike uncertain deliveries of imported film capacitors.
- Standard capacitance values from 100 pF to .1 μF. Voltage ratings of 50 and 100 WVDC.

Write for Engineering Bulletin 2052.3 to
Technical Literature Service, Sprague Electric Co.,
347 Marshall St., North Adams, Mass. 01247

4SP-0102

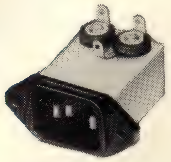
THE BROAD-LINE PRODUCER OF ELECTRONIC PARTS

SPRAGUE
THE MARK OF RELIABILITY
a subsidiary of **GK Technologies** Incorporated

CIRCLE NO. 136

SERIES JX5400 FILTERS

. . . U.L. Recognized



SUPPRESS POWER LINE EMI

- Reduce noise emanating from or interfering with equipment.
- Furnished in 4 different circuit configurations suppressing both common mode (line-to-ground) and differential mode (line-to-line) interference.
- Ideal for filtering external transients in 150 KHz—30 MHz range in equipment containing low-level logic circuitry.

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347 Marshall St., North Adams, Mass. 01247.

4SF-7152R1

THE BROAD-LINE PRODUCER OF ELECTRONIC PARTS

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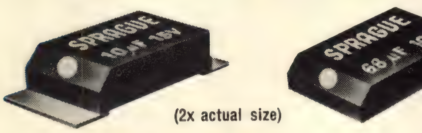
CIRCLE NO. 217

TYPE 193D DOMINO® CAPACITORS



(2x actual size)

HIGH μF, LOW PROFILE

- Solid-tantalum capacitors with two standard terminal configurations . . . leadless with flush solderable pads, or extended-tabs.
- Fully-molded construction eliminates possibility of mechanical damage during handling and mounting.
- Excellent *stability* . . . undesirable parametric changes and catastrophic failures due to mechanical degradation are minimized.
- Capacitance values from .082 to 100 μF, voltage ratings from 3 to 35 WVDC.
- For −55° C to +85° C operation . . . to +125° C with voltage derating.

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4SE-8141R1

THE BROAD-LINE PRODUCER OF ELECTRONIC PARTS

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a subsidiary of **GK Technologies** Incorporated

CIRCLE NO. 218

TYPE 834P METFILM® 'S' CAPACITORS

THE 'ZERO TC' CAPACITOR

- Metallized polysulfone-film section in rectangular molded plastic case offers superior electrical characteristics, small size, rugged construction.
- Capacitance change is typically ±0.25% over broad temperature range of −40°C to +125°C.
- Low dissipation factor (high Q), low dielectric absorption.
- Capacitance tolerances as close as ±1%.

Write for Engineering Bulletin 2610 to
Technical Literature Service, Sprague Electric Co.,
347 Marshall St., North Adams, Mass. 01247.

4SD-8123R1

Dearborn electronics division
SPRAGUE ELECTRIC COMPANY

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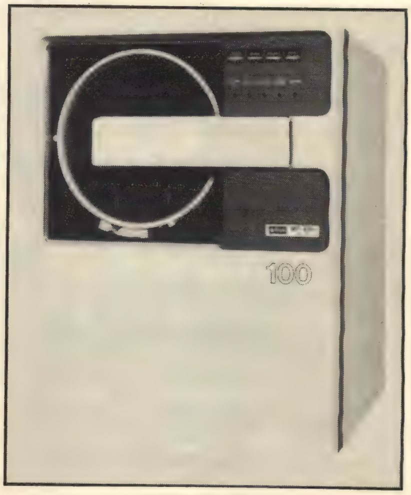
CIRCLE NO. 219

Tape drives stress reliability

Switches with no moving parts and a simple tape path remove the MT-100 Series of magnetic-tape drives from two of the dangers common to other tape units: damage to the tape from the drive itself and mechanical failure of the switch. The line of compact, low-cost drives from Hitachi can operate in either the GCR recording mode, at a density of 6250 bpi, or the PE mode, at a density of 1600 bpi.

Currently, three models of the family are available. The MT102 has a tape speed of 50 ips; transfers 312 kbytes/s under GCR and 80 under PE recording; and rewinds at 250 ips. The MT104 has a tape speed of 80 ips; transfers 500 kbytes/s under GCR and 128 under PE; and rewinds at 320 ips. The MT106 has a tape speed of 125 ips; transfers 781 kbytes/s under GCR and 200 under PE; and rewinds at 375 ips.



The drives will cost about $7000, with GCR formatter. Availability is 90 days.

Hitachi America, Ltd., 100 California St., San Francisco, CA 94111. Kiyoshi Fudono (415) 981-7871.

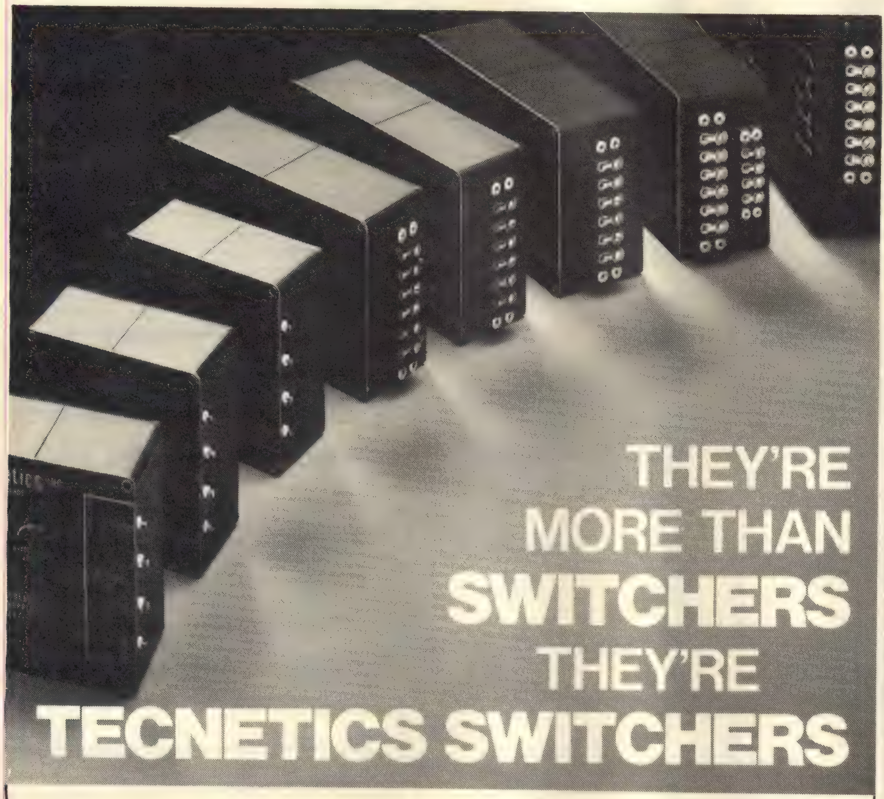
CIRCLE NO. 307

Flexible disk ends warp problems

An 8-in. flexible disk, the Optima Series XE, eliminates problems of disk warp caused by storing disks in automobiles or exposing them to direct sunlight or high-temperature environments. The single-sided disk is capable of sustaining operating and storage temperatures up to 160 F. Maximum recording density is 6537 fc/in.

Verbatim, 323 Soquel Way, Sunnyvale, CA 94087. (408) 245-4400.

CIRCLE NO. 372



A Tecnetics switching power supply is better than most for good reason. First of all, we pioneered pulse width modulation techniques to achieve higher efficiency, cooler operation and compactness. In fact, our 1974 catalog offered switchers as standard items.

Secondly, Tecnetics is a major supplier of high rel switchers to the defense and aerospace industries. These are people that demand the most in reliability and performance.

And finally, Tecnetics today offers nearly 100 switchers, both AC to DC and DC to DC, with power ratings between 25 and 200 watts. They offer EMI filtration, efficiencies up to 92%, overload protection and multiple outputs.

Write for our 1980 catalog today. Look at the specs and you'll see why the switch is on to Tecnetics switchers.

Series	Power	Output	Input	Freq.	Price
3000	25-150	5-48VDC	28 & 48 VDC		$440-665
4000	25-200	5-48VDC	115 VAC	360-440 Hz	440-1030
6200	200	5-48VDC	115 VAC	47-440 Hz	725

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(303) 442-3837 TWX 910-940-3246

CIRCLE NO. 137

For Twisted Pairs... WOVEN

'way to go!

Yes, you can depend on Woven Electronics every time. It's the way to go for twisted pairs, triads, or quads. Fast and easy lead exposure, saves time in handling and installation and because its woven as flat ribbon cable it facilitates routing and conserves space in packaging. Quick delivery from stock 13, 25 and 50 sets, 26 AWG and 28 AWG. For twisted pairs...WOVEN is the way to go. Write or call Woven Electronics,

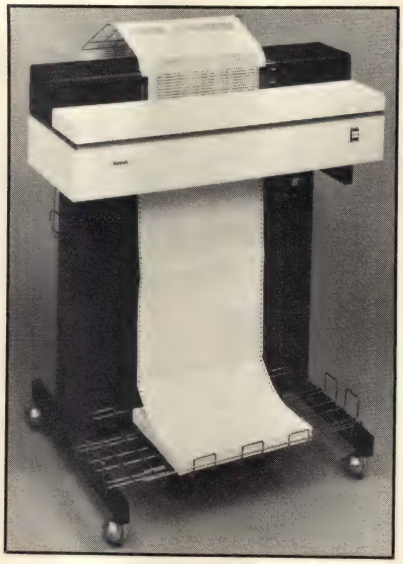
WOVEN ELECTRONICS®
A Division of Southern Weaving Company
P.O. Box 189 Mauldin, S.C. 29662 Phone 803/963-5131

CIRCLE NO. 138

Printer/plotter works in four colors

A microprocessor-controlled, four-color, dot-matrix printer/plotter will serve users needing both graphics and alphanumerics in color. The Model 4100 switches quickly between graphic and alphanumeric modes, while printing at 60 lines/min. and plotting an 11-in. form in 3 min., average.

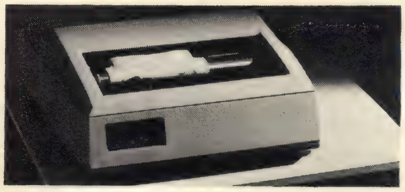
Separate cartridge ribbons and print heads are used for each primary color (magenta, cyan and yellow) as well as black. Both color and black can be printed concurrently—faster than with machines that synthesize black by combining dots from the other three colors.



The printer/plotter will be marketed with a standard 8-bit Centronics interface. An optional format control is available with EAROMs. Priced at $12,000, the 4100 will be available in limited quantities in August.

Ramtek Corp., 2211 Lawson Lane, Santa Clara, CA 95050. (480) 988-2211. **CIRCLE NO. 139**

Two-way head travel increases printer output



Bi-directional head travel increases the throughput speed of the T1705 serial printer to 200 lines per minute. The printer, with a buffered RS-232 interface, is capable of 160 characters/s. Features include dual-tractor paper handling and switch selectable 6 or 8 line/in. spacing. Top of forms and double-wide character printing are also switch selectable. The print head can be easily changed in the field by an operator.

Tally, 8301 S. 180th St., Kent, WA 98031. (206) 251-5524. $1895; 4 wks. **CIRCLE NO. 373**

DOSC Introduces

THE MOST POWERFUL MICROCOMPUTER AVAILABLE TODAY!

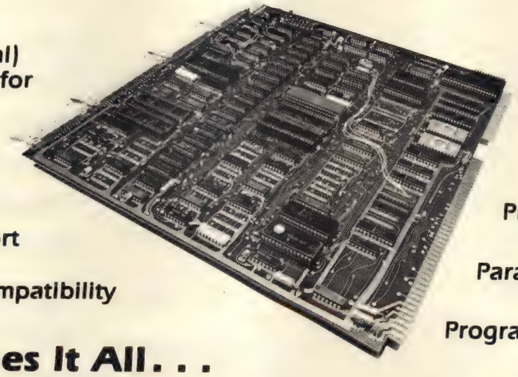
TCB-85/
Total Computer Board

48K RAM (64K optional) with sockets available for up to 16K PROM

Strobed or Scanned Keyboard Interface

Serial I/O Port

Intel Multibus™ Compatibility



Dual-Density/Double-Sided Floppy Disk Controller

Programmable CRT Controller

Parallel Printer Interface

Programmable Interrupt Controller

One Board Does It All . . .

Complete as a stand-alone or used with Intel's Multibus™, the TCB-85 combines outstanding performance and reliability with an impressive variety of features. . .all in one compact, low priced package.

In addition to an extremely powerful I/O capability and high level of integration, the TCB-85 is capable of supporting CP/M and PASCAL with DOSC PROMs.

The TCB-85 uses the Intel 8085A CPU and can optionally be ordered with the Intel 8085A-2/10 MHz CPU.

TM Trademark Intel Corporation

Evaluation units are now available for immediate delivery and priced at just $1275 in quantities of 100.

Get All the Details Now!
Contact Alex Newman at (516) 621-6640

DOSC
OEM PRODUCTS DIVISION
175 I.U. Willets Road, Albertson, NY 11507

CIRCLE NO. 139

If you can answer these questions, you must be designing in transient protection with GE-MOV® II varistors

Q: Why do I have to protect my solid state circuits from transients?

A: Damaging high voltage transients can attack your circuits through the power line, telephone lines, data lines or by current switching in inductances. They can damage expensive power semiconductors, microprocessors and other digital circuitry. Proper transient protection is essential in circuits designed for reliable, low downtime operation.

Q: How *should* I protect my circuit?

A: A metal oxide varistor provides reliability without requiring overrated semiconductor devices which add to circuit cost. More designers specify GE-MOV® II varistors than any other component specifically designed for transient protection. GE-MOV® has proven cost effective even in the cost-conscious consumer television receiver industry.

Q: What is a GE-MOV® II varistor?

A: The GE-MOV® II varistor, introduced by General Electric in 1972, is a voltage dependent, symmetrical resistor which when exposed to high energy voltage transients changes its impedance from a very high standby value to a very low conducting value, thus clamping the voltage to a safe level. The dangerous energy of the incoming high voltage transient is absorbed by the GE-MOV® II varistor, thus protecting voltage sensitive circuit components.

Q: Won't the addition of a GE-MOV® II varistor add to the cost of my circuit?

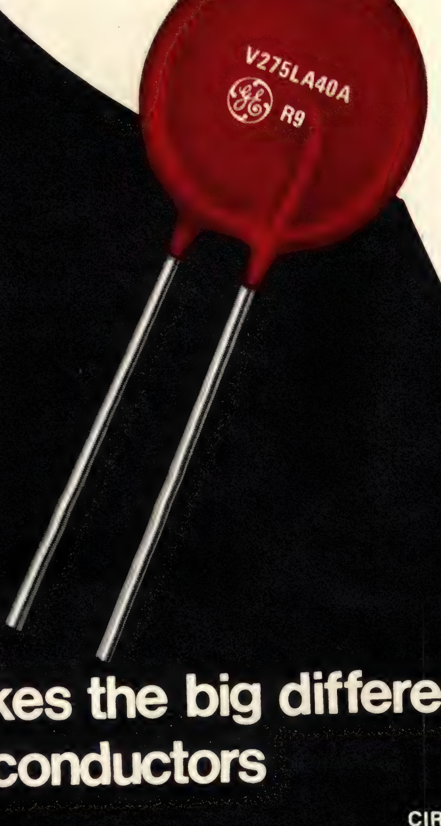
A: The answer is threefold—

1. Using a GE-MOV® II varistor eliminates the need for over-rated components and their additional costs to protect from transients.
2. In an improperly protected circuit, a voltage spike can damage a microprocessor or integrated circuit, that usually costs more than the GE-MOV® II varistor, and causes system shutdown and servicing, which usually costs more than any of the components involved.
3. Isn't the reliability of your product worth 25¢*? You can protect your circuit and help protect your company's name with a GE-MOV® II varistor.

Q: How do I select the proper GE-MOV® II varistor to protect my circuit?

A: First: the varistor should have a peak operating voltage rating that is close to, yet higher than, the normal peak ac-line voltage. Next, determine the energy level of the transient by the term $\frac{1}{2} LI^2$ where I is the peak magnetizing current flow in inductance L, which stores the transient energy in its field. Use the peak current as the expected transient current level. Then select the proper GE-MOV® II varistor from the GE Transient Voltage Manual or Short Form Catalog.

For selection assistance contact your General Electric electronic component sales office, authorized distributor or write General Electric Company, West Genesee Street, Mail Drop 14, Auburn, New York, 13021 or call (315) 253-7321, extension 283.



*Price based on a V130LA10A in quantities of 10,000.

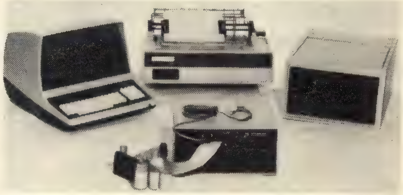
222.25

GE makes the big difference in semiconductors

GENERAL ELECTRIC

CIRCLE NO. 140

Emulator supports μP development



An in-circuit emulator subsystem, the RTE8/8800, supports hardware and software development of Am9080A/8080A, Am8085, Am8048 and Z80 microprocessors. The emulator operates with the AmSYS 8/8 development system in either a single or multiple emulator environment. The emulator can also be configured as a subsystem of the AmSYS29 bit-slice microprocessor development system. No matter which processor a user wishes to emulate, the only additional hardware required is the board containing the CPU and interface circuitry unique to that processor. Basic hardware of the subsystem includes a control processor board, a communications board, a debug board and a real-time trace module. The subsystem costs $4350; the microprocessor modules range from $1180 to $2250.

Advanced Micro Computers, 3340 Scott Blvd., Santa Clara, CA 95051. (408) 988-7777.

CIRCLE NO. 374

Disk carts warn of media damage

Guardian series disk cartridges, designed for small system disk storage files, use impact detectors to warn of possible damage to the media. The detectors, called Shockwatch, consists of capillary tubing containing a thread of liquid. Dispersing action of the liquid, caused by shock or acceleration exceeding predetermined levels, changes the liquid from clear to brilliant red. Cartridge housings use special door, hinge and latch enhancements to assure positive sealing when inserting or removing a cartridge from the disk file.

Memorex CFI Div., 1401 E. Orangethorpe St., Fullerton, CA 92631. (714) 738-6100.

CIRCLE NO. 375

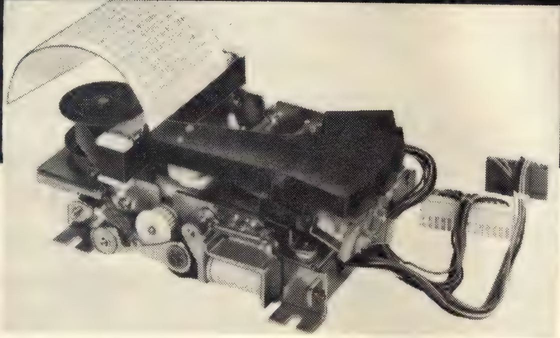
Fast serial printer works in IBM systems

A fast serial printer, 6541-04, performs well in IBM's System/34. Designed as an alternative to IBM's Model 5256, the new printer is compatible with the Series/1, System/38 and 5280 distributed data systems. The compact table-top prints bidirectionally across a full 132 columns.

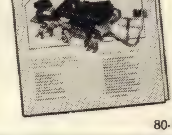
Decision Data, 100 Witmer Rd., Horsham, PA 19044. (215) 674-3300. 8 to 9 wks.

CIRCLE NO. 376

NEW! STAR MICRONICS MODEL DP-822 MINIATURE DOT MATRIX IMPACT PRINTER



STAR'S NEW MODEL DP-822 is the ideal alphanumeric printer for automated banking terminals, desktop calculators, electronic cash registers, medical and scientific instruments— and many other products requiring a reliable, low-cost dot matrix impact printer. It has a replaceable printing head with minimum life expectancy of 15-million characters and is operated by a single 12-volt DC power supply. You get up to 21-column hard-copy printing at a speed of 2.5 lines per second with serial impact strong enough to print two clear copies on carbonless tapes or a single copy on standard 2¼" adding machine tape. A 5 x 7 matrix array yields printed characters in any alphanumeric font up to .071" wide by .114" high. The Star DP-822 costs only $42.95 each in quantities of 1000 units—and control electronics also are available at low cost. Write today for complete information.



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CIRCLE NO. 141

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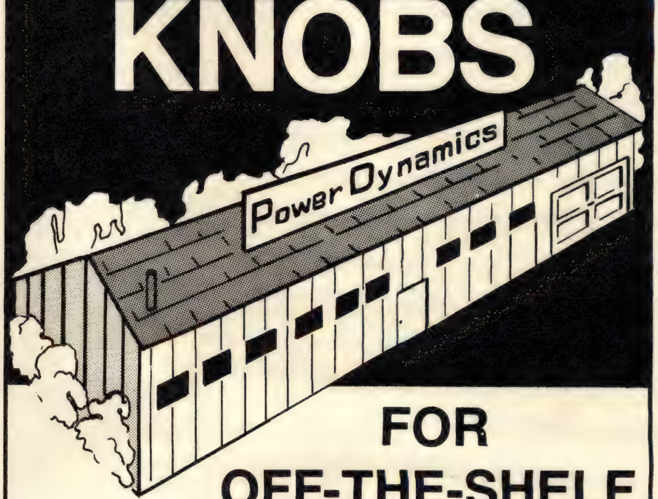

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CIRCLE NO. 142

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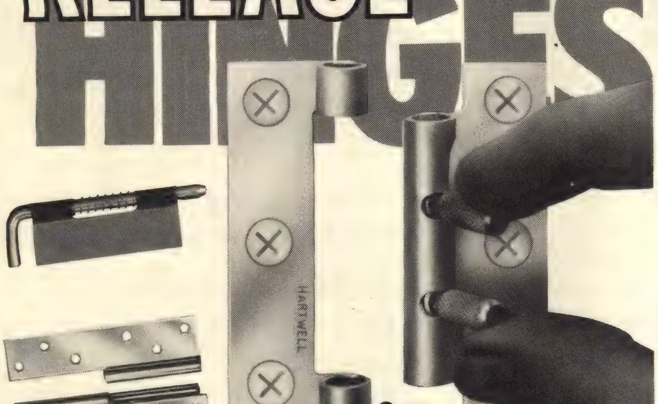

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CIRCLE NO. 144

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SYSTEMS: Airborne, Radar & Troposcatter, Satellite Communications, ECM, IFM & Reconnaissauce, TWT Replacement in Existing Systems.

AMPLIFIER

GERMANIUM

Part Number	F_{RO} GHz (Min)	R_M ohms (Typ)	R_S ohms (Typ)	C_j pF (Typ)	K (Typ)
7510G	10	75	3	1.1	1.25
7515G	15	75	3	0.72	1.30
7520G	20	75	4	0.46	1.35
7525G	25	75	5	0.32	1.40
7530G	30	75	5	0.27	1.40
7540G	40	75	6	0.18	1.45
7550G	50	75	7	0.13	1.45

SWITCHING

GERMANIUM

Part Number	Ip (mA)	Ip tolerance typ	Vp (mV) typ	V_F (mV) typ	C_t (pF) Typ	C_t (pF) Max
5050G	5	5%	70	480	2	5
1050G	10	5%	80	500	4	5
2050G	20	5%	90	540	8	10
5100G	5	10%	70	480	2	5
1100G	10	10%	80	500	6	10
2100G	20	10%	90	540	15	20
5010G	50	10%	100	565	30	50
1010G	100	10%	110	575	60	100

GALLIUM ARSENIDE

Part Number	Ip (mA)	Ip tolerance typ	Vp (mV) typ	V_F (mV) typ	C_t (pF) Typ	C_t (pF) Max
5050A	5	5%	135	1050	2	5
1050A	10	5%	155	1100	4	5
2050A	20	5%	175	1125	8	10
5100A	5	10%	135	1050	2	5
1100A	10	10%	155	1100	6	10
2100A	20	10%	175	1125	15	20
5010A	50	10%	195	1150	30	50
1010A	100	10%	205	1175	60	100

DETECTOR

TYPICAL VALUES

DIODE TYPE	TEST FREQUENCY	TSS*	Figure of Merit $\gamma/\sqrt{Rv}$	Video Resistance $Rv\,\Omega$
100BD	2GHz	−58 dbm	300	400
	4GHz	−56 dbm	750	400
	8GHz	−52 dbm	75	400
	16GHz	−47 dbm	40	400
150BD	2GHz	−59 dbm	230	120
	4GHz	−57 dbm	195	120
	8GHz	−52 dbm	100	120
	16GHz	−46 dbm	55	120
200BD	2GHz	−55 dbm	110	80
	4GHz	−54 dbm	100	80
	8GHz	−51 dbm	100	80
	16GHz	−45 dbm	85	80

*2MHz Bandwidth

CCI Capability: Tunnel Diodes for Oscillators, Detectors, Amplifiers and Switches. Back Diodes & Schottky Diodes for Detector-Mixer Applications. CCI can provide all of its products tested to MILS-19500 HI-REL requirements or specific customer HI-REL requirements including 100% prescreening x-ray, environmental and accelerated aging tests. Devices with special characteristics or special packages to fit unique requirements can be made for you in a short time.

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Telex 132-445

CIRCLE NO. 145

Apples do word processing or information analysis

One Apple III computer system handles word processing, the other managerial applications; both feature a built-in floppy drive.

Two versions of Apple Computer, Inc.'s latest small computer offer capabilities for users who need either word-processing or information-analyst capabilities. Economical as well as versatile, the two Apple IIIs feature a central processor that allows a relocatable base-page register, 128 kbytes of main memory and a self-contained floppy-disk drive. In addition, a large selection of peripheral devices is combined with the Sophisticated Operating System (SOS) to make all system operations user-transparent.

Both versions also include 96 kbytes of RAM, a built-in 5-1/4-in. floppy drive with 143 kbytes of capacity, 12 in. black and white video monitor, two printer interfaces and a keyboard with 74 keys in addition to a separate 13-key numeric keypad.

The Information Analyst package includes SOS Visicalc III, a mail list manager, and Apple Business Basic. The Word Processor offers SOS and word-processing application and training software. This version can be interfaced to a thermal or letter-quality printer.

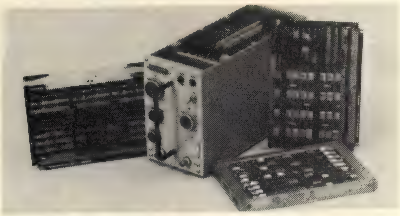
An Apple-designed central processor features a superset of the 6502A instruction set, a relocatable base-page register, a relocatable stack and a 128-kbyte address range. Peripheral devices may request machine attention by interrupting the CPU, or the CPU may poll peripherals.

The Word Processor will sell for $5400 with the thermal printer and $7800 with the letter-quality printer. Customer shipments begin this coming August. The Information Analyst will sell for $4400, and shipments will begin in July, 1980.

Apple Computer, Inc., 10260 Bandley Dr., Cupertino, CA 95014. (408) 996-1010.

CIRCLE NO. 413

16-bit mini operates in severe environments



A ruggedized equivalent of the popular DEC PDP-11 minicomputer, the SECS 2, operates in severe environments. Potential users include the military, aircraft systems and shipboard data gathering and intelligence systems. The 16-bit minicomputer is fully compatible with PDP-11 operating systems and applications software. It is available in either one-half or full ATR (air transport rack) versions. Support modules for SECS 2 include an RS-232 I/O device, 1553B bus I/O, a tape memory system and various sizes of EPROM, ROM, RAM and core memory modules.

EMM/SESCO, 20630 Plummer St., Chatsworth, CA 91311. (213) 998-9090.

CIRCLE NO. 377

Disk system suits 6800/6809 users

A version of the Flex disk operating system runs on custom or nonstandard 6800 and 6809 systems. Flex supports such features as dynamic filespace allocation, random and sequential file accessing, user startup facility, user environment control, English error messages and over 20 commands for all normal disk operation. The new version comes with a 100-page guide.

Technical Systems Consultants, Inc., P.O. Box 2570, 1208 Kent Ave., West Lafayette, IN 47906. (317) 463-2502. $150.

CIRCLE NO. 378

Stand-alone μCs get ready for networking

Three stand-alone, entry-level microcomputer systems, the MCZ-2 Series, come to the market in preparation for local networking capability to be added later in 1980. The computers are offered in modular building-block increments. Single stations will be linked by Z-Net for multistation and multiprocessing functions. MCZ-2/20 is a table-top system without peripherals or software, priced at $5990. With 2.4 Mbytes of floppy disk storage, the price is $10,250. A 19-in. rack-mount version is designated MCZ-2/25. A complete, ready-to-run package, MCZ-2/50 costs $12,175 and includes a MCZ-2/20 with 2.4 Mbytes of storage, a CRT, an operating system.

Ziolog, 10460 Bubb Rd., Cupertino, CA 95014. (408) 446-4666.

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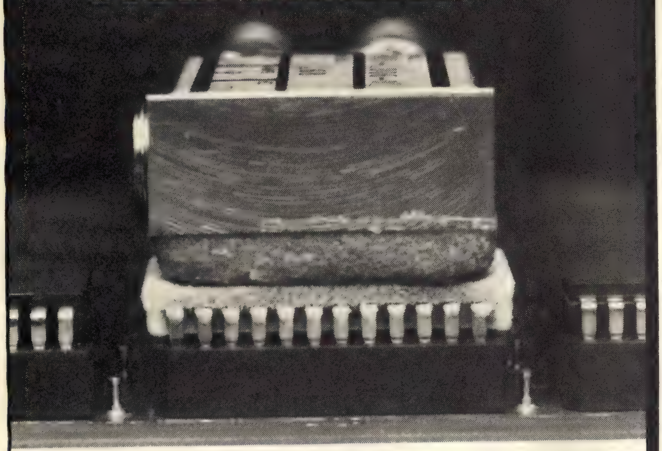

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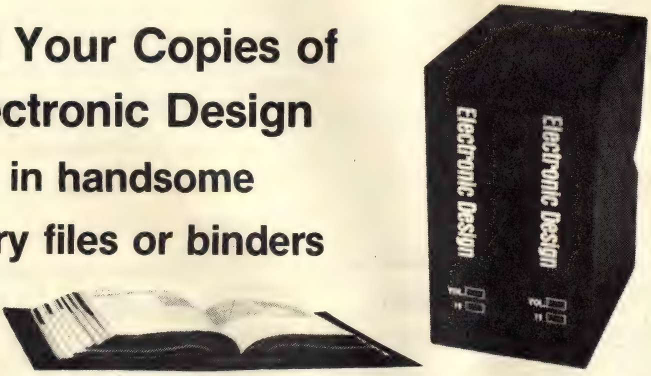

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Model MR-1824. Two Station. Left station provides selective print to 18 characters, independent paper feed, auto paper take-up, slip insertion/validation plus desirable options. Right station provides selective print to 24 characters, independent paper feed, tear off blade and optional logo print. Both stations provide last line visibility.

Model MR-1824
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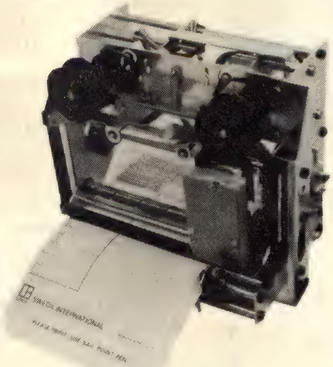
Bi-directional or uni-directional print capability. Speed: 1.4 lines per second.



Model MS-4000. Accommodates various size slips or forms. Cam-operated, geared friction paper feed. Provided with optional sensor for each top and bottom slip position. Adjustable slip stop for table extension, optional.

Both models available in basic mechanism only or with cables, covers and driver electronics.

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Slip Printer
Slip insertion from left side or front. 40 columns (12 cpi) at 2 lines per second. Optional bi-directional capability.

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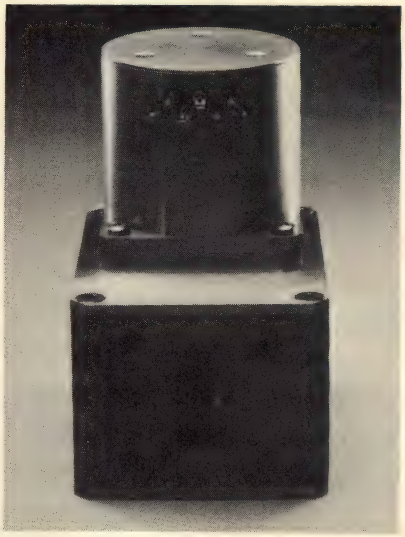
CIRCLE NO. 148

Power divider splits 7.5 to 10-GHz signals



A vane-type power divider, P/N 39D06100, provides failsafe capabilities for redundant systems operating in the 7.5 to 10-GHz range. Typical applications include combining two TWT power sources or selectable use of either. Power handling capability is 1.5 kW cw with a maximum VSWR of 1.2. Insertion loss is 0.2 dB maximum; isolation, 35 dB minimum. Maximum pull-in current is 0.5 A at 28 V dc.

Transco, 4241 Glencoe Ave., Venice, CA 90291. (213) 822-0800.

CIRCLE NO. 380

Modem sends data over 7000 ft of RG62 coax

HSM 100, a synchronous modem, operates at distances up to 7000 ft over RG62 A/U coaxial cable. The modem is factory-set to operate at baud rates from 100 kbits/s to 2.5 Mbits/s. The unit interfaces with data equipment in full or half-duplex modes through RS-232 or RS-422/423 connectors. The modem includes transmit and receive clocks.

Systems Associates, 55 Park St., Troy, MI 48084. (313) 585-7995. $825.

CIRCLE NO. 381

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oduction is challenged to achieve
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rocess window and gives you new
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election, and manufacturing
chnique.

he new
SI laser with RFI
nclosure removed.
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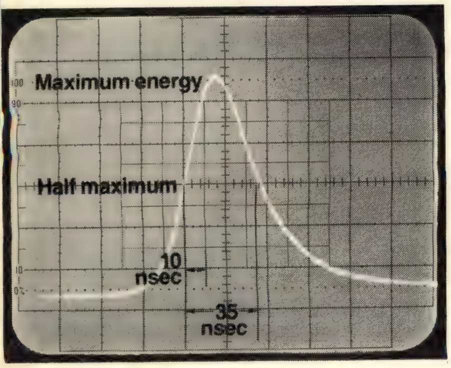
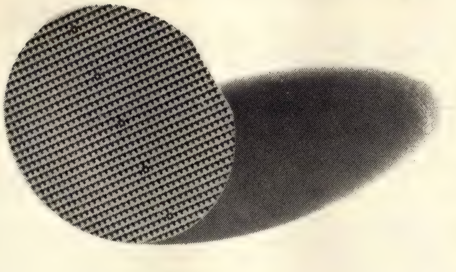
THE PULSE IS SHORT AND SWEET

By designing and building our
wn laser, we can now offer the first
short pulse capability on today's
market (30-40 nsec vs. 150-200
nsec). This means less time for en-
ergy to spread beyond your target
area, preserving resistor quality as
well as the rest of your delicate
monolithic circuitry. Cutting
polysilicon or aluminum links is
swift and clean.



A Q-switched pulse from the new ESI laser; 35 nsec full width measured at half maximum (FWHM).

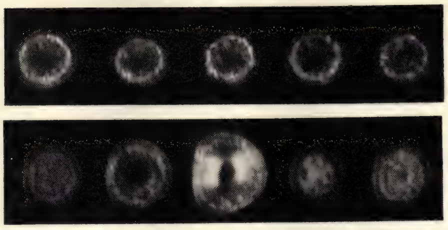
MicroLase is a trademark of Electro Scientific Industries. Inc.



CONSISTENT KERFS OVER LONG RUNS

If you're trimming resistors, you'll find the pulse-to-pulse stability of the ESI laser assures you of long trimming runs without pulse surge or dropout. (Even the energy in the initial pulse is controlled, which no other Q-switched laser can claim.)

The system's unique combination of short pulse capability, pulse-to-pulse stability, and narrower beam waist offers very accurate, very repeatable resistor trimming with minimal post-trim drift.



Consistent spot size and shape from ESI laser (top) vs. typical Q-switched Nd:YAG laser (450x magnification, tantalum nitride).

A FUNCTIONAL TRIMMING STAR

Even your sensitive circuits and special measurement instrumentation will get along with the MicroLase system. Several design innovations substantially reduce radio frequency interference (RFI), giving you a truly low-noise system for functional tuning and other wide bandwidth trimming applications.

OUR HARDWARE IS MORE THAN LASERWARE

The ESI YAG laser is but one state-of-the-art feature of the MicroLase system. Among the rest:

1. Automatic beam-to-work alignment typically within 1 micron through a new photoelectric technique (optional) or within 2.5 microns through resistor edge-sensing.

2. Kerf widths of 4 to 8 microns, made possible by a new design objective lens that also provides up to 500x viewing magnification for the system's closed circuit TV.

3. Enhanced PDP-11 capabilities with DEC's RL-01 five megabyte flying head disk and TU-58 cartridge tape unit.

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CIRCLE NO. 204

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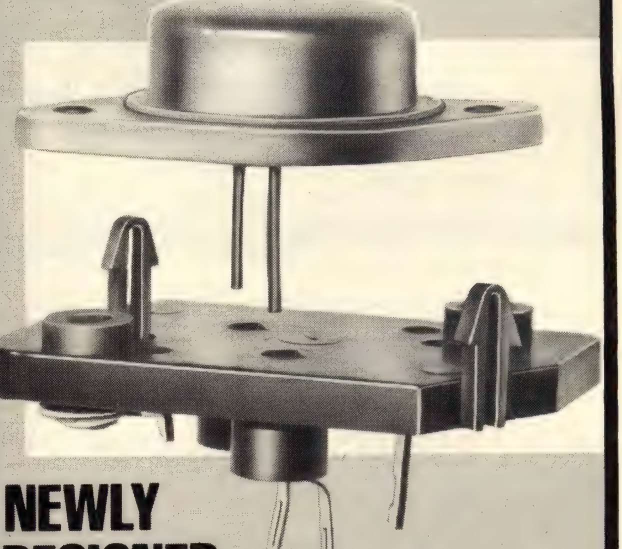

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CIRCLE NO. 205

Incentivesville Scotland

Expanding or relocating, here are nine questions you should ask about Livingston, West Lothian, Scotland.

1. Livingston?

A new town of 40,000 people. Founded 1962 by Act of Parliament to balance the decline of some older industries.

2. Where is it?

Right on the Motorway that runs along Scotland's industrial belt. 15 miles west of Edinburgh, 30 miles east of Glasgow.

Edinburgh Airport is just 10 miles away, with London 75 minutes, Aberdeen 60 minutes, and direct flights to Paris and Amsterdam. Deep sea docks 7 miles away at Grangemouth.

3. Who's there already?

Literally too many to list. Over 140 companies, with a broad manufacturing base. Three major training centres for transport and North Sea oil and gas interests.

4. How about local hassle?

One advantage of a New Town is that it is in business to welcome you, rather than hinder you. After helping 140 arrivals, our professional team are expert in smoothing out hassles for you.

5. Do these New Towns work?

There are 22 British New Towns still developing, and another 10 already developed. More than 2 million people live in them. Research says that companies like being in New Towns, and suggests that they are nearly twice as profitable as competitors elsewhere.*

6. Will we find a work force?

There is plentiful skilled and unskilled labour in the area. And among engineering companies it is being found that days lost through absenteeism and sickness in New Towns factories are less than half of that elsewhere.*

7. Will our high technology feel lonely?

At Livingston, you'll probably be right next door to some of your suppliers–or even customers. And the Scottish Universities (six of them are within a 40 mile radius) have World-wide reputations–and a notable record of co-operation with industry.

8. How about the Incentives?

Livingston is one of the nine New Towns that are designated by the current Government as Special Development areas– i.e. incoming firms can receive maximum money grants, loans and tax allowances.

And locally, you can look to us for mortgage loans and excellent factory and housing arrangemnts–including advance factories.

9. Who do I talk to?

Write to James Pollock, Industrial Development and Estates Manager, Livingston Development Corporation, Livingston, West Lothian, Scotland.
Telephone: Livingston 31177. Telex: 727178.

**Survey (1976) by the centre for Interfirm Comparison for Department of Environment, quoted in Better Buys for Business no. 9. A comparison of financial performance between a group of engineering firms in New Towns and a matched group located elsewhere.*

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CIRCLE NO. 206

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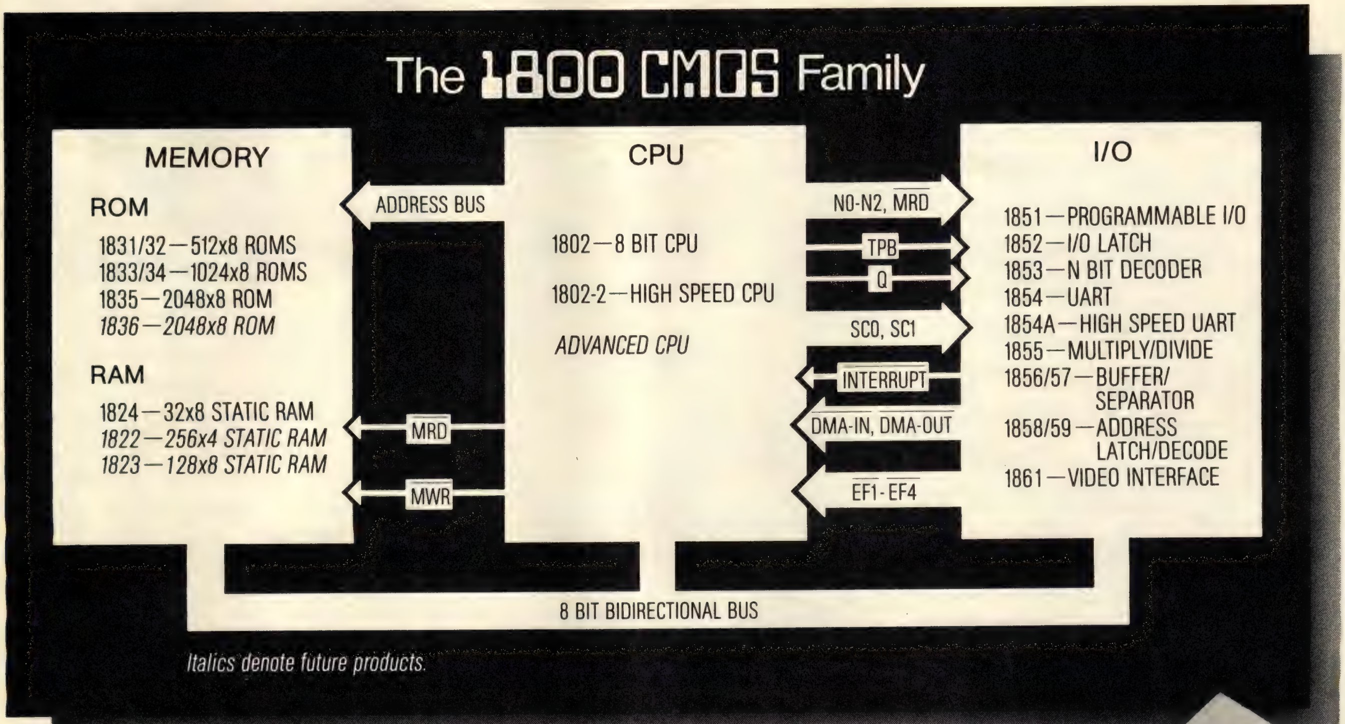

Hughes delivers a complete 1800 CMOS Microprocessor Family in both commercial and military versions.

The commercial grade devices provide low power, wide operating temperature range and the expected high noise immunity of CMOS to such diverse applications as data processors, portable instrumentation, process controllers, and complex electronic games.

The military grade version, screened to standard military reliability requirements, offers the same CMOS advantages and the exacting performance demanded by such programs as space telecommunications, aircraft navigation controls, and geophysical data logging. These units, as well as the commercial units, are available in either a 4 to 6.5 volt or 4 to 12 volt operating range.

The 1800 CMOS Microprocessor Family offers an extensive complement of memory and I/O devices, including such new parts as the 1851 Software Programmable Input/Output Port and the 1855 Eight-Bit Expandable Multiply/Divide units. In addition, several new support devices are being designed for introduction in 1980.

The support doesn't end at the device level; Hughes offers an inexpensive, easy-to-use Hughes Microprocessor Development System which includes a real time hardware emulator. High level software language is also available. In addition to the 1802 CMOS Microprocessor, the Hughes Development System supports other industry-standard microprocessors.

Write for our new 24-page, 1800 CMOS Product Guide; for further information, call (800) 854-3515 or (714) 759-2907.

Solid State Products Division
500 Superior Avenue
Newport Beach, CA 92663

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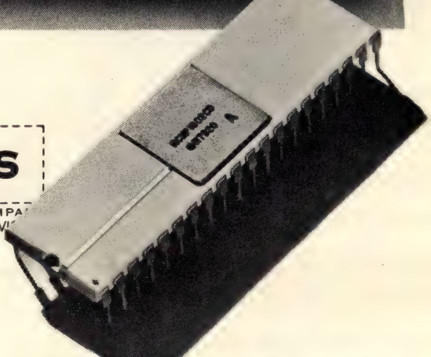

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500 Superior Avenue Newport Beach, CA 92663

I would like more information on the Hughes 1800 CMOS Family.

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Company ____________ Title ____________

Address ____________________

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Telephone ____________ Ext. ________

Application ____________________

ED 6/80

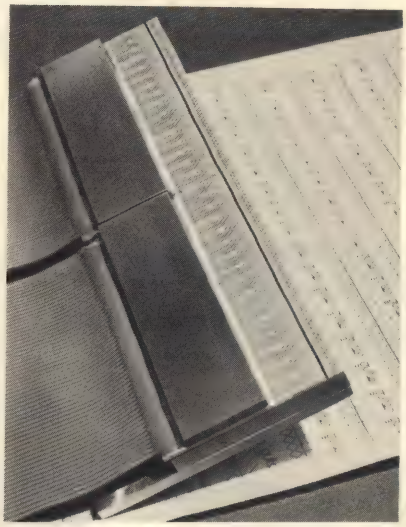
CIRCLE NO. 207

Synthesizers assure clock system accuracy

Use of three separate frequency synthesizer cards, with full voting among the cards, assures increased dependability from a clock distribution system, the CDS-10. The system's three reference oscillators provide a total of 155 different frequencies from 50 Hz to 3.072 MHz on 84 balanced or 168 unbalanced outputs. In the triplicated frequency synthesis technique, a reference oscillator, in disagreement with the other two, will be automatically removed from the common frequency bus.

Versitron, 6310 Chillum Pl. N.W., Washington, DC 20011. (202) 882-8464. **CIRCLE NO. 382**

Preganged printheads spread to almost 9 in.



Preganged thermal printheads, GM series, give users a choice of printing widths from 4.1 to 8.9 in. Rigid edge-to-edge mounting and precise fabrication of the printheads makes the gap between heads almost undetectable. Although factory preganged, the heads are individually adjustable and replaceable. Dot densities from 50 to 100 dots/in. are offered. Using 5 × 7 dot matrix characters, up to 132 columns can be attained. Five standard assemblies are available with 12-in. flexible cables and stripped ends.

Gulton Hybrid Microcircuit, 212 Durham Ave., Metuchen, NJ 08840. (201) 548-2800. $128 to $245 (50 qty); 6 to 8 wks.

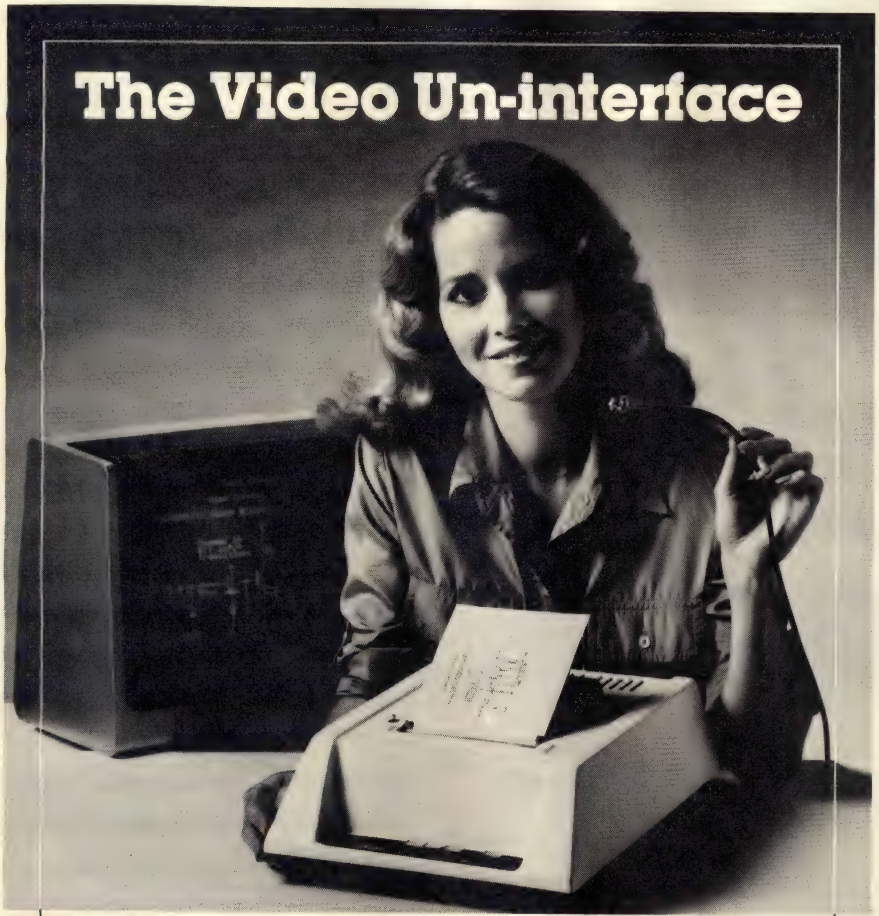
CIRCLE NO. 383

Crystal oscillators stay close to frequency

Series 80 hybrid crystal oscillators feature a frequency stability of 1 ppm. The units, supplied in a DIP configuration, cover frequencies from 4 to 60 MHz with TTL outputs. Sine wave versions are available.

Accutronics, 628 North St., Geneva, IL 60134. (312) 232-2600.

CIRCLE NO. 384



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The Axiom EX-850 Video Printer is uniquely different because it requires absolutely no hardware or software interface. Instead, it connects to the standard video input of your CRT terminal, video monitor or TV set. You can even select normal or high resolution, and positive or negative image.

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In the United Kingdom:
Hybrid (Component) Systems U.K. Ltd.
12A Park Street, Camberley, Surrey
Tel. (0276) 28128 (TELEX 858720 HYBRID G)

CIRCLE NO. 209

New Literature

Suppressors, diodes

Detailed device characterization and applications information on suppressors, transistors and diodes are covered in a 286-page catalog. General Semiconductor Industries, Tempe, AZ

CIRCLE NO. 385

Antenna positioners

Specifications and applications data for single and multi-axis positioners, antenna positioner control units, analog and digital angle displays are included in a catalog. Scientific-Atlanta, Atlanta, GA

CIRCLE NO. 386

Instruments

A 14-page booklet describes, using color photographs, 119 products that are HP-IB (IEEE-488) compatible. Hewlett-Packard, Palo Alto, CA

CIRCLE NO. 387

Data modem

Photographs, system diagrams and a description of the TA201C Bell-compatible data modem's diagnostic features are given in a catalog. Rixon, Silver Spring, MD

CIRCLE NO. 388

Keypads, keyboards

Component keypads and keyboards for use with stock or custom faceplates are listed in a catalog. W.H. Brady Co., Electronic Products Div., Milwaukee, WI

CIRCLE NO. 389

Relays

Military qualified relays, industrial, commercial and computer-grade relays and rf relays are featured in a 64-page catalog. A selection chart is included. Hi-G, Relay Div., Windsor Locks, CT

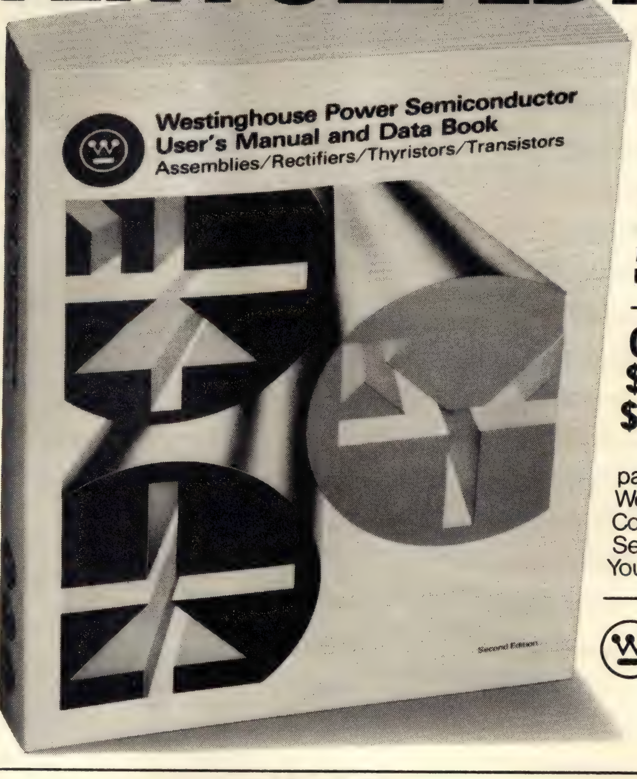
CIRCLE NO. 390

Mounts, spacers

Over 1528 standard product styles and sizes of mounts, spacers and spreaders for component packaging onto PC boards are featured in a packaging digest. Bivar, Santa Ana, CA

CIRCLE NO. 391

A POWER FULL EDITION.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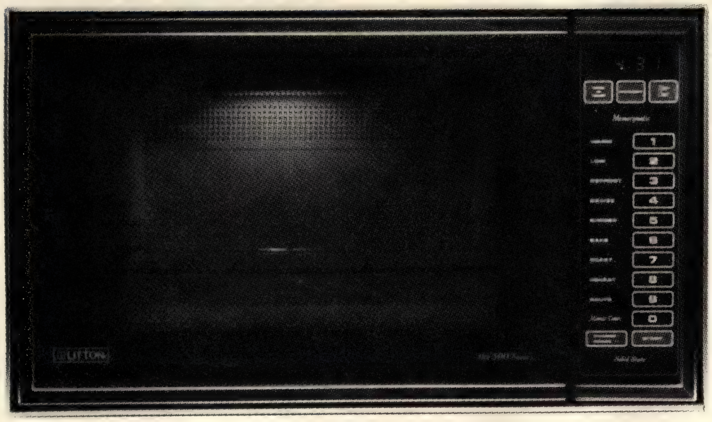

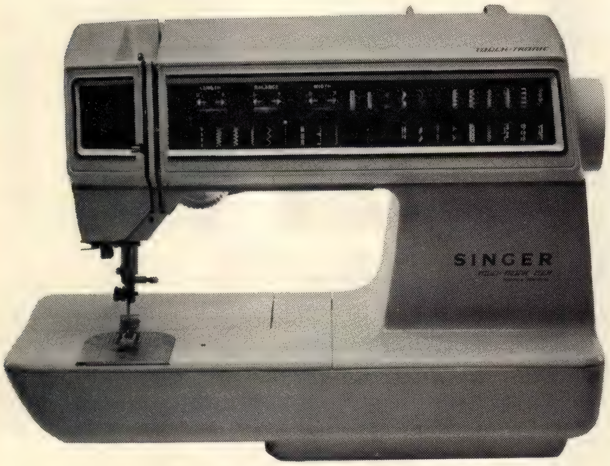

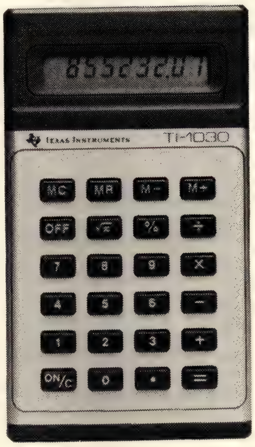

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CIRCLE NO. 211

New Literature

Data converters

Specifications for data converters, linears and nonlinears, power supplies and s/h amplifiers are given in a short-form catalog. Teledyne Philbrick, Dedham, MA **CIRCLE NO. 392**

Polyimides

High performance polyimides are described in a 32-page catalog. Separate sections detail applications and part design guidelines. Rogers, Lithonia, GA **CIRCLE NO. 393**

Pressure transmitter

A two-wire pressure transmitter is highlighted in a data sheet. Operational specifications are given. Sensotec, Columbus, OH **CIRCLE NO. 394**

X-Y recorders

Four X-Y recorders, for OEM use, lab, medical and industrial applications, are featured in an eight-page catalog. Esterline Angus Instrument, Indianapolis, IN **CIRCLE NO. 395**

Interconnections

Fiber-optic interconnections design features and performance characteristics are included in an eight-page catalog. Amphenol North America Div., Oak Brook, IL **CIRCLE NO. 396**

Communication buffers

Line printer communication buffers, minicomputer controllers and interfaces and the PXF printer transfer switch are described in a two-page data sheet. Digital Associates, Printer Systems, Stamford, CT **CIRCLE NO. 397**

Thermistors

A two-page brochure, illustrated with sketches and temperature graphs, covers negative temperature coefficient thermistors. Gulton Industries, Piezo Products Div., Metuchen, NJ **CIRCLE NO. 398**

Conductive glass fibers

Applications and specifications of conductive glass fibers are given in a four-page brochure. Lundy Electronics & Systems, Pompano Beach, FL **CIRCLE NO. 399**

Thermostatic equipment

Included in a 20-page brochure is detailed information on over 40 models of thermostatic equipment, which yield a product line temperature range of −30 to 400 C, in bath sizes ranging from 3.5 to 50 liters. Science/Electronics, Dayton, OH **CIRCLE NO. 404**

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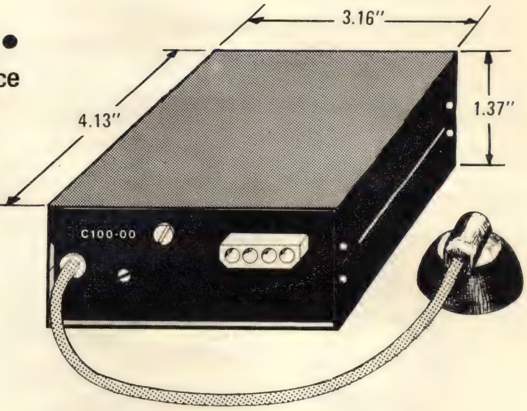

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The Champ delivers another knockout:

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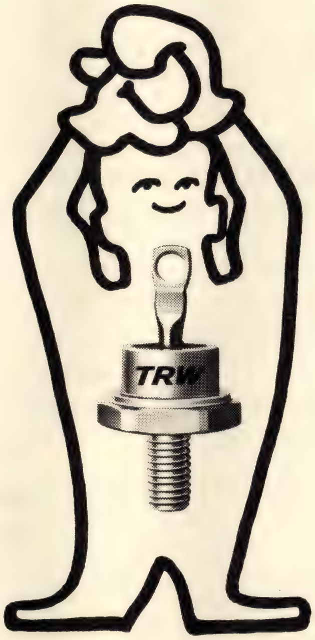

TRW's line of high power Schottky Diodes is now bigger, broader and better performing than ever. And new production capacity means we can deliver **all** the goods. Faster.

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For immediate information on TRW Schottky diodes, call John Power at (213) 679-4561.

TRW Schottky Diodes

Part No.	I_F Rating	V_R	T_j	Package
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SD-32	30	40	**175 °C**	DO-4
SD-231 (Dual)	30	**50**	**175 °C**	TO-3
SD-232 (Dual)	30	40	**175 °C**	TO-3
SD-71	75	**50**	**175 °C**	DO-5
SD-72	75	40	**175 °C**	DO-5
SD-75	75	45	150 °C	DO-5
SD-51	60	45	150 °C	DO-5
SD-51R	60	45	150 °C	DO-5
SD-5171	60	45	150 °C	DO-5*
SD-41	30	45	150 °C	DO-4
SD-241 (Dual)	30	45	150 °C	TO-3
1N6098	50	40	150 °C	DO-5
1N6097	50	30	150 °C	DO-5
1N6096	25	40	150 °C	DO-4
1N6095	25	30	150 °C	DO-4

*With flex lead.

ED-6

TRW Power Semiconductors
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CIRCLE NO. 212

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U.S. technology policy faces a revamping

Dwindling energy supplies, natural resource cartels, environmental concerns, unemployment and overpopulation are the visible edge of problems that U.S. technology must confront during the 1980s, according to Dr. Frank Press, science advisor to the President. At this year's IEEE Technology Policy Conference, he outlined four programs of international cooperation the U.S. must pursue to meet the coming challenges.

Where U.S. allies (Western nations) are concerned, risky and expensive development efforts (such as synthetic fuel plants) should be carried out as joint ventures.

Dealings with the Russians will get the toughest scrutiny. Any future agreements must contain as much potential benefit for the U.S. as for the USSR. However, all official technology exchanges are presently frozen in response to the invasion of Afghanistan.

Developing Third World nations should expect science and technology to be a part of any future U.S. assistance. The emphasis will be on showing recipients how to solve their own problems. The days of cash handouts are about over.

Recent progress toward normalized relations with the People's Republic of China suggest the advent of large-scale student exchanges and favored treatment for U.S. industries in China. American companies are helping the Chinese explore for oil right now.

Questioned about foreign engineering students that seek U.S. employment after graduation, Dr. Press agreed with the suggestion that they return to their native countries. These students are said to depress engineering salaries because they consider wages secondary to gaining a foothold in the U.S. Currently, about 34% of the students in graduate engineering programs in the U.S. are aliens.

Honeywell engineers organize for more pay

By reactivating the Honeywell Engineers and Technicians Association (HEAT), engineers and technicians in Honeywell's Avionics, Residential Control and Defense Systems Groups (Minneapolis, MN) are reacting to the 13% wage gains won by organized hourly workers. Honeywell's 2000 engineers and 1000 technicians have been getting 7-9% increases based on merit pool "guidelines."

About 650 people attended HEAT's first formal meeting this year on March 24. HEAT has been inactive for several years, following a successful low-keyed campaign in 1974 to remove salary inequities. In its previous life, HEAT never attained the status of a formal bargaining unit.

But all that is about to change. HEAT president David Ames says Honeywell has been officially advised of HEAT's desire to bargain for wages and benefits. Union authorization cards have been distributed, and so far HEAT has signed up about 1000 engineers. Communications to prospective HEAT members have been a problem, reports Ames. A feature article about the group, scheduled to run in the *Circulator* (in-plant newsletter), was cancelled by corporate brass.

Ames emphasizes that Honeywell engineers are not angry with the company, but merely want a better method of dealing with management than individual actions, which are fruitless.

Fed engineers caught in per diem famine

Working for Uncle Sam may hold little attraction for young engineers if the current benefits package is not improved. What really hurts are the unrealistic per diem allowances granted for job-related travel. This issue strikes home because federally employed engineers usually work with vendors on problems that cannot be settled over the phone.

Government per diem rates are now pegged at $50 per day (maximum), while personal automobile mileage is rated at 20 cents per mile (the General Services Administration pays only 18.5 cents per mile). As a result, federal engineers must put up with "fleabag" accommodations and fast-food diets while attempting to minimize unrecoverable out-of-pocket expenses, according to Thomas P. Bruderle, staff director of the National Society of Professional Engineers' Professional Engineers in Government Group.

There is legislation in the works now (HR 7072) that would offer some relief—but Bruderle calls it another case of too little too late. The bill proposes a per diem maximum of $75 for trips to high-cost cities and an increase in the mileage allowance to 25 cents. However, in metropolitan areas like New York, Washington, DC and Chicago, daily expenses can easily exceed $100.

As if that weren't bad enough, the Government only makes per diem advances for three or four days of travel. For briefer excursions, the federal employee must use personal funds, which will be reimbursed. However, recovering the money can drag on for a month after the trip.

Don Mennie

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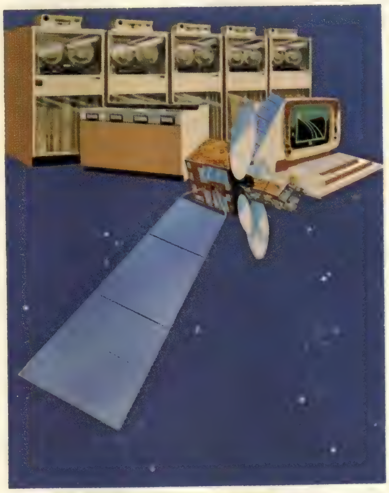

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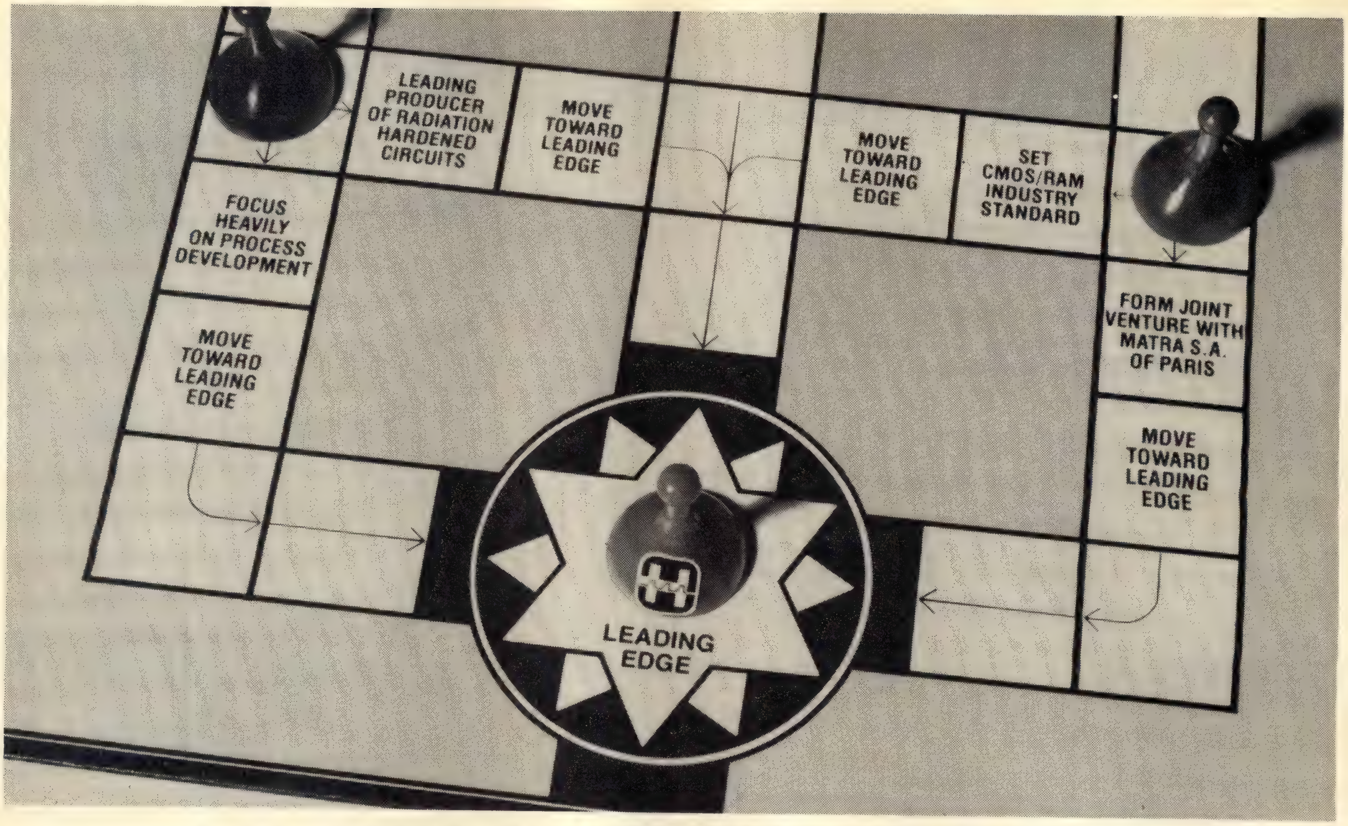
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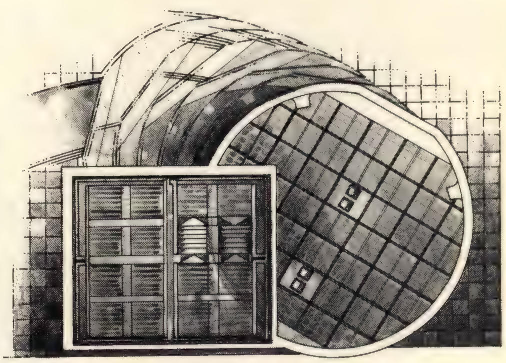

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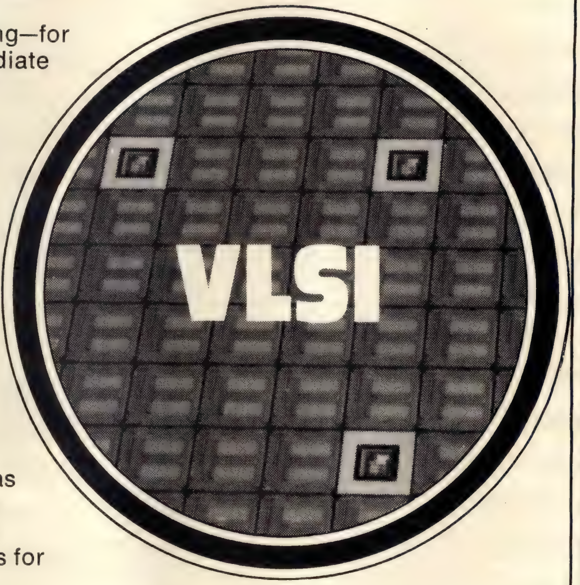

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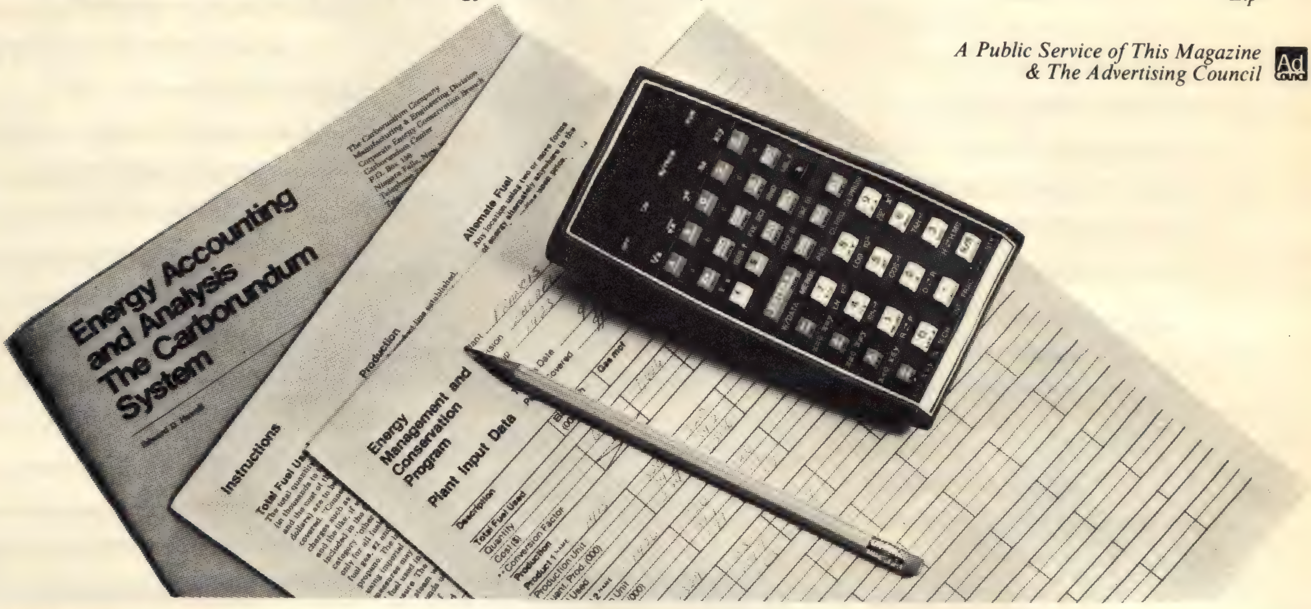
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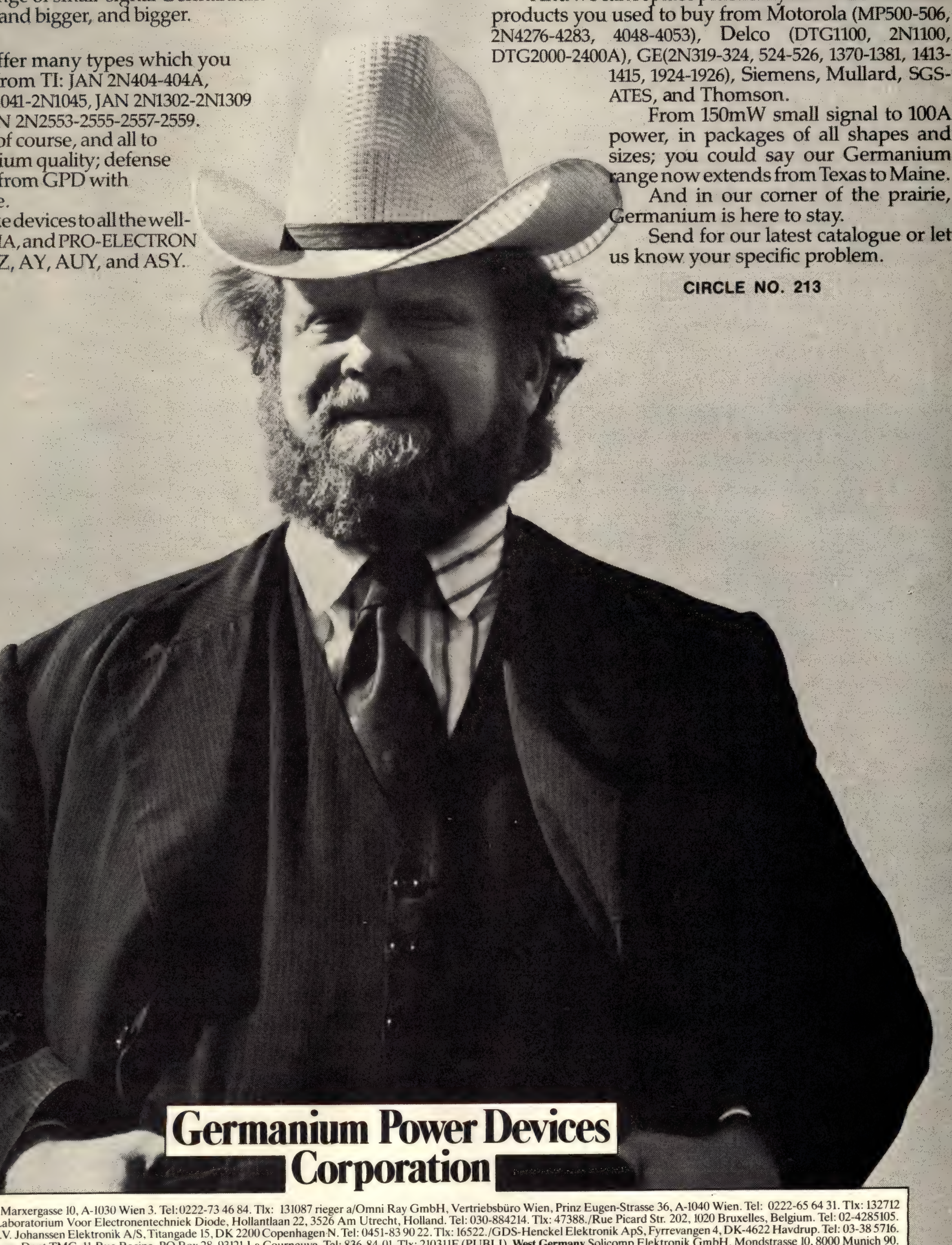

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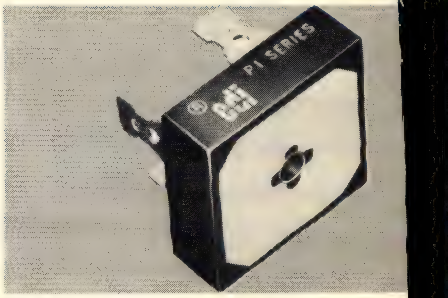

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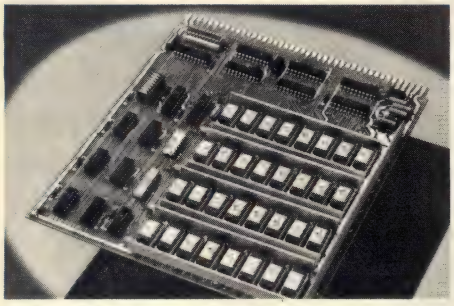

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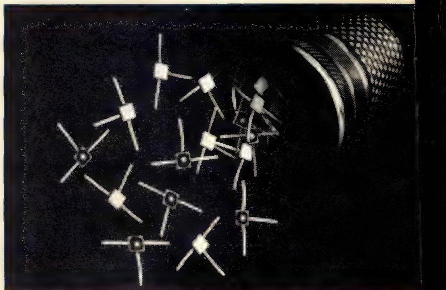

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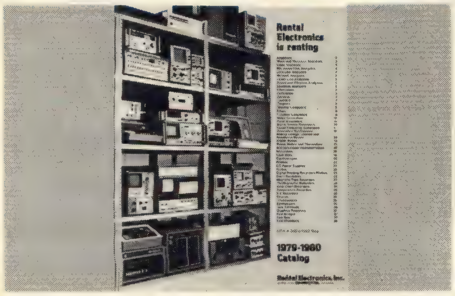

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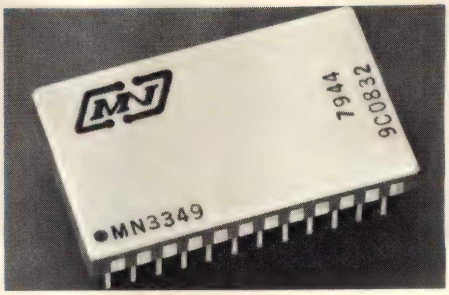

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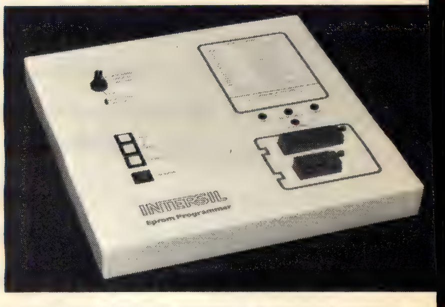

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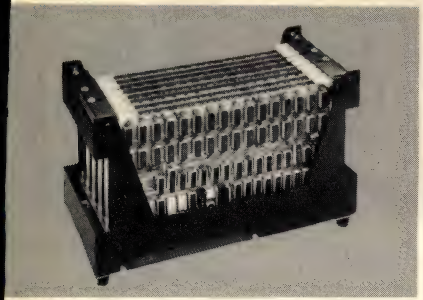

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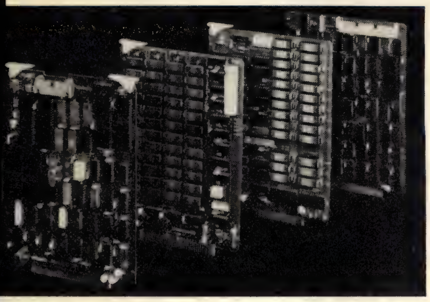

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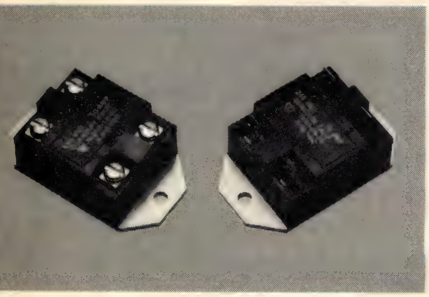

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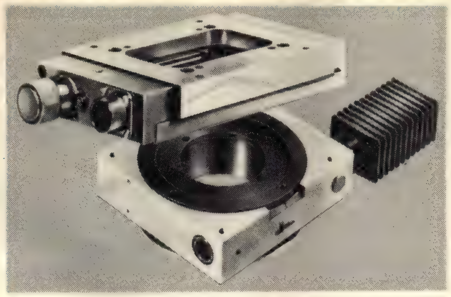

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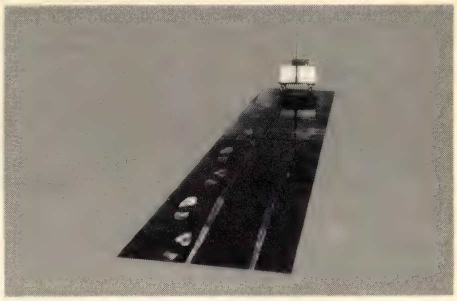

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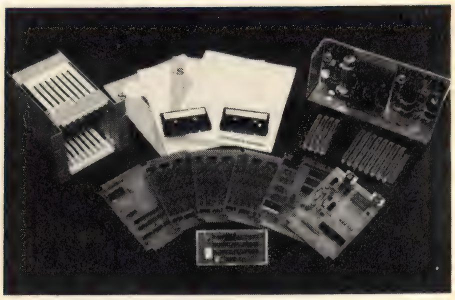

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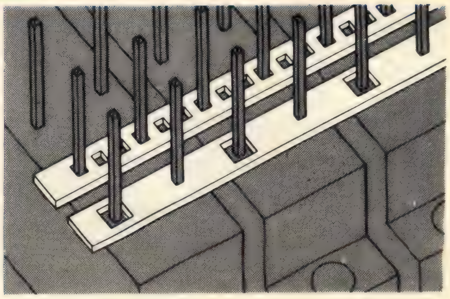

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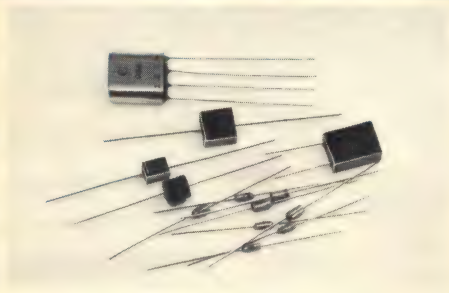

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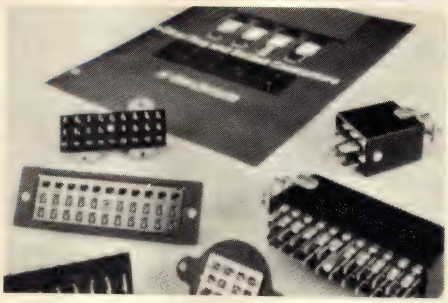

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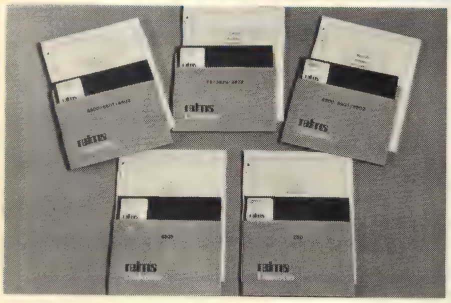

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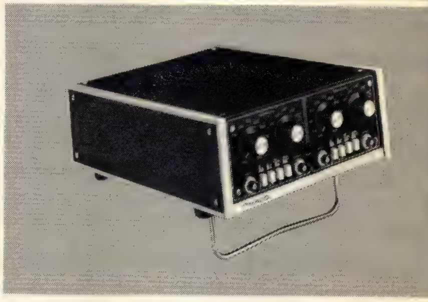

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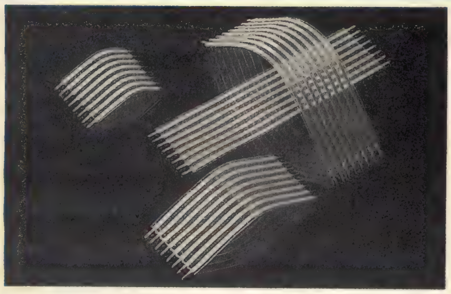

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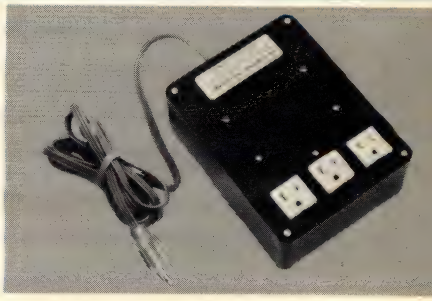

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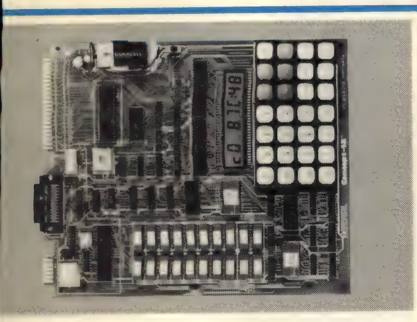

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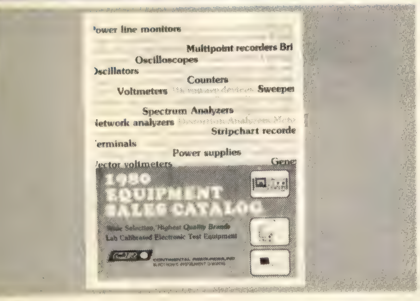

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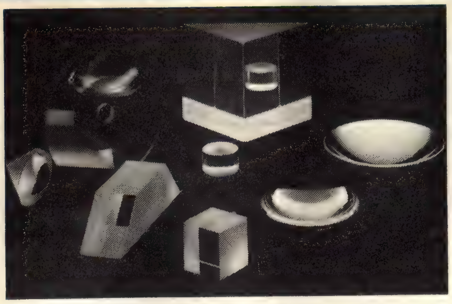

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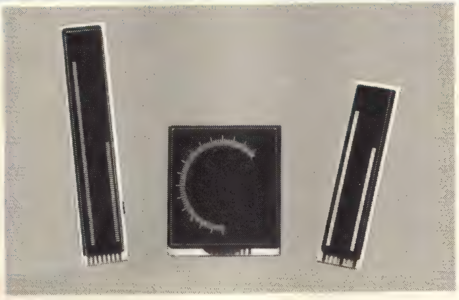

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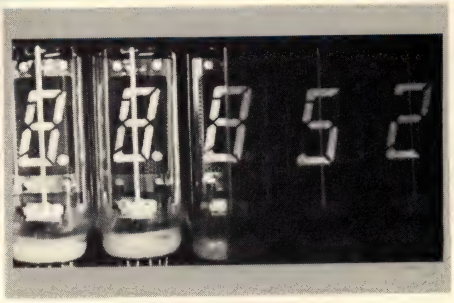

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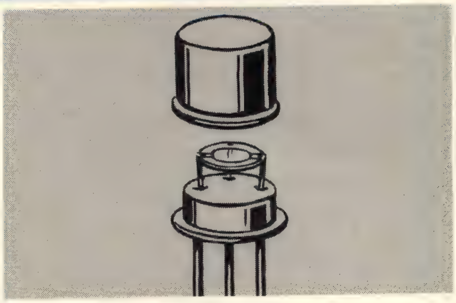

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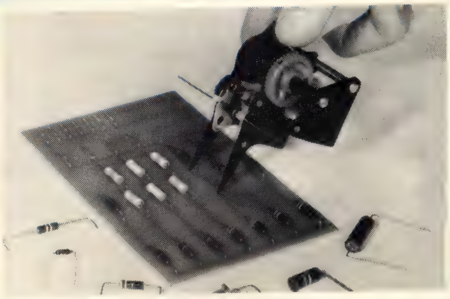

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Index Of Advertisers

AMP, Incorporated 227
AVX Ceramics Corporation †74
Abbott Transistor Laboratories, Inc. 14
Acme Spring Inc. *520
Addmaster Corporation 218
Advanced Micro Devices 6-7
Airpax Electronics, Cheshire Div. 106
Allen Bradley Co. 238
American Microsystems, Inc. †58-59
Ampex Corporation †60
Amphenol North American division Bunker Ramo Corporation 214
Analog Devices, Inc. 35, 253
Applied Microsystems 239
Axiom Corp. 282

B.H. Frank 306
B & K Precision 24
Beau Products 306
Belden Corporation 228
Boschert Inc. 85
Bourns, Inc. Cover IV
Buckbee-Mears Company 306
Burr-Brown Research Corporation 243
Burroughs Corporation 307

CTS Corporation †203
Caddock Electronics 209
Cambion 242, 260, 275
Centralab, Inc. 248, 249
Clary Corp. 305
Computer Automation, Inc. 43
Continental Resources 307
Contraves AG *52L
Cramer, Inc. 217
Cromemco 21
Cubit 251
Custom Components, Inc. 274

Data General Corporation 128-129
Data I/O Corporation 261
Datametrics, Inc. 250
Deltron, Inc. 210
Diplohmatic AS *52N
Dosc 270

EBL Co. 307
EMM-SESCO 252
Eastern Air Devices 306
Eaton Corp. 312
Eaton Corp., Cutler-Hammer 244
Elco Corporation 140
Electro Scientific Industries 277
Electronic Design *52M, 167, 168-169, 245-246, 307
Electronic Devices, Inc. 304
Electronic Hardware 251
Electronic Measurements, Inc. 213
Electronic Solutions 305
Electronic Specialists 306
Elevam Electronic Tube Co. 216
Elfab Corp. 73
Engelhard Corporation 231
Erie Technological Products, Inc. 256
Essex Group 224, 225
Exact Electronics, Inc. 233

Fairchild SATS Division 88-89
Farrand Controls 197
Ferranti Electric, Inc. †20

GTE Microcircuits 130
GenRad 188-189
General Electric Company, Semiconductor Products Department 271
General Instrument Corporation 260
General Semiconductor Industries, Inc. 108
Germanium Power Devices Corp. 303
Gold Book, The 273
Gould, Inc., Instruments Division 107
Grayhill, Inc. 226
Guardian California 305
Gulton Industries, Inc. 215

Harris Semiconductor, A Division of Harris Corporation 50-51
Harvey Electronics †17
Hartwell, Corp. 273
Harwil Co. 307
Hayden Book Company, Inc. *74, *203, 222, *278
Heinemann Electric Company 41
Hewlett-Packard 8, 12
Hughes Aircraft Company, Solid State Products 281
Humphrey, Inc. 304
Hybrid Systems Corporation 283
Hysol Inc. 232

IBM Data Processing Division 103, 104-105
ILC Data Devices, Inc. 170
IMC Magnetics Corporation 250
Intel Corporation 187
International Microcircuits, Inc. †20
Intersil 126-127, 304, 305, 307
Isotronics, Inc. 229
Ithaco, Inc. 306

Janco Corporation 15
Johnson Company, E.F. 211

Keystone Electronics Corporation 279
Klinger Scientific Corp. 305
Koh-I-Noor Radiograph, Inc. 254-255
Krohn-Hite Corporation 30

Litronix, Inc. †53
Livingston Development Co. 280

3M Company 204-205
Magnetico, Inc. 305
Mallory Corp. 308
Micro Networks Corporation 304
Micro Technical Industries 218
Microswitch, A Division of Honeywell 263
Mini-Circuits Laboratory, A Division of Scientific Components Corp. 4
Monolithic Memories, Inc. †54-55
Mostek Corporation 219
Motorola Semiconductor Products, Inc. 141-148
MuRata Corporation of America †52

NJE Corporation 247
North Atlantic Industries, Inc. 16

Optical Electronics, Inc. 266
Optical Information Systems, Exxon Enterprises Inc. 62
Oscilloquartz SA *52P

PPG Industries, Inc. 285
PTK 286
Panasonic Electronic Components Cover II
Paratronics, Inc. 177
Philips Test & Measuring Instruments, Inc. *52B, *52J&K
Phoenix Data, Inc. 304
Piezo Technology, Inc. *52-0
Plessey Semiconductors *52
Polaroid Corp. 94
Pomona Electronics, A Division of ITT 186
Power Dynamics 272
Power/Mate Corp. 37, 306
Power One, Inc. 121
Power Tech, Inc. 223
Practical Automation Inc. 240
Precision Monolithics, Incorporated 10-11
Publicitas SA 242

Qantex 93
Quartz Products Corp. 314

RCA 201, 220-221, 222
Racal Recorders †56-57
Relational Memories Systems 39, 306, 307
Renaissance Systems 307
Rental Electronics, Inc. 179, 304
Rockwell International 138
Rogers Corporation 304, 305
Rolm Corporation 206
Rolyn Optics 307
Rowe Industries 275

SGL Homalite 307
Siemens Corporation *52I, †278, †18-19
Silicon Systems, Inc. 259
Sodeco, Div. of Landis and Gyr, Inc. 258
Solid State Scientific, Inc. 230
Spectronics, Incorporated 158
Spirig 305
Sprague Electric Company 46, 267
Star Micronics 272
Step Engineering 262
Systems Consultants Inc. 64

TEC, Incorporated 241
TRW Capacitors, an Electronic Components Division of TRW, Inc. 180
TRW Power Semiconductors, an Electronic Components Division of TRW, Inc. 287
TRW/IRC Resistors, an operation of TRW Electronic Components 304
TRW/LSI Products 61
TEAC Corp. *52E
Technical Materials, Inc. 264
Tecnetics, Inc. 268
Tektronix, Inc. 44-45, 49, 124-125, 157, 235
Teledyne Crystalonics 306
Teledyne Philbrick 265
Teledyne Semiconductor 178
Tempil Division 304
Teradyne, Inc. 236-237
TESLAco., Inc. 279
Texas Instruments, Incorporated 90-91, 190
Triplett Corporation 198

Union Carbide, Electronics Div., Components Department 22-23
United System Corporation 139

Varo, Inc. 257
Victoreen Instrument Division Shellar-Globe Corporation 92

Wavetek San Diego, Inc. 1
Wes-Con Products Inc. 240, 266
Westinghouse Corporation 284
Westrex OEM Products 276
Wintek Corporation 305
Wirsbo Elektronik AB *52N
Woven Electronics 269

Xicor, Inc. 27,28-29

Yardney Electric Corporation 208

Recruitment

Allen Bradley Co. 294
American Microsystems, Inc. 298
Beall Personnell 298
Coulter Electronics, Inc. 299
E-Systems, Inc Garland Division 301
Ford Aerospace & Communications Corp-Aernutronical Div. 299
Harris Semiconductor Group 292
Hughes Aircraft Company 297
Landrum Personnel Associates 301
Litton Data Systems 300
Lockheed Electronics Company 290
NCR Microelectronics 296
Nebraska Job Service 290
Program Automation 298
Raytheon Company - Missile Systems Division 300
Sperrybunivac - Semiconductor Division 295
Staffdynamics 301
Storage Technology Corporation 298
Wang Laboratories 298

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	3610	3650	3600	3640
Diameter	⅞"	1¼"	¾"	1¼"
Standard Resistance Range (Ohms)	100-100K	100-500K	100-100K	100-500K
Resistance Tolerance	±5%	±3%	±5%	±3%
Repeatability (Voltage Ratio)	0.1%	±0.05%	0.1%	±0.05%
Power Rating (25°C)	1.5w	2.5w	1.5w	2.5w
Rotational Life (Revolutions)	50,000	100,000	100,000	100,000
Mounting Style	Snap-in	Recessed Cup	Bushing	Bushing

Save time . . . save money . . . save space. Specify Knobpot potentiometers – built only by Bourns. They're in stock now at your local Bourns distributor and available for immediate installation. Call your local Bourns representative or distributor for more information and for your new 52 page PP-1 Precision Potentiometer catalog.

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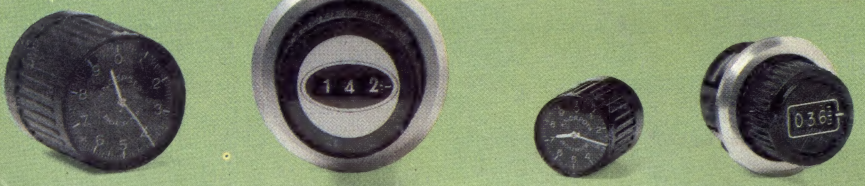

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